01. COVER

Variscite

CONTENT

Disclaimer:

SchematicS are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.

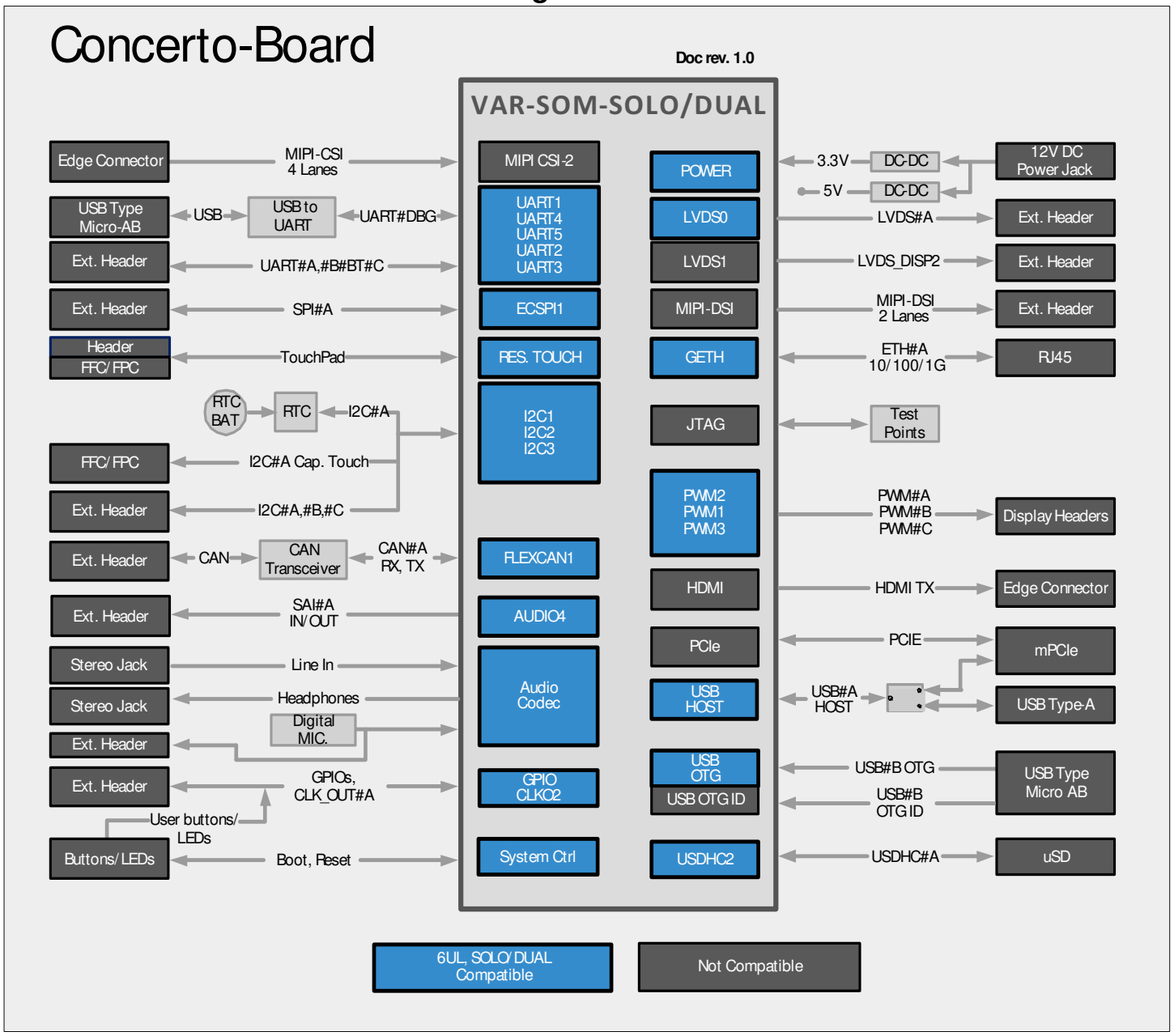
Revision History

Document	Carrier	Description
1.0	Rev 1.0	Initial
1.1	Rev 1.1	Add D25 R106 C108 for external ETH phy reset delay
1.2	Rev 1.1A	R47 add to BOM 0ohm/0402 D21 R84 Q3 - remove from BOM RX1 add manual 10K pull down on uart debug TX line
1.3	Rev 1.1A	Add VAR-SOM-6UL & VAR-SOM-SOLO/DUAL Symbols 1st Release
1.4	Rev 1.2	- Remove D21 R84 Q3 from Layout - GPLED1 - Change U17 TS3A27518EZQSR to QFN Part - RX1 Addon added to layout as R108 - R22 remove - Isolation resistor R107 on J1.154 added
1.5	Rev 1.3	FPF2193 Changed to TPS22950C
1.6	Rev 1.3	FB1,FB3,FB4 Changed to BLM15PD121SN1D J5, J9 Changed to USB3090-30-A Q1 Changed to TPS27081ADDCR U5 Changed to DS1337U+ VPC1 Changed to VPC0435-2U

Variscite

Title: 01. Cover			
Size: A3	Document Number: Concerto-Board	Project: Concerto-Board	Rev: 1.3_R1.6
Designer: Leonid S.		Approved By:	
Date: Sunday, August 27, 2023		Sheet 1 of 10	

02. VAR-SOM-SOLO/DUAL Block Diagram



Variscite

Title: 02. VAR-SOM-SOLO Block Diagram			
Size: A3	Document Number: Concerto-Board	Project: Concerto-Board	Rev: 1.3_R1.6
Designer: Leonid S.		Approved By:	
Date: Sunday, August 27, 2023		Sheet 2 of 10	

03.SOM

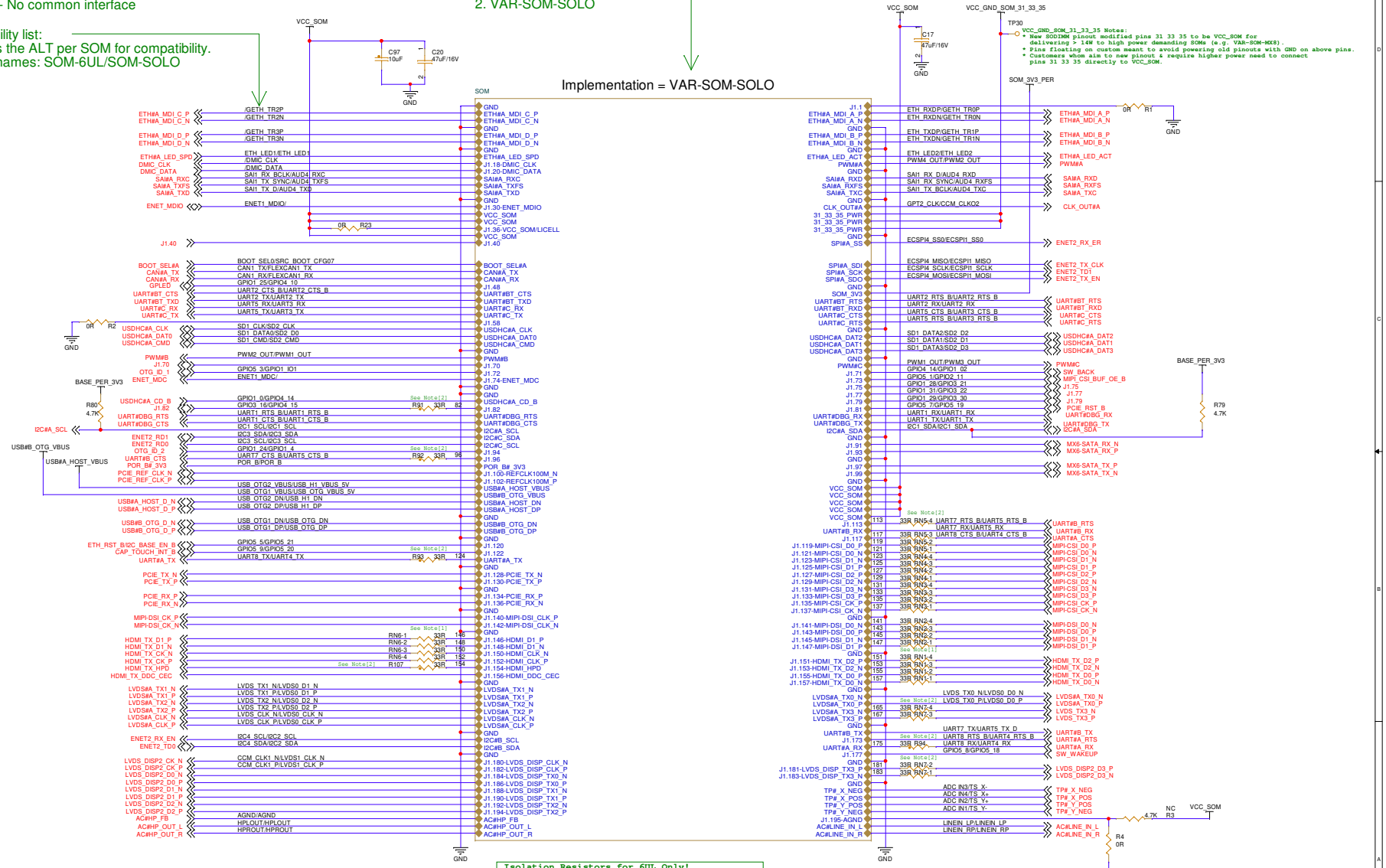
OFF Page connector index:
1. Function# - Interface common to SOM-6UL & SOM-SOLO
2. J1.xxx-Function: Interface for several SOMs
3. J1.xxx - No common interface

Compatibility list:
Describes the ALT per SOM for compatibility.
Order of names: SOM-6UL/SOM-SOLO

For cross probing between SOM symbol and the specific SOM Connector used, set the "Implemetation" property value in SOM port symbol to one of the following:

1. VAR-SOM-6UL
2. VAR-SOM-SOLO

Implementation = VAR-SOM-SOLO



Isolation Resistors for 6UL Only!

Note[1] Resistor for isolating stubs & minimizing emc radiation. Signal shared on SOM-6UL ENET1* bus.

Note[2] Resistor for isolating stubs & minimizing emc radiation. Signal shared on SOM-6UL LCDIF* bus.

Variscite

Title: 03A. VAR-SOM-6UL_CONN			
Size: C	Document Number: Concerto-Board	Project: Concerto-Board	Rev: 1.3_R1.0
Designer: Leonid S.		Approved By:	
Date: Sunday, August 27, 2023		Sheet 3 of 10	

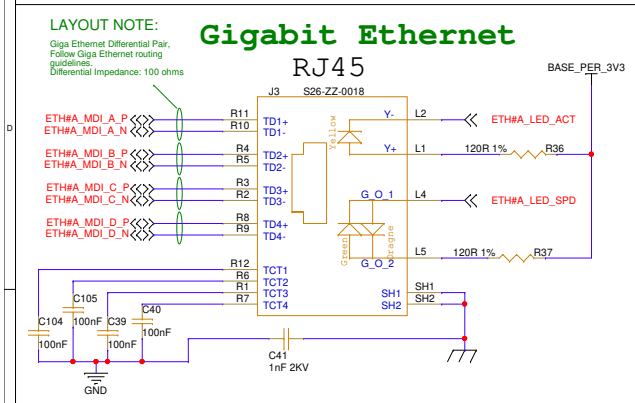
04. VAR-SOM-SOLO/DUAL Connector

Variscite

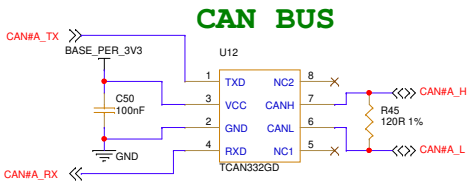
Title: 04. VAR-SOM-SOLO Connector			
Size: A2	Document Number: Concerto-Board	Project: Concerto-Board	Rev: 1.3_R1.0
Designer: Leopold S.		Approved By:	
Date: Sunday, August 27, 2023		Sheet 4 of 10	

05. Ethernet, Audio, CAN

Gigabit Ethernet RJ45

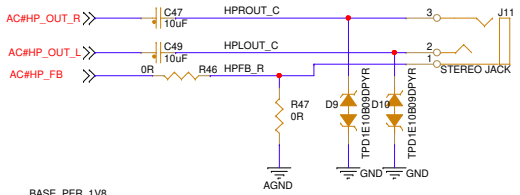


CAN BUS

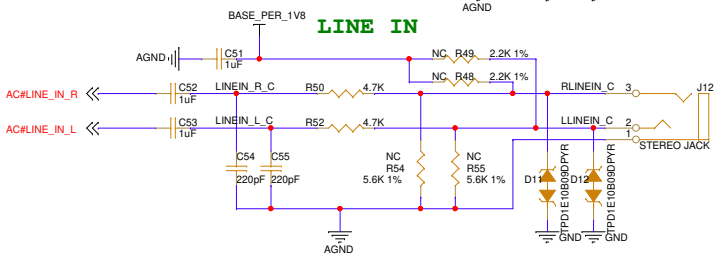


AUDIO

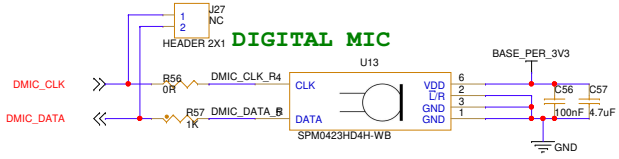
HEADPHONES



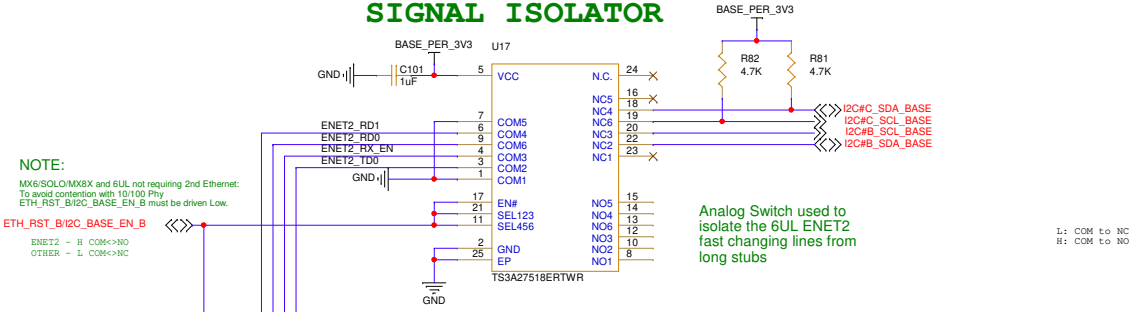
LINE IN



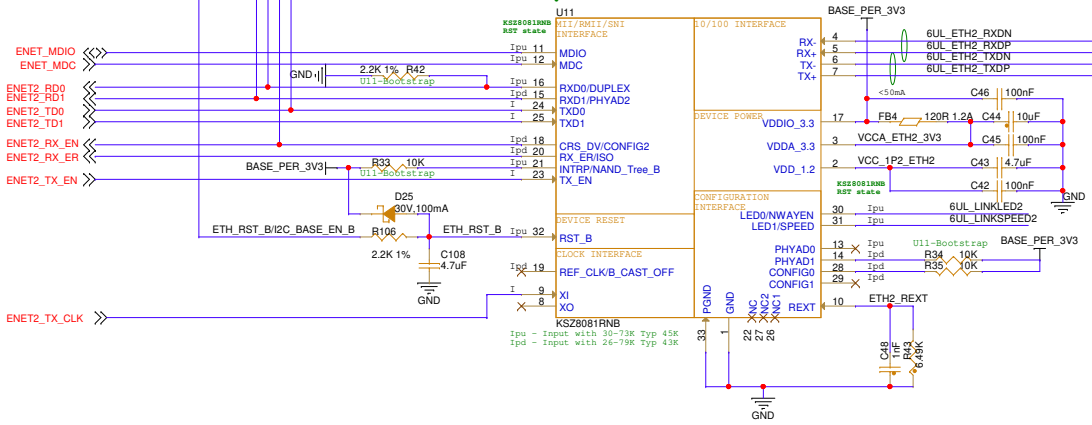
DIGITAL MIC



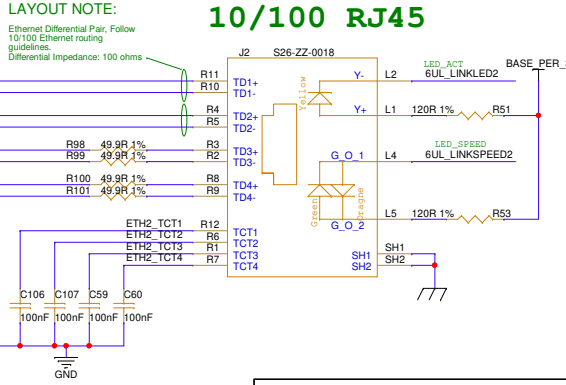
SIGNAL ISOLATOR

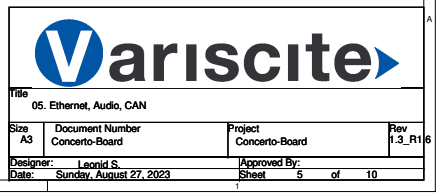


SOM-6UL 10/100 ENET2 PHY



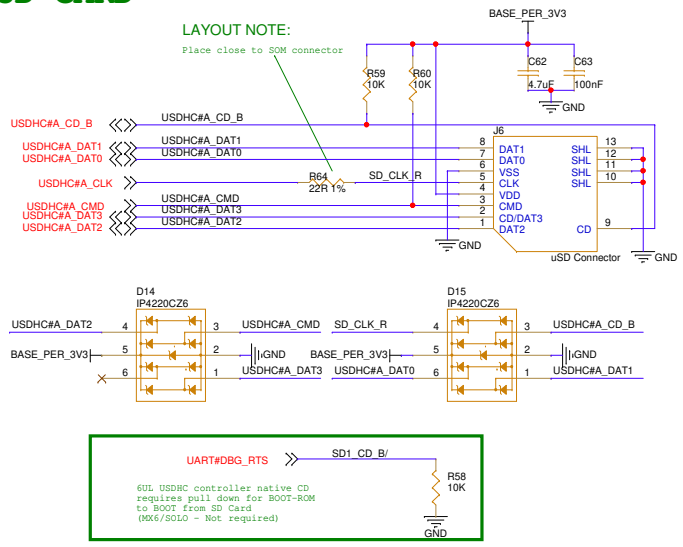
SOM-6UL 10/100 RJ45



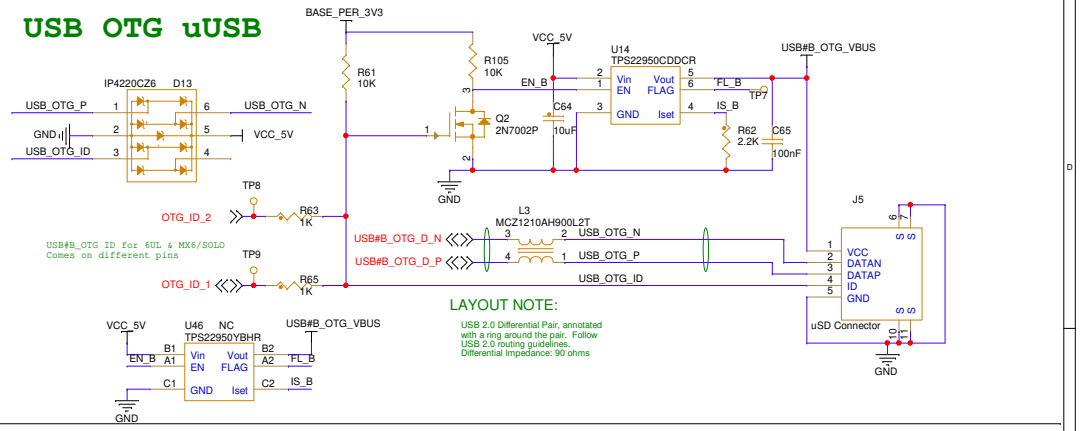


06. USB, AUDIO, PCIe, SD, SATA

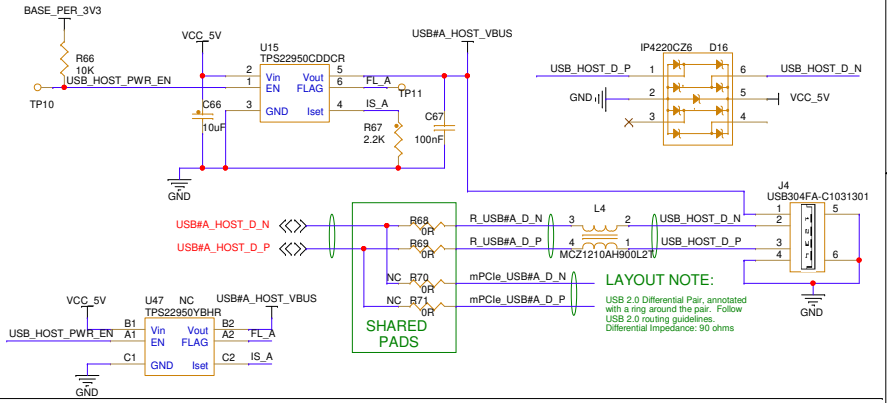
uSD CARD



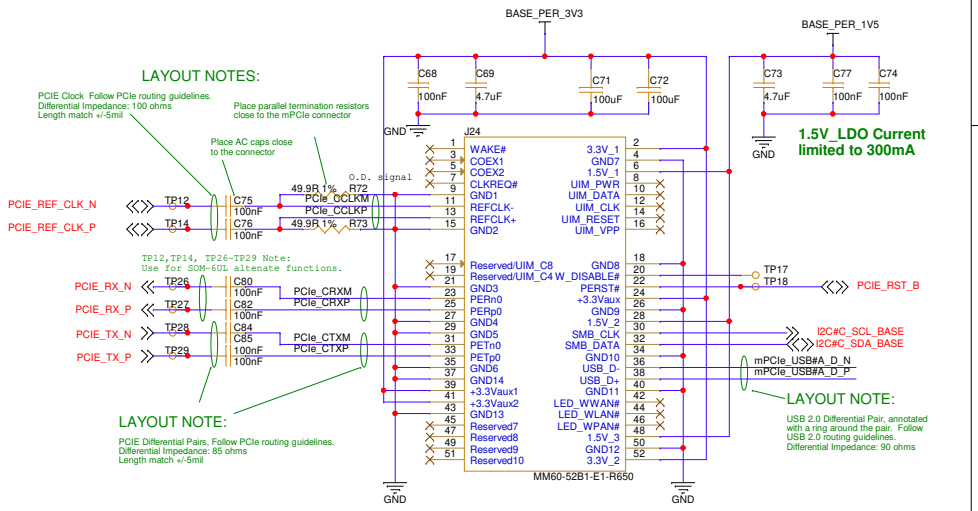
USB OTG uUSB



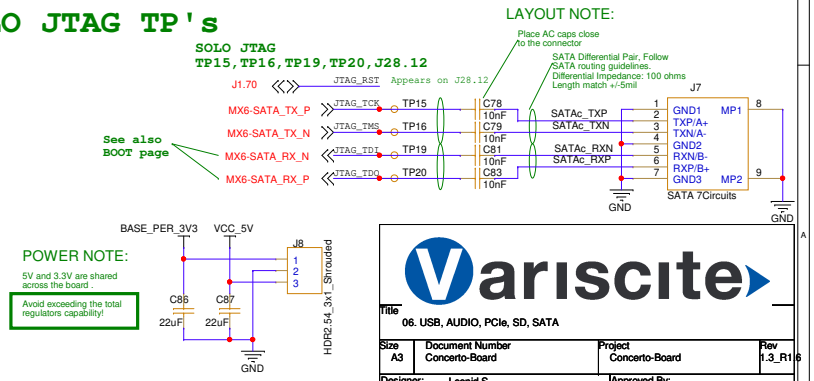
USB HOST Type-A



MX6/SOLO/MX8X PCIe



MX6 SATA+PWR
SOLO JTAG TP's

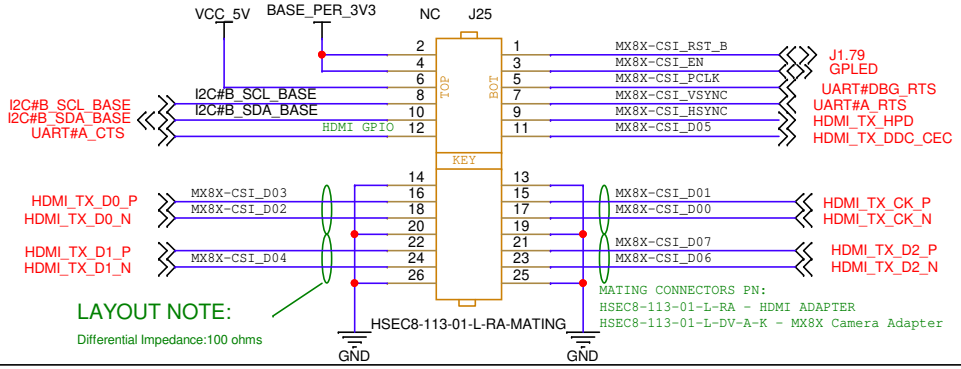


Variscite

Title: 06. USB, AUDIO, PCIe, SD, SATA			
Size: A3	Document Number: Concerto-Board	Project: Concerto-Board	Rev: 1.3_R1.6
Designer: Leonid S.		Approved By:	
Date: Sunday, August 27, 2023		Sheet 6 of 10	

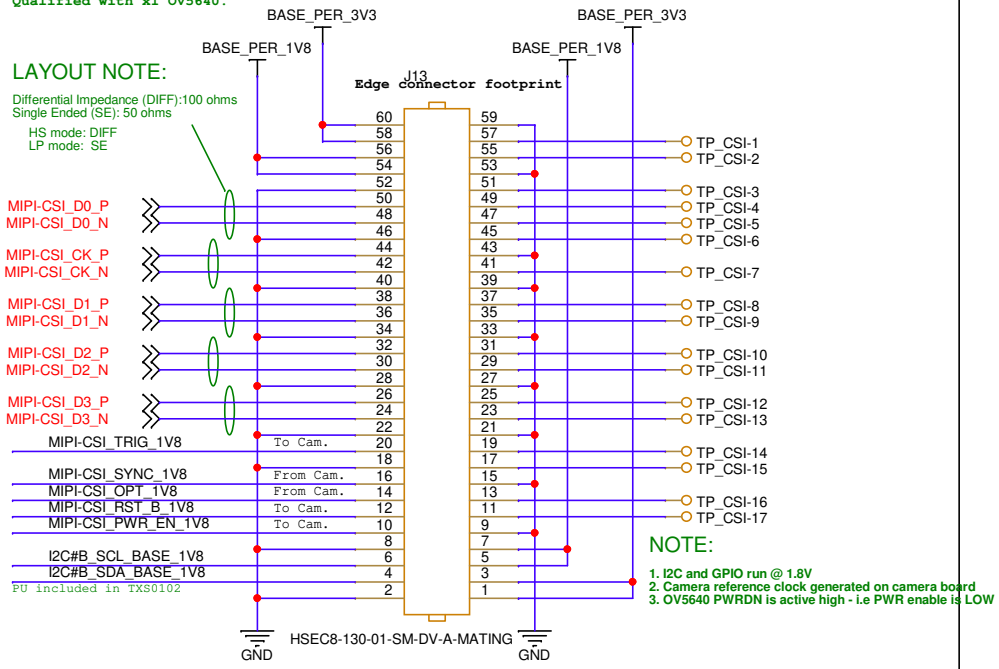
07. HDMI, MIPI-CSI, CSI

MX6/SOLO HDMI MX8X CSI

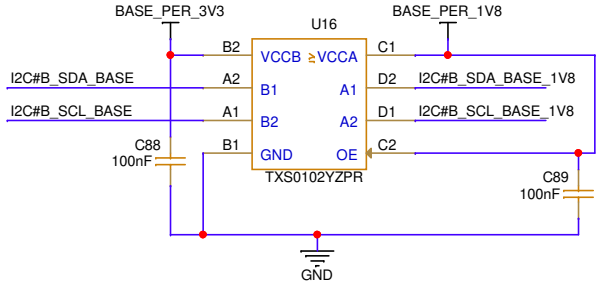


MX6/SOLO MIPI-CSI

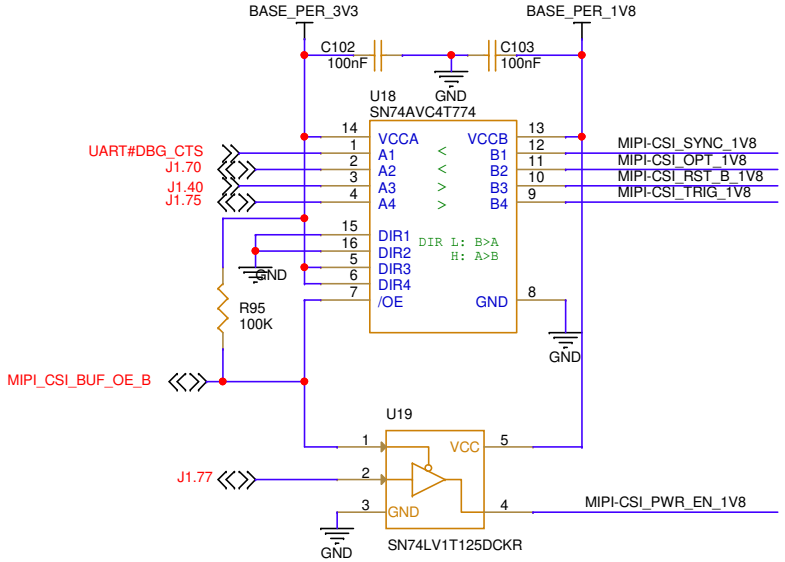
Connects to Variscite Custom MIPI-CSI2 Camera Board
Qualified with x1 OV5640.



I2C Level Translator



MX6/SOLO CAMERA BUFFERS



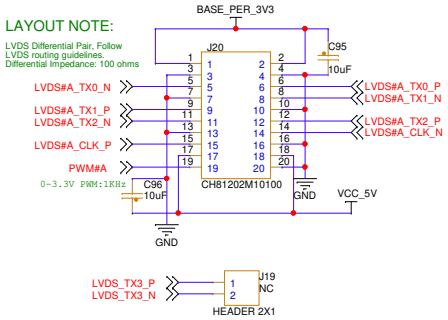
Variscite

Title: 07. HDMI, MIPI-CSI, CSI			
Size: A4	Document Number: Concerto-Board	Project: Concerto-Board	Rev: 1.3_R1.6
Designer: Leonid S.		Approved By:	
Date: Sunday, August 27, 2023		Sheet 7 of 10	

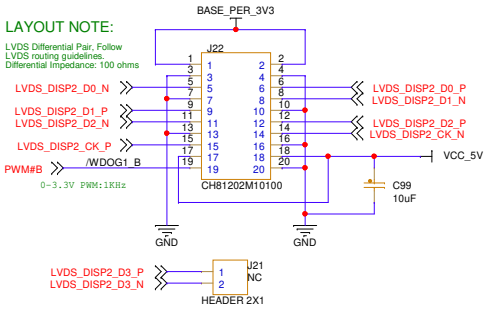
08. Display,Touch, Headers

DISPLAY

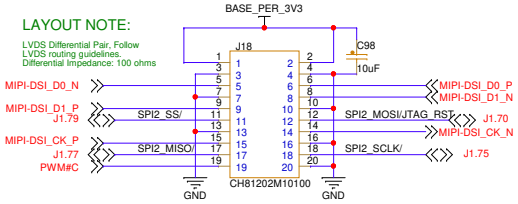
LVDS_DISP#A



LVDS_DISP2 6UL - NA

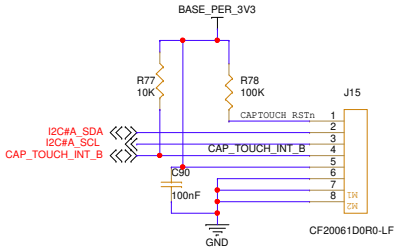


MIPI-DSI (MX6/SOLO)
SPI2 (6UL)
QSPI0B (MX8X)

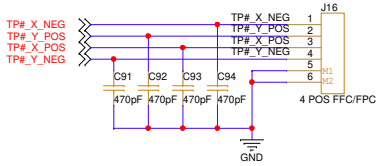


TOUCH

CAPACITIVE TOUCH

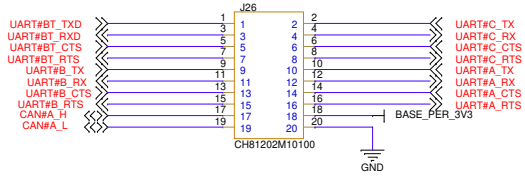


RESISTIVE TOUCH

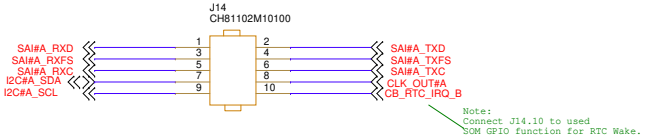


HEADERS

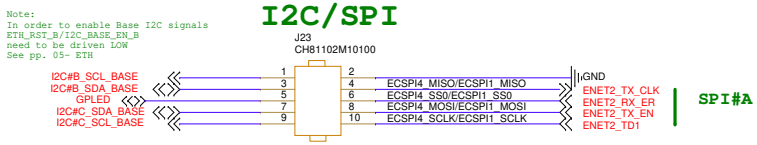
UART/ESAI/CAN



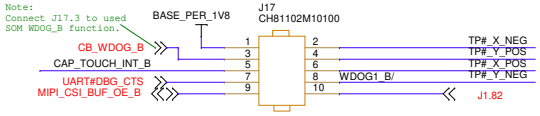
I2C/SAI



I2C/SPI



ANALOG



Variscite

Title: 08. Display,Touch, Headers			
Size: A3	Document Number: Concerto-Board	Project: Concerto-Board	Rev: 1.3_R1.6
Designer: Leonid S.		Approved By:	
Date: Sunday, August 27, 2023		Sheet 8 of 10	

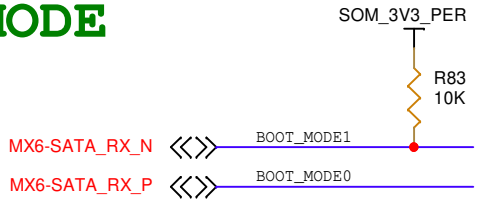
09. BOOT, Buttons, LEDs

6UL BOOT MODE

NOTE:

BOOT_MODE1 - Place PU close to SATA line to minimize stub
- Clean GND under R83 pad

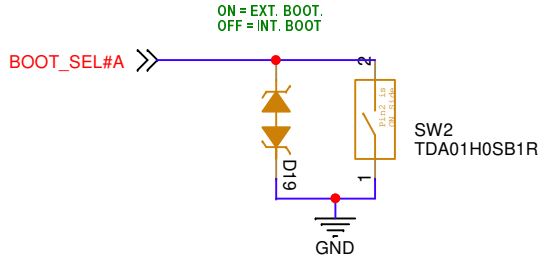
BOOT_MODE0 - Avoid driving High during boot/ PD on SOM



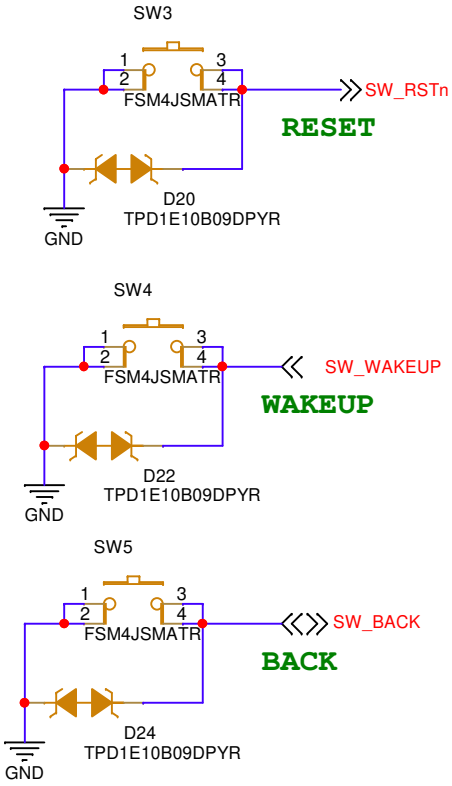
All LCDIF_D[0..23] pins should not be driven during boot to undesired value.

Note: For full LCDIF boot values see datasheet of allowed values per pin

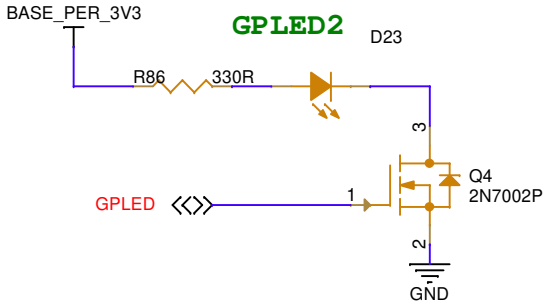
BOOT SEL



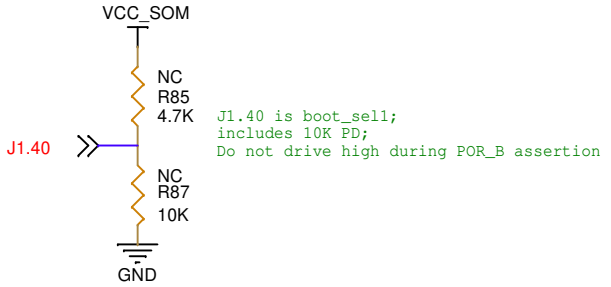
BUTTONS



LEDS



SOLO BOOT_CFG

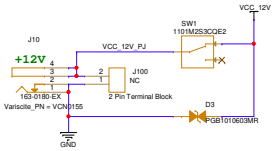


Variscite

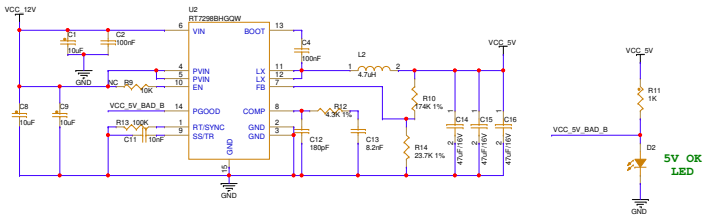
Title: 09. BOOT, Buttons, LEDs			
Size: A	Document Number:	Project:	Rev: 1.3_R16
Designer: Leonid S.		Approved By:	
Date: Sunday, August 27, 2023		Sheet 9 of 10	

10. Power, RTC, BoardID, Reset, Debug

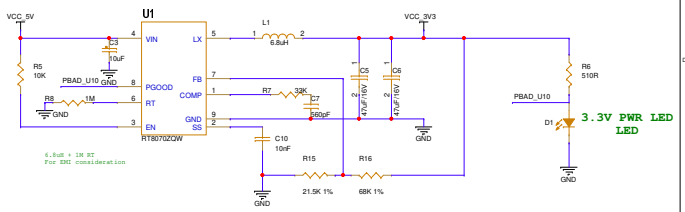
12V POWER JACK & ON/OFF Switch



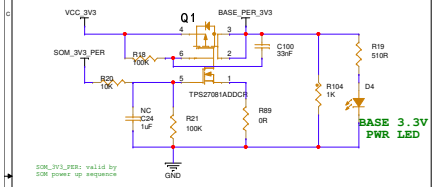
12V TO 5V/6A



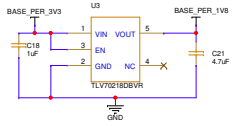
3.3V/4A FROM 5V



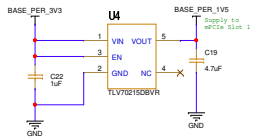
3.3V BASE



1.8V/0.3A BASE



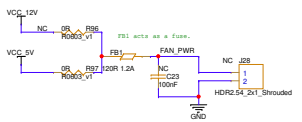
1.5V/0.3A BASE



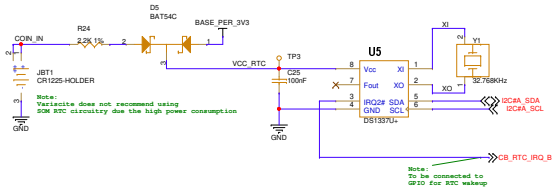
SOM PWR

CURRENT MEASUREMENT

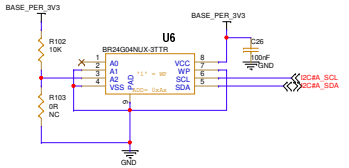
Optional FAN



RTC BATTERY

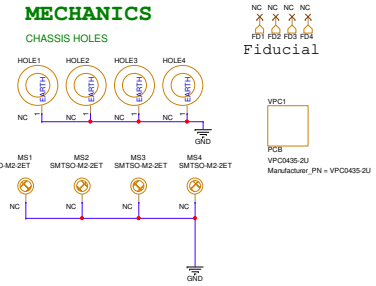


BOARD ID

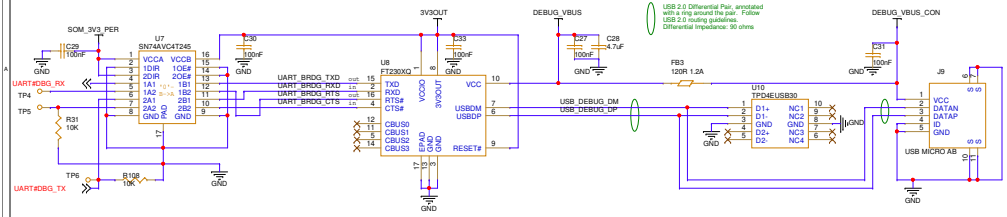


MECHANICS

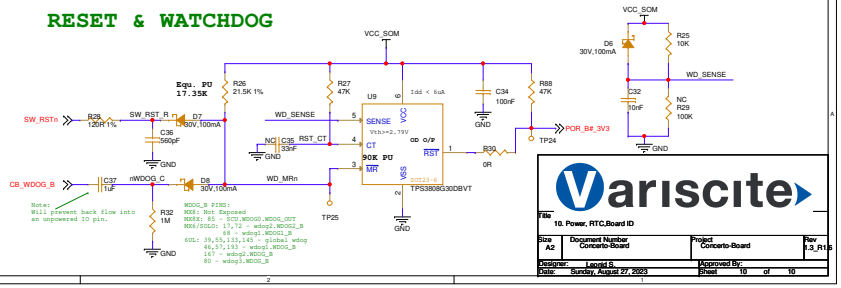
CHASSIS HOLES



DEBUG UART USB BRIDGE



RESET & WATCHDOG



Variscite

Title: 10. Power, RTC,Board ID			
Size: A2	Document Number: Concerto-Board	Project: Concerto-Board	Rev: 1.3_R1.0
Designer: Lavoid S.		Approved By:	
Date: Sunday, August 27, 2023		Sheet 10 of 10	