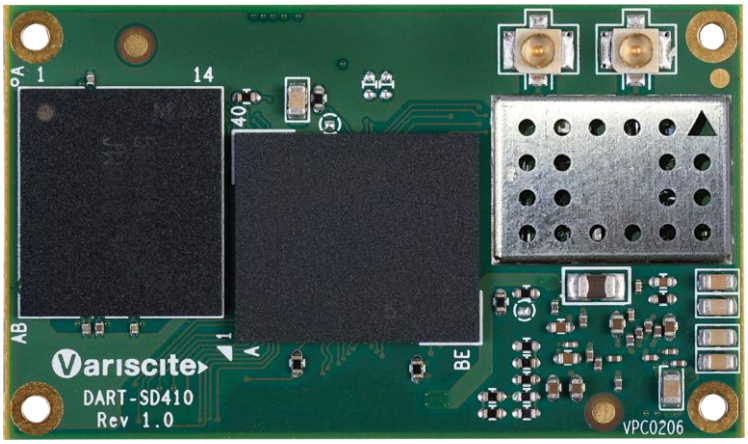
VARISCITE LTD.

DART-SD410 v1.01 Datasheet

Snapdragon™ 410 - based System-on-Module



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DART-SD410 Datasheet

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Document Revision History

Revision	Date	Notes
1.0	13/01/2016	Initial
1.1	04/06/2017	Power consumption data added Heat spreading section added
1.2	05/06/2017	Suspend current added
1.3	27/09/2017	Mounting holes dimensions added
1.4	25/07/2018	Updated section 9, added Reliability Prediction data
1.5	28/08/2018	Board thickness information added Dissipation pad dimensions added

1. Overview

1.1. General Information

The DART-SD410 is a high performance System-on-Module. It provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics and video capabilities, as well as high-processing power. Compact, cost effective and with low power consumption, the DART-SD410 is in ideal choice for a high end products.

Supporting products:

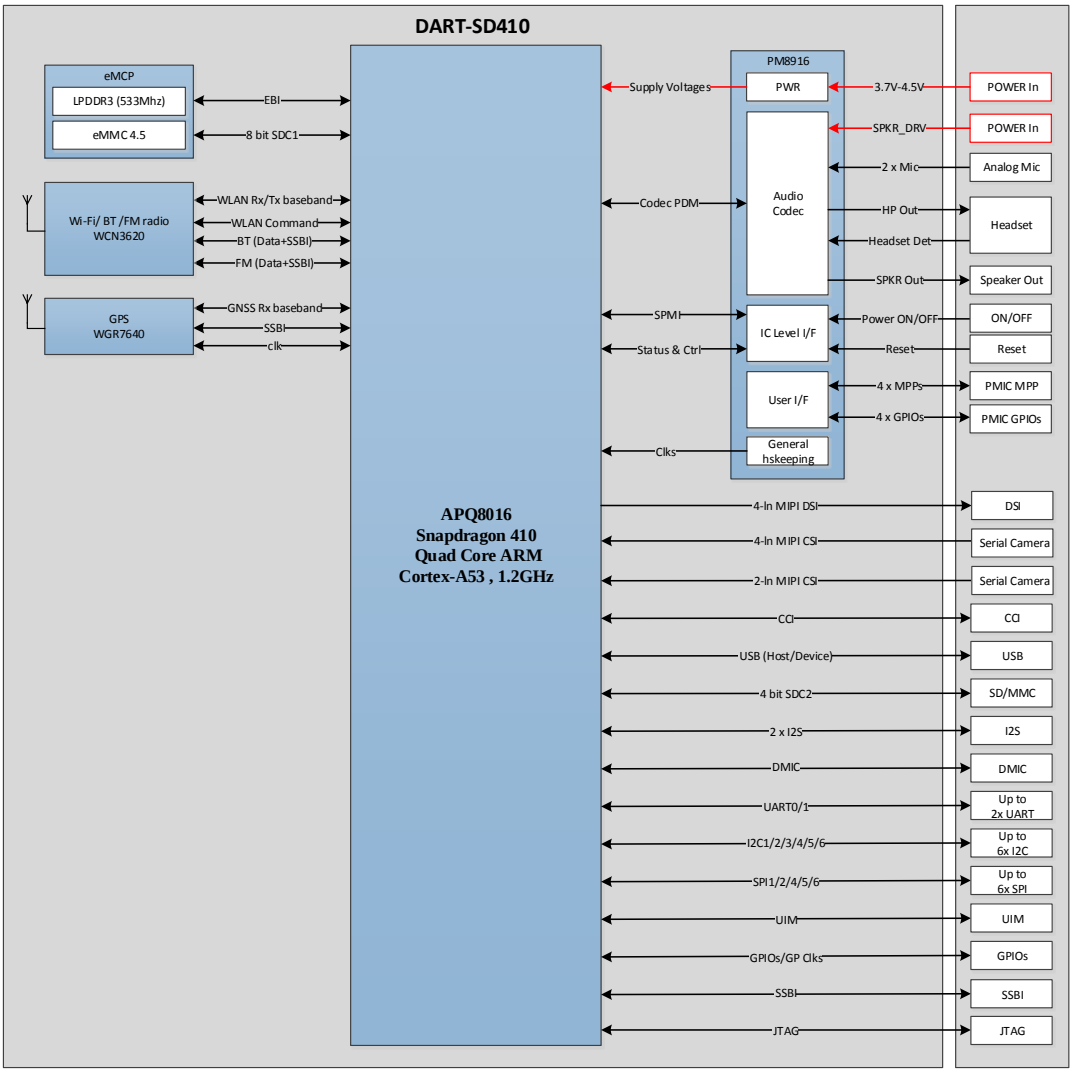
- VAR-SD410CustomBoard – evaluation board
  - ✓ Carrier-Board, compatible with DART-SD410
  - ✓ Schematics
- Dual CSI Camera extension board
- O.S support
  - ✓ Linux BSP
  - ✓ Android
  - ✓ Windows 10 (coming soon)

Contact Variscite support services for further information: mailto:support@variscite.com.

1.2. Feature Summary

- Qualcomm Snapdragon 410 Quad Core ARM® Cortex™-A53, 64 bit, 1.2 GHz
- Memory: up to 16GB eMMC and 2GB LPDDR3 (32-bit up to 533MHz)
- Display: 1 x MIPI-DSI 4-lane - HD (1280 x 720) 60 fps; 16/18/24 bpp RGB
- Camera: 2 x MIPI-CSI, 4-lane up to 13MP and 2-lane up to 8MP
- Wi-Fi/BT/FM Connectivity IC with single band 2.4GHz 802.11 b/g/n, Bluetooth 4.0/BLE and backward BT2.1+EDR / BT3.0, Worldwide FM radio
- GNSS receiver for GPS, BeiDou and GLONASS or Galileo operation
- 1 x USB2.0 Host/Device
- 1 x SD/MMC
- Serial interfaces (SPI, I2C, UART, I2S, UIM)
- JTAG
- 2 x Microphone In, Stereo headphones out, Speaker Out
- Digital microphone
- Single 3.7V-4.5V power supply
- 2 x 90 pin Board to Board Connectors
- Small size: 25mm x 43mm x 4mm

1.3. Block Diagram



2. Main Hardware Components

This section summarizes the main hardware building blocks of the DART-SD410

2.1. APQ8016

2.1.1. Overview

Embedded computing devices continue to integrate more and increasingly complex functions, and support more functionality while maintaining performance, board space, and cost.
These demands are met by the APQ8016 (Figure 1-1) – with its ARM Cortex-A53 application Processors – which further expand mass-market chipset capabilities by making rich multimedia features accessible to more consumers worldwide.

The APQ8016 has a high level of integration that reduces the bill-of-material (BOM), which Delivers board-area savings. The cost and time-to-market advantages of this IC will help drive adoption in mass markets around the world.

Wireless products based on the APQ8016 chipset may include:

- Music player-enabled devices and applications
- Cameras
- Devices with gaming, streaming video, and video conferencing features
- GPS, GLONASS, and BeiDou for global location-based service.
- Wireless connectivity–Bluetooth, WLAN, and FM receiver (with WCN3620)

The APQ8016 benefits are applied to each of these product types and include:

- Higher integration to reduce PCB surface area, time-to-market, and BOM costs while adding capabilities and processing power
- Integrated application processors and hardware cores to eliminate multimedia coprocessors, and to provide superior image quality and resolution for devices while extending application times
    - Higher computing power for high-end applications, and DC power savings for longer run times
- Position location and navigation systems supported through the WGR7640 global navigation satellite system (GNSS) receiver
    - The APQ8016 Chipset supports Gen 8C operation
    - Standalone GPS, GLONASS, and COMPASS
    - 1 Hz tracking
    - Small, power- and thermal-efficient WGR7640 packaging
- A single platform providing dedicated support for all market-leading codecs and other multimedia formats to support deployments around the world
- DC power reduction using innovative techniques
- Support for the latest, most popular operating systems

2.1.2. APQ8016 Functional Block Diagram

The APQ8016 chipset and system software solution supports the Convergence Platform for Applications by leveraging the years of systems expertise and field experience with GNSS Technologies. Since the APQ8016 includes so many diverse functions, its operation is more easily understood by considering major functional blocks individually. Therefore, the APQ8016 document set is organized according to the following block partitioning:

- Architecture and baseband processors
- Memory support
- Air interfaces
- Multimedia
- Connectivity
- Internal functions
- Interfaces to other functions (including the other ICs within the chipset)
- Configurable general-purpose input/output (GPIO) ports

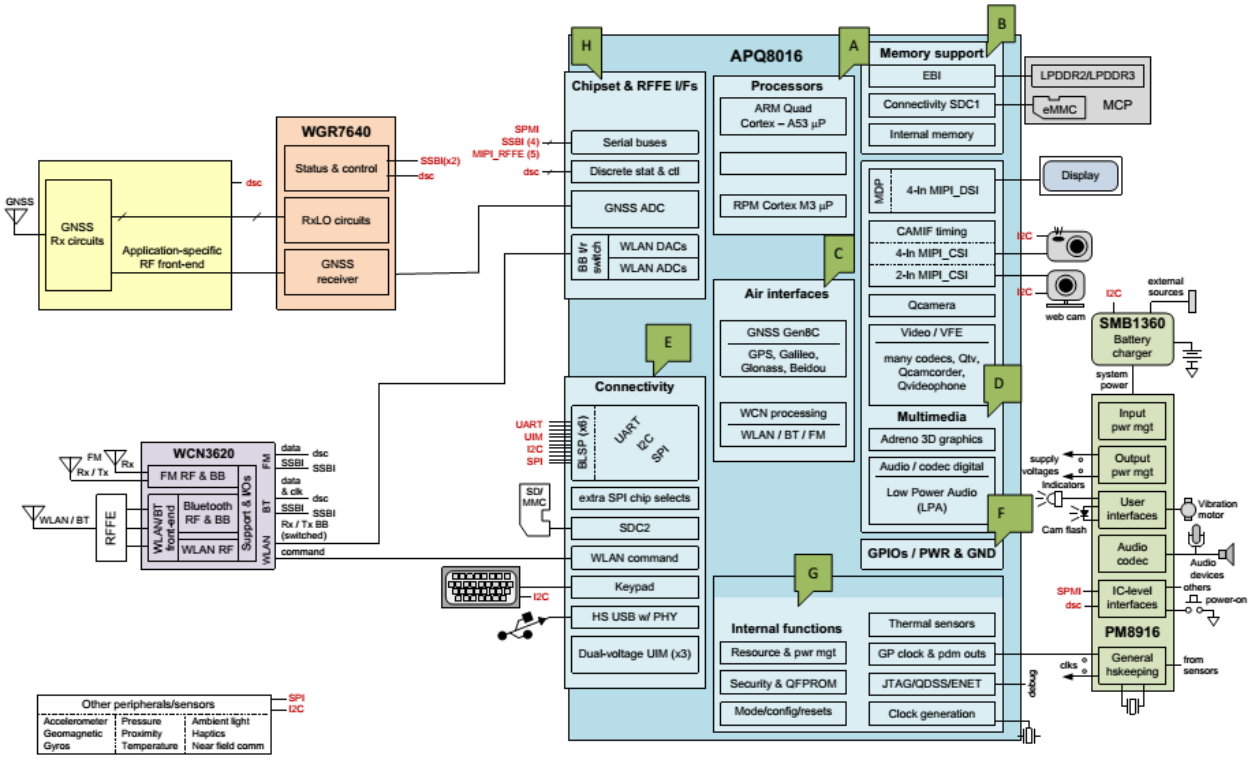


Figure 1-1 APQ8016 functional block diagram and example application

The APQ8016 features are summarized in the following table:

Feature	APQ8016 capability
A ***Processors***	
	ARM Cortex-A53 microprocessor cores up to 1.2 GHz ▪ 64-bit processor ▪ Quad core, 512 kB L2 cache ▪ Primary boot processor
RPM system	▪ Cortex M3: Modem power manager (MPM) ▪ MPM coordinates shutdown/wakeup, clock rates, and VDDs
B ***Memory support***	
System memory via EBI	Non PoP LPDDR2, LPDDR3 SDRAM; 32-bit wide; up to 533 MHz
Graphics internal memory	128 kB unified SRAM pool on-chip memory (GMEM)
External memory via SDC1	eMMC v4.5/SD flash devices
C ***RF Support***	
Air interfaces ▪ WLAN/BT/FM	▪ Yes – all (with WCN3620)
GNSS – Qualcomm IZat™ location engine	Gen 8C: Support for 3 bands concurrently: ▪ GPS, BeiDou, and Glonass or ▪ GPS, BeiDou, and Galileo
D ***Multimedia***	
Display interfaces ▪ MIPI_DSI ▪ General display features	▪ HD (1280 x 720) 60 fps; 16/18/24 bpp RGB ▪ MIPI DSI 4-lane ▪ Wi-Fi display – 720p 30/1080p 30 ▪ FHD + 720p external wireless display
Camera interfaces ▪ Number of CSIs	▪ Qcamera ▪ Two; 1.5 Gbps per lane
▪ Primary (CSI0) ▪ Secondary (CSI1) ▪ Configurations supported ▪ General camera features	▪ 4-lane; supports CMOS and CCD sensors ▪ Up to 13 MP sensors ▪ 2-lane MIPI CSI – webcam support up to 8 MP sensors ▪ Pixel manipulations, camera modes, image effects, and post-processing techniques, including defective pixel correction ▪ I2C control
Mobile display processor	MDP for display processing
Video applications performance ▪ Encode ▪ Decode	▪ 720p 30 fps (H.264 Baseline/MPEG-4) ▪ 30 fps 1080p (MPEG-4/H.264/VP8/H.263) ▪ WFD 720p @ 30 fps ▪ 30 fps 1080p (MPEG-4/H.264/H.263/DivX/MPEG2/VC1/Soreson/VP8) ▪ WFD 1080p @ 30 fps
Graphics	Adreno 306; up to 400 MHz 3D graphics accelerator
Audio	

▪ Low-power audio ▪ Voice codec support ▪ Audio codec support ▪ Enhanced audio ▪ Synthesizer	Low power audio for mp3 and AAC playback; surround sound; ▪ Versatile – many audio playback and voice modes; encoders for audio and FM ▪ recording; many concurrency modes ▪ G711; Raw PCM; QCELP; EVRC, -B, -WB; AMR-NB, -WB; GSMEFR, ▪ -FR, -HR ▪ MP3; AAC, +, eAAC; AMR-NB, -WB, G.711, WMA 9/10 Pro ▪ Dolby Digital Plus and DTS-HD surround sound ▪ Fluence™ Noise Cancellation ▪ QAudioFX/Qconcert/QEnsemble ▪ 128-voice polyphony wavetable
Web technologies	▪ V8 JavaScript Engine optimizations ▪ Webkit browser JPEG hardware decode acceleration ▪ Networking Stack IP and HTTP tuning ▪ Flash 10.x and video processor decode optimization
E ***Connectivity***	
BLSP ports ▪ UART ▪ I2C ▪ SPI (master only)	6, 4-bits each; multiplexed serial interface functions ▪ Yes – up to 4 Mbps ▪ Yes – cameras, sensors, SMB, etc. ▪ Yes – cameras, sensors, etc.
UIM	Three ports – dual voltage (1.8 V/2.85 V)
USB	One USB 2.0 high-speed
Secure digital interfaces	▪ Up to two ports, both dual-voltage ▪ One 8-bit and one 4-bit ▪ SD 3.0; SD/MMC card; eMMC v4.5
Wireless connectivity ▪ WLAN ▪ Bluetooth ▪ FM radio	▪ With WCN3620 ▪ 802.11 a/b/g/n ▪ BT 4.0 LE and earlier ▪ Rx
Touch screen support	Capacitive panels via external IC (I2C, SPI, and interrupts)
Audio interfaces ▪ DMIC ▪ MI2S ▪ CDC PDM port	 ▪ One port for digital microphone application ▪ Up to two ports (primary and secondary ports) ▪ Interface between PM8916 and APQ8016 for audio application
F ***Configurable GPIOs***	
Number of GPIO ports	122 GPIOs – GPIO_0 to GPIO_121
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	The logic block used for configuring different IOs and interfaces for the desired functionality and pad attributes
G ***Internal functions***	
PLLs and clocks	▪ Multiple clock regimes; watchdog and sleep timers ▪ 19.2 MHz CXO master clock input ▪ General-purpose outputs: M/N counter, PDM
Resource and power manager	▪ Fundamental to power management ▪ Key blocks: RPM core, Cortex M3, security controller, MPM ▪ Improved efficiency via clock control, split-rail power collapse and voltage scaling; several low-power sleep modes

Debug	JTAG, QDSS
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset and RF front-end (RFFE) interface features	
RFICs ▪ GNSS baseband data ▪ Status and control	▪ WGR7640 ▪ Rx analog interface ▪ SSBIs and discrete signals as needed via GPIOs
Power management	▪ PM8916 ▪ 2-line SPMI; dedicated clock and reset lines; plus other GPIOs as needed
WCN wireless connectivity ▪ WLAN baseband data ▪ WLAN status and control ▪ Bluetooth ▪ FM radio	WCN3620 ▪ Multiplexed Rx/Tx analog interface ▪ Proprietary 5-line interface ▪ 2-line data interface plus SSBI ▪ 1-line data interface plus SSBI
QCA near field communicator	I2C plus other GPIOs as needed

2.2. Memory

2.2.1. RAM

The DART-SD410 is available with 1GB and 2GB of LPDDR3 memory.

2.2.2. Non-volatile Storage Memory

The DART-SD410 is available with 8GB and 16GB eMMC storage.

2.3. PMIC + Audio Codec

Qualcomm's PM8916 device is a Power Management Integrated circuit (PMIC) with an integrated Audio Codec, designed specifically for use with Qualcomm's MSM8x16 application processors. The PM8916 regulates all power rails required on SOM from a single 3.7 V-4.5V power supply.

The PM8916 device includes many diverse functions, and can be organized by the device functionality as follows:

- Input power management
- Output power management
- General housekeeping
- User interfaces
- IC interfaces
- Configurable pins – either multipurpose pins (MPPs) or general-purpose input/output. (GPIOs) – that can be configured to function within some of the other categories

2.4. Wi-Fi + BT + FM

The DART-SD410 contains Qualcomm's The WCN3620 IC which integrates three different connectivity technologies into a single device:

- Wireless local area network (WLAN) compliant with the IEEE 802.11b/g/n specification
- Bluetooth (BT) compliant with the BT specification version 4.0 (BR/EDR+BLE)
- Worldwide FM radio, with Rx modes supporting the Radio Data System (RDS) for Europe and the Radio Broadcast Data System (RBDS) for the USA

2.5. GPS

The DART-SD410 contains Qualcomm's WGR7640 a GNSS receiver for GPS, GLONASS, and COMPASS operation.

3. External Connectors

The DART-SD410 exposes two 90 pin Board to Board low profile connectors.
The recommended mating connectors for Custom board interfacing are:

DF40C-90DS-0.4V(51)

Pin#:
Pin number on the connector

Pin Name:
Default DART-SD410 pin name

Type:
Pin type & direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Pin Group:
Pin functionality group

APQ8016 Ball:
Ball number

Mode (Tables 3.2 & 3.4):
Pin mux mode option

3.1. DART-SD410 Connector Pin-out

J1					
Pin #	**Pin Name**	**Type**	**Description**	**GPIO**	**Ball**
J1.1	VPH_PWR	POWER	Main power supply, 3.7V-4.5V DC-IN		
J1.2	VPH_PWR	POWER	Main power supply, 3.7V-4.5V DC-IN		
J1.3	VPH_PWR	POWER	Main power supply, 3.7V-4.5V DC-IN		
J1.4	VPH_PWR	POWER	Main power supply, 3.7V-4.5V DC-IN		
J1.5	VPH_PWR	POWER	Main power supply, 3.7V-4.5V DC-IN		
J1.6	VPH_PWR	POWER	Main power supply, 3.7V-4.5V DC-IN		
J1.7	VPH_PWR	POWER	Main power supply, 3.7V-4.5V DC-IN		
J1.8	VPH_PWR	POWER	Main power supply, 3.7V-4.5V DC-IN		
J1.9	CDC_VDD_SPKDRV	POWER	+3.7/+5V class-D speaker amplifier supply input		PM8916.G14
J1.10	DGND	POWER	Digital GND		
J1.11	CDC_VDD_SPKDRV	POWER	+3.7/+5V class-D speaker amplifier supply input		PM8916.G14
J1.12	MIPI_DSI0_DATA3_M	DS	MIPI DSI interface 0 lane 3 negative		AL2
J1.13	SPKR_OUT_P	AO	Class-D speaker amp + output		PM8916.F14
J1.14	MIPI_DSI0_DATA3_P	DS	MIPI DSI interface 0 lane 3 positive		AK1
J1.15	SPKR_OUT_P	AO	Class-D speaker amp + output		PM8916.F14
J1.16	MIPI_DSI0_DATA2_M	DS	MIPI DSI interface 0 lane 2 negative		AH3
J1.17	SPKR_OUT_M	AO	Class-D speaker amp – output		PM8916.E12, PM8916.E13
J1.18	MIPI_DSI0_DATA2_P	DS	MIPI DSI interface 0 lane 2 positive		AG4
J1.19	SPKR_OUT_M	AO	Class-D speaker amp - output		PM8916.E12, PM8916.E13
J1.20	MIPI_DSI0_DATA1_M	DS	MIPI DSI interface 0 lane 1 negative		AF3
J1.21	USB_VBUS	POWER	USB VBUS for OTG		
J1.22	MIPI_DSI0_DATA1_P	DS	MIPI DSI interface 0 lane 1 positive		AE4
J1.23	CDC_HPH_L	AO	Headphone left channel output		PM8916.F12
J1.24	MIPI_DSI0_CLK_M	DS	MIPI DSI interface 0 clock negative		AH1
J1.25	CDC_HPH_R	AO	Headphone right channel output		PM8916.G12
J1.26	MIPI_DSI0_CLK_P	DS	MIPI DSI interface 0 clock positive		AG2
J1.27	CDC_HPH_REF	AI	Headphone ground sensing		PM8916.G11
J1.28	MIPI_DSI0_DATA0_M	DS	MIPI DSI interface 0 lane 0 negative		AF1
J1.29	CDC_HS_DET	AI	Headset detection		PM8916.K14
J1.30	MIPI_DSI0_DATA0_P	DS	MIPI DSI interface 0 lane 0 positive		AE2
J1.31	DGND	POWER	Digital GND		
J1.32	DGND	POWER	Digital GND		
J1.33	CDC_MIC_BIAS2	AO	Microphone #2 bias		PM8916.J11
J1.34	MIPI_CSI1_CLK_M	DS	MIPI CSI interface 1 clock negative		AB5
J1.35	CDC_MIC_BIAS1	AO	Microphone #1 bias		PM8916.L12

J1					
Pin #	**Pin Name**	**Type**	**Description**	**GPIO**	**Ball**
J1.36	MIPI_CSI1_CLK_P	DS	MIPI CSI interface 1 clock positive		AB3
J1.37	DGND	POWER	Digital GND		
J1.38	MIPI_CSI1_DATA1_M	DS	MIPI CSI interface 1 lane 1 negative		AC2
J1.39	CDC_MIC1_P	AI	Main microphone		PM8916.K13
J1.40	MIPI_CSI1_DATA1_P	DS	MIPI CSI interface 1 lane 1 positive		AB1
J1.41	GND_CFILT	POWER	Ground reference for PMIC bias		PM8916.J13
J1.42	MIPI_CSI1_DATA0_M	DS	MIPI CSI interface 1 lane 0 negative		AA2
J1.43	CDC_MIC2_P	AI	Headset microphone		PM8916.K11
J1.44	MIPI_CSI1_DATA0_P	DS	MIPI CSI interface 1 lane 0 positive		Y1
J1.45	GND_CFILT	POWER	Ground reference for PMIC bias		PM8916.J13
J1.46	DGND	POWER	Digital GND		
J1.47	DGND	POWER	Digital GND		
J1.48	MIPI_CSI0_DATA2_M	DS	MIPI CSI interface 0 lane 2 negative		W2
J1.49	SDC2_DATA_3	IO	External SD card Data 3 line		P7
J1.50	MIPI_CSI0_DATA2_P	DS	MIPI CSI interface 0 lane 2 positive		V1
J1.51	SDC2_DATA_2	IO	External SD card Data 2 line		T7
J1.52	MIPI_CSI0_DATA3_M	DS	MIPI CSI interface 0 lane 3 negative		AA6
J1.53	SDC2_DATA_0	IO	External SD card Data 0 line		P3
J1.54	MIPI_CSI0_DATA3_P	DS	MIPI CSI interface 0 lane 3 positive		Y5
J1.55	SDC2_DATA_1	IO	External SD card Data 1 line		R6
J1.56	MIPI_CSI0_CLK_M	DS	MIPI CSI interface 0 clock negative		W6
J1.57	SDC2_CMD	IO	External SD card Command line		N6
J1.58	MIPI_CSI0_CLK_P	DS	MIPI CSI interface 0 clock positive		V5
J1.59	SDC2_CLK	O	External SD card Clock output		R4
J1.60	MIPI_CSI0_DATA1_M	DS	MIPI CSI interface 0 lane 1 negative		U2
J1.61	DGND	POWER	Digital GND		
J1.62	MIPI_CSI0_DATA1_P	DS	MIPI CSI interface 0 lane 1 positive		T1
J1.63	SPI0_CLK	IO	SPI0 clock (BLSP5_0)	GPIO_19	J4
J1.64	MIPI_CSI0_DATA0_M	DS	MIPI CSI interface 0 lane 0 negative		U4
J1.65	SPI0_MOSI	IO	SPI0 MOSI (BLSP5_3)	GPIO_16	K7
J1.66	MIPI_CSI0_DATA0_P	DS	MIPI CSI interface 0 lane 0 positive		U6
J1.67	SPI0_CS_N	IO	SPI0 Chip Select (BLSP5_1)	GPIO_18	J6
J1.68	DGND	POWER	Digital GND		
J1.69	SPI0_MISO	IO	SPI0 MISO (BLSP5_2)	GPIO_17	G6
J1.70	SPI1_CS_N	IO	SPI1 Chip Select (BLSP3_1)	GPIO_10	H1
J1.71	DGND	POWER	Digital GND		
J1.72	SPI1_MISO	IO	SPI1 MISO (BLSP3_2)	GPIO_9	G2
J1.73	I2C1_SCL	IO	I2C1 Clock (BLSP6_3)	GPIO_23	BA2

J1					
Pin #	**Pin Name**	**Type**	**Description**	**GPIO**	**Ball**
J1.74	SPI1_CLK	IO	SPI1 Clock (BLSP3_0)	GPIO_11	E2
J1.75	I2C1_SDA	IO	I2C1 Data (BLSP6_3)	GPIO_22	AV7
J1.76	SPI1_MOSI	IO	SPI1 MOSI (BLSP3_3)	GPIO_8	H5
J1.77	I2C0_SDA	IO	I2C0 Data (BLSP2_1)	GPIO_6	AY3
J1.78	DGND	POWER	Digital GND		
J1.79	I2C0_SCL	IO	I2C0 Clock (BLSP2_0)	GPIO_7	AV3
J1.80	CSI1_MCLK	IO	Camera master clock 1	GPIO_27	C2
J1.81	DGND	POWER	Digital GND		
J1.82	GPIO_28	IO	General purpose IO	GPIO_28	F1
J1.83	UART1_TX	IO	UART1 Transmit (BLSP2_3)	GPIO_4	AT9
J1.84	CSI0_MCLK	IO	Camera master clock 0	GPIO_26	H3
J1.85	UART1_RX	IO	UART1 Receive (BLSP2_2)	GPIO_5	AY1
J1.86	DGND	POWER	Digital GND		
J1.87	FORCED_USB_BOOT	IO	Force USB boot control	GPIO_37	E4
J1.88	I2C2_SCL	IO	Camera control interface I2C Clock	GPIO_30	F3
J1.89	APQ_RESIN_N	I	System Reset		
J1.90	I2C2_SDA	IO	Camera control interface I2C Data	GPIO_29	B3

J2					
Pin #	**Pin Name**	**Type**	**Description**	**GPIO**	**Ball**
J2.1	VREG_L11_SDC	POWER	2.95V power supply output for External SD Card		PM8916.G3
J2.2	PM_MPP3	IO	PM8916 Multipurpose pin 3	PM8916 MPP_3	PM8916.J4
J2.3	VREG_L11_SDC	POWER	2.95V power supply output for External SD Card		PM8916.G3
J2.4	PM_GPIO2	IO	PM8916 GPIO_2	PM8916 GPIO_2	PM8916.H6
J2.5	DGND	POWER	Digital GND		
J2.6	PM_MPP4	IO	PMIC Configurable MPP_4	PM8916 MPP_4	PM8916.J5
J2.7	PM_RESIN_N	I	Reset In signal/ Volume, Zoom DOWN key		PM8916.C3
J2.8	PM_MPP2	IO	PM8916 Multipurpose pin 2	PM8916 MPP_2	PM8916.K4
J2.9	PHONE_ON_N	I	Power ON/OFF Signal		PM8916.K10
J2.10	PM_GPIO1	IO	PM8916 GPIO_1	PM8916 GPIO_1	PM8916.J7
J2.11	DGND	POWER	Digital GND		
J2.12	GPIO_21	IO	General purpose IO	GPIO_21	AW6
J2.13	VREG_L12_SDC	POWER	2.95V power supply output for External SD Card		PM8916.B3
J2.14	GPIO_120	IO	General purpose IO	GPIO_120	F39

J2					
Pin #	**Pin Name**	**Type**	**Description**	**GPIO**	**Ball**
J2.15	DGND	POWER	Digital GND		
J2.16	PM_GPIO3	IO	PM8916 GPIO_3	PM8916 GPIO_3	PM8916.N11
J2.17	GPIO_112	IO	General purpose IO	GPIO_112	AW36
J2.18	PM_GPIO4	IO	PM8916 GPIO_4	PM8916 GPIO_4	PM8916.L8
J2.19	GPIO_96	IO	General purpose IO	GPIO_96	BC32
J2.20	FM_RX_ANT	AI	WCN3620 FM antenna signal		WCN3620.50
J2.21	DGND	POWER	Digital GND		
J2.22	BOOT_CONFIG_1	IO	Boot configuration control bit 1	GPIO_81	BD7
J2.23	UART0_TX	IO	UART0 Transmit (BLSP1_3)	GPIO_0	BA38
J2.24	BOOT_CONFIG_0	IO	Boot configuration control bit 0	GPIO_80	BD5
J2.25	UART0_RTS_N	IO	UART0 RTS (BLSP1_0)	GPIO_3	AY37
J2.26	BOOT_CONFIG_3	IO	Boot configuration control bit 3	GPIO_83	BC40
J2.27	UART0_RX	IO	UART0 Receive (BLSP1_2)	GPIO_1	BB39
J2.28	GPIO_20	IO	General purpose IO	GPIO_20	AY7
J2.29	UART0_CTS_N	IO	UART0 CTS (BLSP1_1)	GPIO_2	AV35
J2.30	DGND	POWER	Digital GND		
J2.31	DGND	POWER	Digital GND		
J2.32	USB_HS_D_M	DS	USB HS data minus		AC40
J2.33	BOOT_CONFIG_2	IO	Boot configuration control bit 2	GPIO_82	BC38
J2.34	USB_HS_D_P	DS	USB HS data plus		AB39
J2.35	BOOT_CONFIG_5	IO	Boot configuration control bit 5	GPIO_86	BD39
J2.36	DGND	POWER	Digital GND		
J2.37	DGND	POWER	Digital GND		
J2.38	GPIO_25	IO	General purpose IO	GPIO_25	AU4
J2.39	GPIO_106	IO	General purpose IO	GPIO_106	AY39
J2.40	GPIO_24	IO	General purpose IO	GPIO_24	AT5
J2.41	GPIO_116	IO	General purpose IO	GPIO_116	AW38
J2.42	DGND	POWER	Digital GND		
J2.43	GPIO_114	IO	General purpose IO	GPIO_114	E40
J2.44	GPIO_52	IO	General purpose IO	GPIO_52	AA38
J2.45	GPIO_105	IO	General purpose IO	GPIO_105	AU36
J2.46	GPIO_49	IO	General purpose IO	GPIO_49	Y37
J2.47	GPIO_113	IO	General purpose IO	GPIO_113	D39
J2.48	GPIO_50	IO	General purpose IO	GPIO_50	AA34
J2.49	DGND	POWER	Digital GND		
J2.50	GPIO_51	IO	General purpose IO	GPIO_51	Y35
J2.51	GPIO_110	IO	General purpose IO	GPIO_110	B39

J2					
Pin #	**Pin Name**	**Type**	**Description**	**GPIO**	**Ball**
J2.52	GPIO_69	IO	General purpose IO	GPIO_69	L36
J2.53	GPIO_98	IO	General purpose IO	GPIO_98	A38
J2.54	GPIO_108	IO	General purpose IO	GPIO_108	K35
J2.55	GPIO_38	IO	General purpose IO	GPIO_38	B37
J2.56	DGND	POWER	Digital GND		
J2.57	EEPROM_WP	I	EEPROM Write protect		
J2.58	GPIO_109	IO	General purpose IO	GPIO_109	J34
J2.59	MI2S_DATA0	IO	MI2S interface #2 Data0 signal	GPIO_119	BA40
J2.60	GPIO_62	IO	General purpose IO	GPIO_62	G34
J2.61	MI2S_WS	IO	MI2S interface #2 Word Select signal	GPIO_117	AV37
J2.62	KEY_VOLP_N	IO	Volume, Zoom UP key	GPIO_107	H33
J2.63	MI2S_SCK	IO	MI2S interface #2 SCLK signal	GPIO_118	AR36
J2.64	USB_HS_ID	IO	USB ID pin for host mode detection	GPIO_121	G38
J2.65	DGND	POWER	Digital GND		
J2.66	DGND	POWER	Digital GND		
J2.67	I2C3_SCL	IO	I2C3 Clock (BLSP4_0)	GPIO_15	AN36
J2.68	JTAG_SRST_N	I	JTAG reset for debug		K1
J2.69	I2C3_SDA	IO	I2C3 Data (BLSP4_1)	GPIO_14	AN40
J2.70	JTAG_TMS	I	JTAG mode-select input		L2
J2.71	BBCLK2	O	Baseband low power XO output 2		PM8916.F3
J2.72	JTAG_TCK	I	JTAG clock input		M1
J2.73	GPIO_12	IO	General purpose IO	GPIO_12	AM39
J2.74	JTAG_TDI	I	JTAG data input		M3
J2.75	GPIO_13	IO	General purpose IO	GPIO_13	AM35
J2.76	JTAG_TRST_N	I	JTAG reset		K3
J2.77	DGND	POWER	Digital GND		
J2.78	JTAG_TDO	O	JTAG data output		J2
J2.79	GPIO_115	IO	General purpose IO	GPIO_115	E38
J2.80	JTAG_PS_HOLD	I	PMIC Power supply hold control input		PM8916.G5
J2.81	GPIO_97	IO	General purpose IO	GPIO_97	C38
J2.82	DGND	POWER	Digital GND		
J2.83	GPIO_35	IO	General purpose IO	GPIO_35	A4
J2.84	GPIO_33	IO	General purpose IO	GPIO_33	G4
J2.85	GPIO_31	IO	General purpose IO	GPIO_31	D3
J2.86	GPIO_34	IO	General purpose IO	GPIO_34	F5
J2.87	GPIO_32	IO	General purpose IO	GPIO_32	D1
J2.88	GPIO_36	IO	General purpose IO	GPIO_36	C4
J2.89	DGND	POWER	Digital GND		

J2					
Pin #	**Pin Name**	**Type**	**Description**	**GPIO**	**Ball**
J2.90	DGND	POWER	Digital GND		

3.2. Pin Mux

The table below summarizes the additional available functionality for each pin in the two board to board connectors.

J1				
Pin #	**Ball**	**Ball name**	**Configurable function**	**Functional description**
J1.63	J4	GPIO_19	BLSP5_0	Configurable I/O BLSP #5, bit 0; SPI, or I2C
J1.65	K7	GPIO_16	BLSP5_3 BLSP1_SPI_CS2_N	Configurable I/O BLSP #5, bit 3; SPI, or I2C Chip select 2 for SPI on BLSP1
J1.67	J6	GPIO_18	BLSP5_1	Configurable I/O BLSP #5, bit 1; SPI, or I2C
J1.69	G6	GPIO_17	BLSP5_2 BLSP2_SPI_CS2_N	Configurable I/O BLSP #5, bit 2; SPI, or I2C Chip select 2 for SPI on BLSP1
J1.70	H1	GPIO_10	BLSP3_1	Configurable I/O BLSP #3, bit 1; SPI, or I2C
J1.72	G2	GPIO_9	BLSP3_2	Configurable I/O BLSP #3, bit 2; SPI or I2C
J1.73	BA2	GPIO_23	BLSP6_0	Configurable I/O BLSP #6, bit 0; SPI, or I2C
J1.74	E2	GPIO_11	BLSP3_0	Configurable I/O BLSP #3, bit 0; SPI, or I2C
J1.75	AV7	GPIO_22	BLSP6_1	Configurable I/O BLSP #6, bit 1; SPI, or I2C
J1.76	H5	GPIO_8	BLSP3_3	Configurable I/O BLSP #3, bit 3; SPI or I2C
J1.77	AY3	GPIO_6	BLSP2_1	Configurable I/O BLSP #2, bit 1; UART, SPI, or I2C
J1.79	AV3	GPIO_7	BLSP2_0	Configurable I/O BLSP #2, bit 0; UART, SPI, or I2C
J1.80	C2	GPIO_27	CAM_MCLK1	Configurable I/O Camera master clock 1
J1.82	F1	GPIO_28	CAM1_RST_N	Configurable I/O Camera 1 reset
J1.83	AT9	GPIO_4	BLSP2_3 BLSP1_SPI_CS3_N	Configurable I/O BLSP #2, bit 3; UART or SPI Chip select 3 for SPI on BLSP1
J1.84	H3	GPIO_26	CAM_MCLK0	Configurable I/O Camera master clock 0
J1.85	AY1	GPIO_5	BLSP2_2 BLSP2_SPI_CS3_N	Configurable I/O BLSP #2, bit 2; UART or SPI Chip select 3 for SPI on BLSP2
J1.87	E4	GPIO_37	BLSP3_SPI_CS2_N FORCED_USB_BOOT	Configurable I/O Chip select 2 for SPI on BLSP3 Force USB boot control
J1.88	F3	GPIO_30	CAM_I2C_SCL	Configurable I/O Camera control interface I2C 0 serial Clock
J1.90	B3	GPIO_29		Configurable I/O

J1				
Pin #	**Ball**	**Ball name**	**Configurable function**	**Functional description**
			CAM_I2C_SDA	Camera control interface I2C 0 serial data

J2				
Pin #	**Ball**	**Ball name**	**Configurable function**	**Functional description**
J2.2	PM8916.J4	MPP_3	VREF_DAC Digital I/O (optional)	Configurable MPP (AO) Reference for modem IC DAC (AO) Digital input/output usage (optional) (IO)
J2.4	PM8916.H6	GPIO_2	NFC_CLK_REQ	Configurable GPIO NFC control signal to request clock
J2.6	PM8916.J5	MPP_4	WLED_PWM Digital I/O (optional)	Configurable MPP (AO) PWM control for external WLED driver (AO) Digital input/output usage (optional) (IO)
J2.8	PM8916.K4	MPP_2	SKIN_TEMP HR_LED_SNK Digital I/O (optional)	Configurable MPP (AO) Skin temperature measurement (AI) Home row LED current sink (AI) Digital input/output usage (optional) (IO)
J2.10	PM8916.J7	GPIO_1	UIM_BATT_ALM	Configurable GPIO Battery removal alarm for UIM and UIM battery alarm input to the MSM
J2.12	AW6	GPIO_21	BLSP6_2 GP_PDM_1B	Configurable I/O BLSP #6, bit 2; SPI, or I2C General-purpose PDM output 1B, 12-bit, XO/4 clock
J2.14	F39	GPIO_120	BLSP3_SPI_CS1_N	Configurable I/O Chip select 1 for SPI on BLSP3
J2.16	PM8916.N11	GPIO_3	WTR_LDO_EN	Configurable GPIO Enable signal to power WTR with external LDO
J2.17	AW36	GPIO_112	MI2S_2_D1	Configurable I/O MI2S #2 serial data channel 1
J2.18	PM8916.L8	GPIO_4		Configurable GPIO
J2.19	BC32	GPIO_96	EXT_GNSS_LNA_EN	Configurable I/O External GNSS LNA enable
J2.22	BD7	GPIO_81	BOOT_CONFIG_1	Configurable I/O Boot configuration control bit 1
J2.23	BA38	GPIO_0	BLSP1_3 DMIC0_CLK	Configurable I/O BLSP #1, bit 3; UART or SPI Digital MIC0 clock
J2.24	BD5	GPIO_80	BOOT_CONFIG_0 (WDOG_DISABLE)	Configurable I/O Boot configuration control bit 0
J2.25	AY37	GPIO_3	BLSP1_0	Configurable I/O BLSP #1, bit 0; UART, SPI or I2C
J2.26	BC40	GPIO_83	BOOT_CONFIG_3	Configurable I/O Boot configuration control bit 3
J2.27	BB39	GPIO_1	BLSP1_2 DMIC0_DATA	Configurable I/O BLSP #1, bit 2; UART or SPI Digital MIC0 data
J2.28	AY7	GPIO_20	BLSP6_3	Configurable I/O BLSP #6, bit 3; SPI, or I2C

J2				
Pin #	**Ball**	**Ball name**	**Configurable function**	**Functional description**
			GP_PDM_0A	General-purpose PDM output 0A, 12-bit, XO/4 clock
J2.29	AV35	GPIO_2	BLSP1_1	Configurable I/O BLSP #1, bit 1; UART, SPI or I2C
J2.33	BC38	GPIO_82	BOOT_CONFIG_2	Configurable I/O Boot configuration control bit 2
J2.35	BD39	GPIO_86	BOOT_CONFIG_5	Configurable I/O Boot configuration control bit 5
J2.38	AU4	GPIO_25	DSI_RST_N GP_PDM_0B	Configurable I/O Display reset General-purpose PDM output 0B, 12-bit, XO/4 clock
J2.39	AY39	GPIO_106	SSBI_WTR1_TX	Configurable I/O SSBI 2 for RFIC 1
J2.40	AT5	GPIO_24	MDP_VSYNC_P	Configurable I/O MDP vertical sync – primary
J2.41	AW38	GPIO_116	MI2S_1_MCLK	Configurable I/O MI2S #1 master clock
J2.43	E40	GPIO_114	MI2S_1_D0	Configurable I/O MI2S #1 serial data channel 0
J2.44	AA38	GPIO_52	UIM3_PRESENT GP_PDM_1A	Configurable I/O UIM3 removal detection General-purpose PDM output 1A, 12-bit, XO/4 clock
J2.45	AU36	GPIO_105	SSBI_WTR1_RX	Configurable I/O SSBI 1 for RFIC 1
J2.46	Y37	GPIO_49	BT_DATA	Configurable I/O Bluetooth dual function: data and strobe
J2.47	D39	GPIO_113	MI2S_1_SCLK GP_PDM_2B	Configurable I/O MI2S #1 bit clock General-purpose PDM 2B output
J2.48	AA34	GPIO_50	UIM3_CLK GP_CLK_2A	Configurable I/O UIM3 clock General-purpose clock output 2A
J2.50	Y35	GPIO_51	UIM3_RST GP_CLK_3A	Configurable I/O UIM3 reset General-purpose clock output 3A
J2.51	B39	GPIO_110	BLSP1_SPI_CS1_N MI2S_1_WS GP_MN	Configurable I/O Chip select 1 for SPI on BLSP1 MI2S #1 word select (L/R) General-purpose M/N:D counter output
J2.52	L36	GPIO_69	MAG_INT BLSP3_SPI_CS3_N	Configurable I/O Magnometer interrupt Chip select 3 for SPI on BLSP3
J2.53	A38	GPIO_98	LCD_BL_EN GP_PDM_2A	Configurable I/O Display backlight enable General-purpose PDM 2A output
J2.54	K35	GPIO_108	KYPD_SNS1	Configurable I/O Keypad sense bit 1
J2.55	B37	GPIO_38	SD_CARD_DET_N CCI_TIMER2	Configurable I/O Secure digital card detection Camera control interface timer 2
J2.58	J34	GPIO_109	KYPD_SNS2	Configurable I/O Keypad sense bit 2
J2.59	BA40	GPIO_119		Configurable I/O

J2				
Pin #	**Ball**	**Ball name**	**Configurable function**	**Functional description**
			MI2S_2_D0	MI2S #2 serial data channel 0
J2.60	G34	GPIO_62	SMB_INT	Configurable I/O SMB interrupt
J2.61	AV37	GPIO_117	MI2S_2_WS	Configurable I/O MI2S #2 word select (L/R)
J2.62	H33	GPIO_107	KYPD_SNS0	Configurable I/O Keypad sense bit 0
J2.63	AR36	GPIO_118	MI2S_2_SCLK	Configurable I/O MI2S #2 bit clock
J2.64	G38	GPIO_121	BLSP2_SPI_CS1_N USB_HS_ID SD_WRITE_PROTECT1	Configurable I/O Chip select 2 for SPI on BLSP2 USB ID pin for host mode detection SD write protection
J2.67	AN36	GPIO_15	BLSP4_0	Configurable I/O BLSP #4, bit 0; SPI, or I2C
J2.69	AN40	GPIO_14	BLSP4_1	Configurable I/O BLSP #4, bit 1; SPI, or I2C
J2.73	AM39	GPIO_12	BLSP4_3 GP_CLK_2B	Configurable I/O BLSP #4, bit 3; SPI, or I2C General-purpose clock output 2B
J2.75	AM35	GPIO_13	BLSP4_2 GP_CLK_3B	Configurable I/O BLSP #4, bit 2; SPI, or I2C General-purpose clock output 3B
J2.79	E38	GPIO_115	GYRO_ACCEL_INT_N MI2S_1_D1	Configurable I/O Gyro interrupt MI2S #1 serial data channel 1
J2.81	C38	GPIO_97	LCD_DRIVER_5V_EN GP_CLK_1B BOOT_CONFIG_14	Configurable I/O 5 V display driver enable General-purpose clock output 1B Boot configuration control bit 14
J2.83	A4	GPIO_35	CAM0_RST_N	Configurable I/O Camera 0 reset
J2.84	G4	GPIO_33	CCI_ASYNC0	Configurable I/O Camera control interface async 0
J2.85	D3	GPIO_31	CCI_TIMER0 GP_CLK0	Configurable I/O Camera control interface timer 0 General-purpose clock 0
J2.86	F5	GPIO_34	CAM0_STANDBY_N	Configurable I/O Camera 0 (rear camera) standby
J2.87	D1	GPIO_32	CCI_TIMER1 GP_CLK1	Configurable I/O Camera control interface timer 1 General-purpose clock 1
J2.88	C4	GPIO_36	FLASH_LED_RESET	Configurable I/O LED Flash reset

Notes:

PM8196 MPP/GPIOs:

[1] All MPPs default to their high-Z state at power-up and must be configured after power up for their intended purposes.
All GPIOs default to 10 µA pull down at power up and must be configured after power-up for their intended purposes.

[2] Configure unused MPPs as 0 mA current sinks (high-Z) and GPIOs as digital inputs With their internal pull-downs enabled.

[3] Only even MPPs can be configured as current sink and only odd MPPs can be configured as analog output.

4. SOM's interfaces

4.1. Display Interfaces

The DART-SD410 consists the following display interfaces:

- One MIPI DSI 4-lane - HD (1280 x 720) 60 fps; 16/18/24 bpp RGB
- Wifi display – 720p 30/1080p 30
- FHD + 720p external wireless display

4.1.1. MIPI DSI

MIPI DSI signals:

Signal	Pin #	Type	Description
MIPI_DSI0_DATA3_M	J1.12	ODS	MIPI DSI interface 0 lane 3 negative
MIPI_DSI0_DATA3_P	J1.14	ODS	MIPI DSI interface 0 lane 3 positive
MIPI_DSI0_DATA2_M	J1.16	ODS	MIPI DSI interface 0 lane 2 negative
MIPI_DSI0_DATA2_P	J1.18	ODS	MIPI DSI interface 0 lane 2 positive
MIPI_DSI0_DATA1_M	J1.20	ODS	MIPI DSI interface 0 lane 1 negative
MIPI_DSI0_DATA1_P	J1.22	ODS	MIPI DSI interface 0 lane 1 positive
MIPI_DSI0_CLK_M	J1.24	ODS	MIPI DSI interface 0 clock negative
MIPI_DSI0_CLK_P	J1.26	ODS	MIPI DSI interface 0 clock positive
MIPI_DSI0_DATA0_M	J1.28	ODS	MIPI DSI interface 0 lane 0 negative
MIPI_DSI0_DATA0_P	J1.30	ODS	MIPI DSI interface 0 lane 0 positive

4.2. Camera Interfaces

The DART-SD410 exports 2 MIPI CSI camera interface ports with the following capabilities:

- 4-lane ;1.5 Gbps per lane; supporting up to 13 MP sensors
- 2-lane ;1.5 Gbps per lane; supporting up to 8 MP sensors
- Pixel manipulations, camera modes, image effects, and post-processing techniques, including defective pixel correction.
- I2C controls

4.2.1. MIPI CSI0

MIPI CSI0 signals:

Signal	Pin #	Type	Description
MIPI_CSI0_DATA2_M	J1.48	IDS	MIPI CSI interface 0 lane 2 negative
MIPI_CSI0_DATA2_P	J1.50	IDS	MIPI CSI interface 0 lane 2 positive
MIPI_CSI0_DATA3_M	J1.52	IDS	MIPI CSI interface 0 lane 3 negative
MIPI_CSI0_DATA3_P	J1.54	IDS	MIPI CSI interface 0 lane 3 positive
MIPI_CSI0_CLK_M	J1.56	IDS	MIPI CSI interface 0 clock negative
MIPI_CSI0_CLK_P	J1.58	IDS	MIPI CSI interface 0 clock positive
MIPI_CSI0_DATA1_M	J1.60	IDS	MIPI CSI interface 0 lane 1 negative
MIPI_CSI0_DATA1_P	J1.62	IDS	MIPI CSI interface 0 lane 1 positive

MIPI_CSI0_DATA0_M	J1.64	IDS	MIPI CSI interface 0 lane 0 negative
MIPI_CSI0_DATA0_P	J1.66	IDS	MIPI CSI interface 0 lane 0 positive

4.2.2. MIPI CSI1

MIPI CSI1 Signals:

Signal	Pin #	Type	Description
MIPI_CSI1_CLK_M	J1.34	IDS	MIPI CSI interface 1 clock negative
MIPI_CSI1_CLK_P	J1.36	IDS	MIPI CSI interface 1 clock positive
MIPI_CSI1_DATA1_M	J1.38	IDS	MIPI CSI interface 1 lane 1 negative
MIPI_CSI1_DATA1_P	J1.40	IDS	MIPI CSI interface 1 lane 1 positive
MIPI_CSI1_DATA0_M	J1.42	IDS	MIPI CSI interface 1 lane 0 negative
MIPI_CSI1_DATA0_P	J1.44	IDS	MIPI CSI interface 1 lane 0 positive

4.2.3. Camera Control signals:

In addition to the signal lines the SOM exposes a dedicated I2C channel and Supplementing signals for camera control:

Camera Control signals:

Signal	Pin #	Type	Description
CAM_MCLK0	J1.84	O	Camera master clock 0
CAM_MCLK1	J1.80	O	Camera master clock 1
CCI_TIMER0	J2.85	O	Camera control interface timer 0
CCI_TIMER1	J2.87	O	Camera control interface timer 1
CCI_TIMER2	J2.55	O	Camera control interface timer 2
CCI_ASYNC0	J2.84	I	Camera control interface async 0
CAM0_RST_N	J2.83	O	Camera 0 reset
CAM1_RST_N	J1.82	O	Camera 1 reset
CAM0_STANDBY_N	J2.86	O	Camera 0 standby

4.3. Wi-Fi, Bluetooth, FM Radio

The DART-SD410 contains Qualcomm's The WCN3620 IC which integrates three different connectivity technologies into a single device:

- Wireless local area network (WLAN) compliant with the IEEE 802.11b/g/n specification
- Bluetooth (BT) compliant with the BT specification version 4.0 (BR/EDR+BLE)
- Worldwide FM radio, with Rx modes supporting the Radio Data System (RDS) for Europe and the Radio Broadcast Data System (RBDS) for the USA

4.4. USB 2.0 OTG

The DART-SD410 exports one USB 2.0 High-speed interface.
The USB port can be set to Host mode or Device mode.

USB Signals:

Signal	Pin #	Type	Description
USB_VBUS	J1.21	I	USB VBUS for OTG
USB_HS_D_M	J2.32	DS	USB HS data minus
USB_HS_D_P	J2.34	DS	USB HS data plus
USB_HS_ID	J2.64	I	USB ID pin for Host mode detection Low: Host mode High: Device mode

4.5. SD/MMC

The DART-SD410 MMC features a 4-bit SD/MMC card interface for connecting external memory or a Micro SD card slot.

SDC2 Signals:

Signal	Pin #	Type	Description
SDC2_DATA_3	J1.49	IO	SD card Data 3 line
SDC2_DATA_2	J1.51	IO	SD card Data 2 line
SDC2_DATA_0	J1.53	IO	SD card Data 0 line
SDC2_DATA_1	J1.55	IO	SD card Data 1 line
SDC2_CMD	J1.57	IO	SD card Command line
SDC2_CLK	J1.59	O	SD card Clock output

4.6. Audio

The DART-SD410 features the following audio interfaces:

- PM8196's integrated audio codec interfaces:
    1. Analog inputs:
        - 2 biased single ended microphones: 1 primary, 1 headset
          With Programmable input gain of: 0, 6, 12, 18, 21, and 24 dB
    2. Analog outputs:
        - 1 stereo headset with Up to five button MBHC headset support + input for headset jack detection; 1 Vrms output
        - Class-D mono speaker
        - Over current protection on HPH and speaker outputs

    Multiple input/output audio support sample rates of: 8, 16, 32, and 48 kHz

- APQ8016's integrated audio interfaces:
    1. Digital microphone input
    2. 2x MI2S Digital audio interface

PM8196 Audio interface Signals:

Signal	Pin #	Type	Description
CDC_VDD_SPKDRV	J1.9	POWER	+5V class-D speaker amplifier supply input
CDC_VDD_SPKDRV	J1.11	POWER	+5V class-D speaker amplifier supply input
SPKR_OUT_P	J1.13	AO	Class-D speaker amp + output
SPKR_OUT_M	J1.17	AO	Class-D speaker amp – output
CDC_HPH_L	J1.23	AO	Headphone left channel output
CDC_HPH_R	J1.25	AO	Headphone right channel output
CDC_HPH_REF	J1.27	AI	Headphone ground sensing
CDC_HS_DET	J1.29	AI	Headset detection
CDC_MIC_BIAS2	J1.33	AO	Microphone #2 bias
CDC_MIC_BIAS1	J1.35	AO	Microphone #1 bias
CDC_MIC1_P	J1.39	AI	Main microphone
GND_CFILT	J1.41	POWER	Ground reference for PMIC bias
CDC_MIC2_P	J1.43	AI	Headset microphone
GND_CFILT	J1.45	POWER	Ground reference for PMIC bias

APQ8016 Digital Microphone Signals:

Signal	Pin #	Type	Description
DMIC0_CLK	J2.23	O	Digital MIC0 clock
DMIC0_DATA	J2.27	IO	Digital MIC0 data

APQ8016 Digital Audio interface Signals:

Signal	Pin #	Type	Description
MI2S_2 _D1	J2.17	IO	MI2S interface #2 Data1 signal
MI2S_2 _D0	J2.59	IO	MI2S interface #2 Data0 signal
MI2S_2 _WS	J2.61	IO	MI2S interface #2 Word Select signal
MI2S_2 _SCK	J2.63	IO	MI2S interface #2 SCLK signal
MI2S_1_D0	J2.43	IO	MI2S interface #1 Data0 signal
MI2S_1_SCLK	J2.47	IO	MI2S interface #1 SCLK signal
MI2S_1 _WS	J2.51	IO	MI2S interface #1 Word Select signal
MI2S_1_D1	J2.79	IO	MI2S interface #1 Data1 signal

4.7. BAM-enabled low-speed peripheral (BLSP)

The BLSP supports the following serial protocols:

- UART_DM
  - Up to 4 Mbps UART
  - Supports all baud rates from 75 to 115200 bps and 4 Mbps
  - 5-8 bits character size, 0.5-2 bits stop bit, no/even/odd/space parity
  - Optional HW flow control based on CTS/RFR (HW or SW based)
  - Other: RX-break, hunt char, sticky error status, overflow detection, FIFO watermarking, FIFO resizing, HW data timeout, HW inactivity timeout
- I2C
  - Up to 3.4 MHz clock rate
- SPI
  - Up to 50 MHz operation on all six possible ports

The SOM exposes 6 BLSP ports each 4 bit wide. Each can be configured to one of the following options:

BLSP1 interface Signals:

bit	Pin	configuration				
		4-pin UART	**I2C + GPIOs**	**I2C + 2-pin UART**	**4-pin SPI**	**4 GPIOs**
3	J2.23	BLSP1_UART_TX UART transmit data	GPIO_0 Configurable I/O	BLSP1_UART_TX UART transmit data	BLSP1_SPI_MOSI SPI master out/slave in	GPIO_0 Configurable I/O
2	J2.27	BLSP1_UART_RX UART receive data	GPIO_1 Configurable I/O	BLSP1_UART_RX UART receive data	BLSP1_SPI_MISO SPI master in/slave out	GPIO_1 Configurable I/O
1	J2.29	BLSP1_UART_CTS_N UART clear-to-send	BLSP1_I2C_SDA_A I2C serial data	BLSP1_I2C_SDA_A I2C serial data	BLSP1_SPI_CS_N SPI chip select	GPIO_2 Configurable I/O
0	J2.25	BLSP1_UART_RFR_N UART ready-for-receive	BLSP1_I2C_SCL_A I2C serial clock	BLSP1_I2C_SCL_A I2C serial clock	BLSP1_SPI_CLK SPI clock	GPIO_3 Configurable I/O

BLSP2 interface Signals:

bit	Pin	configuration				
		4-pin UART	**I2C + GPIOs**	**I2C + 2-pin UART**	**4-pin SPI**	**4 GPIOs**
3	J1.83	BLSP2_UART_TX UART transmit data	GPIO_4 Configurable I/O	BLSP2_UART_TX UART transmit data	BLSP2_SPI_MOSI SPI master out/slave in	GPIO_4 Configurable I/O
2	J1.85	BLSP2_UART_RX UART receive data	GPIO_5 Configurable I/O	BLSP2_UART_RX UART receive data	BLSP2_SPI_MISO SPI master in/slave out	GPIO_5 Configurable I/O
1	J1.77	BLSP2_UART_CTS_N UART clear-to-send	BLSP2_I2C_SDA_A I2C serial data	BLSP2_I2C_SDA_A I2C serial data	BLSP2_SPI_CS_N SPI chip select	GPIO_6 Configurable I/O
0	J1.79	BLSP2_UART_RFR_N UART ready-for-receive	BLSP2_I2C_SCL_A I2C serial clock	BLSP2_I2C_SCL_A I2C serial clock	BLSP2_SPI_CLK SPI clock	GPIO_7 Configurable I/O

BLSP3 interface Signals:

bit	Pin	configuration				
		4-pin UART	**I2C + GPIOs**	**I2C + 2-pin UART**	**4-pin SPI**	**4 GPIOs**
3	J1.76	N/A	GPIO_8 Configurable I/O	N/A	BLSP3_SPI_MOSI SPI master out/slave in	GPIO_8 Configurable I/O
2	J1.72	N/A	GPIO_9 Configurable I/O	N/A	BLSP3_SPI_MISO SPI master in/slave out	GPIO_9 Configurable I/O
1	J1.70	N/A	BLSP3_I2C_SDA_A I2C serial data	N/A	BLSP3_SPI_CS_N SPI chip select	GPIO_10 Configurable I/O
0	J1.74	N/A	BLSP2_I2C_SCL_A I2C serial clock	N/A	BLSP3_SPI_CLK SPI clock	GPIO_11 Configurable I/O

BLSP4 interface Signals:

bit	Pin	configuration				
		4-pin UART	**I2C + GPIOs**	**I2C + 2-pin UART**	**4-pin SPI**	**4 GPIOs**
3	J2.73	N/A	GPIO_12 Configurable I/O	N/A	BLSP4_SPI_MOSI SPI master out/slave in	GPIO_12 Configurable I/O
2	J2.75	N/A	GPIO_13 Configurable I/O	N/A	BLSP4_SPI_MISO SPI master in/slave out	GPIO_13 Configurable I/O
1	J2.69	N/A	BLSP4_I2C_SDA_A	N/A	BLSP4_SPI_CS_N SPI chip select	GPIO_14 Configurable I/O
0	J2.67	N/A	BLSP4_I2C_SCL_A I2C serial clock	N/A	BLSP4_SPI_CLK SPI clock	GPIO_15 Configurable I/O

BLSP5 interface Signals:

bit	Pin	configuration				
		4-pin UART	I2C + GPIOs	I2C + 2-pin UART	4-pin SPI	4 GPIOs
3	J1.65	N/A	GPIO_16 Configurable I/O	N/A	BLSP5_SPI_MOSI SPI master out/slave in	GPIO_16 Configurable I/O
2	J1.69	N/A	GPIO_17 Configurable I/O	N/A	BLSP5_SPI_MISO SPI master in/slave out	GPIO_17 Configurable I/O
1	J1.67	N/A	BLSP5_I2C_SDA_B	N/A	BLSP5_SPI_CS_N SPI chip select	GPIO_18 Configurable I/O
0	J1.63	N/A	BLSP5_I2C_SCL_B I2C serial clock	N/A	BLSP5_SPI_CLK SPI clock	GPIO_19 Configurable I/O

BLSP6 interface Signals:

bit	Pin	configuration				
		4-pin UART	I2C + GPIOs	I2C + 2-pin UART	4-pin SPI	4 GPIOs
3	J2.28	N/A	GPIO_20 Configurable I/O	N/A	BLSP6_SPI_MOSI SPI master out/slave in	GPIO_20 Configurable I/O
2	J2.12	N/A	GPIO_21 Configurable I/O	N/A	BLSP6_SPI_MISO SPI master in/slave out	GPIO_21 Configurable I/O
1	J1.75	N/A	BLSP6_I2C_SDA_A	N/A	BLSP6_SPI_CS_N SPI chip select	GPIO_22 Configurable I/O
0	J1.73	N/A	BLSP6_I2C_SCL_A	N/A	BLSP6_SPI_CLK SPI clock	GPIO_23 Configurable I/O

Extra chip selects SPI for BLSP ports configured as SPI:

Signal	Pin #	Type	Description
BLSP1_SPI_CS3_N	J1.83	IO	BLSP 1 Chip select 3
BLSP2_SPI_CS3_N	J1.85	IO	BLSP 2Chip select 3
BLSP1_SPI_CS2_N	J1.65	IO	BLSP 1 Chip select 2
BLSP2_SPI_CS2_N	J1.69	IO	BLSP 2 Chip select 2
BLSP3_SPI_CS2_N	J1.87	IO	BLSP 3 Chip select 2
BLSP3_SPI_CS3_N	J2.52	IO	BLSP 3 Chip select 3
BLSP1_SPI_CS1_N	J2.51	IO	BLSP 1 Chip select 1
BLSP3_SPI_CS1_N	J2.14	IO	BLSP 3 Chip select 1
BLSP2_SPI_CS1_N	J2.64	IO	BLSP 2 Chip select 1

4.8. UIM

The SOM exposes one User identification module (UIM):

UIM Signals:

Signal	Pin #	Type	Description
UIM3_DATA	J2.46	IO	UIM3 data
UIM3_CLK	J2.48	O	UIM3 clock
UIM3_RESET	J2.50	O	UIM3 reset
UIM3_PRESENT	J2.44	I	UIM3 removal detection

4.9. Sensors and keypad

The SOM exposes several signals for Sensors and keypad buttons connection:

Sensors and keypad Signals:

Signal	Pin #	Type	Description
SMB_INT	J2.60	I	SMB interrupt
MAG_INT	J2.52	I	Magnometer interrupt
GYRO_ACCEL_INT_N	J2.79	I	Gyro interrupt
KYPD_SNS0	J2.62	I	Keypad sense bit 0
KYPD_SNS1	J2.54	I	Keypad sense bit 1
KYPD_SNS2	J2.58	I	Keypad sense bit 2

4.10. JTAG

The SOM exports a JTAG interface for debug and test control

JTAG signals:

Signal	Pin #	Type	Description
JTAG_SRST_N	J2.68	I	JTAG reset for debug
JTAG_TMS	J2.70	I	TAG mode-select input
JTAG_TCK	J2.72	I	JTAG clock input
JTAG_TDI	J2.74	I	JTAG data input
JTAG_TRST_N	J2.76	I	JTAG reset
JTAG_TDO	J2.78	O	JTAG data output
JTAG_PS_HOLD	J2.80	I	Power-supply hold control input

4.11. General Purpose IOs

Many of the APQ8016 pins can be used as GPIOs.
In addition, the PM8196 exports 3 multipurpose pins (MPPs) & 4 GPIOs.

PM8196 MPPs can be configured as:
1) Digital in/out
2) Uni-directional level-translating I/Os
3) Analog multiplexer inputs
4) Current sinks
5) VREF buffer outputs

PM8196 GPIOs are configurable as digital inputs or outputs or level-translating I/Os, and are faster than MPPs

See Chapter 3, Tables 3.1 and 3.2 for complete SOM connectors signal list and GPIO multiplexing.

4.12. General System Control

4.12.1. Boot Options

Boot Configuration pins [14:0] control various secure boot, debugging, and boot device options (Refer to section 3.2 for complete signal list and multiplexing).
Many of these options are hard-wired on shipped devices via qFUSE settings.
The following boot configuration pins and GPIOs are of interest:

Pin Name	Pin Number
BOOT_CONFIG_0	J2.24
BOOT_CONFIG_1	J2.22
BOOT_CONFIG_2	J2.33
BOOT_CONFIG_3	J2.26
BOOT_CONFIG_5	J2.35
FORCED_USB_BOOT	J1.87

1) BOOT_CONFIG[3:1]
These pins determine the SOM boot sequence according to the following truth table:

BOOT_CONFIG[3:1]	BOOT OPTIONS
000	SDC1 --> SDC2 --> USB2.0
001	SDC2 --> SDC1 --> USB2.0
010	SDC1 --> USB2.0
011	USB2.0

Note:
The Default Boot option is 000, which is the On-SOM eMMC connected to SDC1 interface.

2) BOOT_CONFIG[0]

Pin Name	Pin Number
BOOT_CONFIG_0	J2.24

When high ‘1’ Watch Dog is disabled

3) BOOT_CONFIG[5]

Pin Name	Pin Number
BOOT_CONFIG_5	J2.35

Requires an External 10K ohm pull up for Apps Boot from eMMC

4) FORCED_USB_BOOT

Pin Name	Pin Number
FORCED_USB_BOOT	J1.87

An option for forced USB Boot is available through this pin.
When High ‘1’ the boot source will be from USB regardless of the BOOT_CONFIG pins’ state.

4.12.2. Power

Pin Name	Pin Number
PHONE_ON_N	J2.9

Upon applying power the board, the boot process will start. Once the board is running:
A board shut-down will occur when this signal is logic '0' for more than 8 seconds
If the board in sleep mode setting this signal to logic '0' low for more than 3 sec will wake up the board.

4.12.3. Reset

Pin Name	Pin Number
APQ_RESIN_N	J1.89

A logic '0' will reset the board.

Pin Name	Pin Number
PM_RESIN_N	J2.7

A logic '0' lasting less more 10 seconds Reset.

4.12.4. General purpose clocks, PDM, and additional RFIC interface signals

The APQ8016 IC has several general purpose clock outputs, as well as general purpose pulse Density modulated (PDM) outputs:

- GP_PDM – a configurable pulse-density output (12-bit value configurable), with the base frequency set at 4.8 MHz.
  - The APQ8016 supports three different instances of this configurable PDM output
  - GP_PDM0, 1, and 2 can each be used independently. If there is an A or B option in the IO name, it means only one or the other can be used.

- G GP_CLK – A general purpose clock output that lets the user configure a desired clock output by first selecting a clock source (GPLL0 or 19.2 MHz) and then programming a desired
  - The APQ8016 supports four different instances of this clock output
  - GP_CLK0, 1, 2, and 3 can be used independently. If there is an A or B option in the IO name, it means only one or the other can be used.
  - Different division ratios may result in differing jitter, with integer divisors producing the cleanest outputs.

- GP_MN – Similar to GP_CLK, except the source clock is always 4.8 MHz. It is only Available behind GPIO110.

General purpose clocks, PDM:

Signal	Pin #	Type	Description
GP_PDM_1A	J2.44	O	General-purpose PDM output 1A, 12-bit, XO/4 clock
GP_PDM_0B	J2.38	O	General-purpose PDM output 0B, 12-bit, XO/4 clock
GP_PDM_1B	J2.12	O	General-purpose PDM output 1B, 12-bit, XO/4 clock
GP_PDM_2A	J2.53	O	General-purpose PDM output 2A, 12-bit, XO/4 clock
GP_PDM_2B	J2.47	O	General-purpose PDM output 2B, 12-bit, XO/4 clock
GP_CLK0	J2.85	O	General-purpose clock 0

GP_CLK1	J2.87	O	General-purpose clock 1
GP_CLK_1A	J2.46	O	General-purpose clock 1A
GP_CLK_2A	J2.48	O	General-purpose clock 2A
GP_CLK_3A	J2.50	O	General-purpose clock 3A
GP_CLK_1B	J2.81	O	General-purpose clock 1B
GP_CLK_2B	J2.73	O	General-purpose clock 2B
GP_CLK_3B	J2.75	O	General-purpose clock 3B
GP_MN	J2.51	O	General-purpose M/N:D counter output

Additional RFIC interface signals:

Signal	Pin #	Type	Description
SSBI_WTR1_RX	J2.45	IO	SSBI (single-wire serial bus Interface) 1 for RFIC 1
SSBI_WTR1_TX	J2.39	IO	SSBI (single-wire serial bus Interface) 2 for RFIC 1

4.13. Power

4.13.1. Power Supply

Signal	Pin #	Type	Description
VPH_PWR	J1.1-J1.8	Power In	DART-SD410 Single DC-IN Supply voltage. Voltage range: 3.7V -4.5V
CDC_VDD_SPKDRV	J1.9, J1.11	Power In	5V class-D speaker amplifier supply input
VREG_L11_SDC	J2.1, J2.3	Power Out	2.95V power supply output for External SD Card
VREG_L12_SDC	J2.13	Power Out	2.95V power supply output for External SD Card

4.13.2. Ground

Signal	Pin #	Type	Description
DGND	J1.10, J1.31, J1.32, J1.37, J1.46, J1.47, J1.61, J1.68, J1.71, J1.78, J1.81, J1.86, J2.5, J2.11, J2.15, J2.21, J2.30, J2.31, J2.36, J2.37, J2.42, J2.49, J2.56, J2.65, J2.66, J2.77, J2.82, J2.89, J2.90	Power	Digital ground
GND_CFILT	J1.41, J1.45	Power	Ground reference for PMIC bias

5. Absolute Maximum Characteristics

Power Supply	Min	Max	Unit
Main Power Supply, DC-IN	-0.5	6	V
Class-D speaker amplifier supply input, CDC_VDD_SPKDRV	-0.5	6	V

6. Operational Characteristics

6.1. Power supplies

	Min	Typical	Max	Unit
Main Power Supply, DC-IN	3.7	3.7	4.5	V
CDC_VDD_SPKDRV	3.0	3.7/5.0	5.5	V

6.2. Power Consumption

CPU usage:

Task	SOM VBAT current draw in ma @3.7v
Suspend *	Less than 5 mA
Idle (~10% CPU) @ 400mhz	60 mA
FHD Movie Video playback on 800x480 LVDS Screen	200 mA
Camera record 1080p	450 mA
100% CPU Dhrystone test – Quad core	850 mA
Suggested power supply capability	2000 mA

*Note: Suspend mode supported only in Android.

Additional peripherals:

Task	SOM VBAT current draw in ma @3.7v
WLAN transmission	200 mA
GPS	120 mA

Power supplies Output rating:

Power Rail	Max allowed current draw in ma
VREG_L11_SDC	600mA
VREG_L12_SDC	50mA

For more information please visit out Wiki Page at address:
http://variwiki.com/index.php?title=DART-SD410_Android_Comparison

7. Heat spread

There are solder mask free copper islands on the bottom of the SOM.
The copper islands are connected to ground and should be used to guide heat away from the SOM to the base board. They can be left unconnected if heat guidance is not needed.

8. DC Electrical Characteristics

APQ8016 Digital 1.8V: Camera Control, DMIC, MI2S, BLSP, UIM, Sensor, Keypad, JTAG, General System Control, GPIOs.

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage	CMOS/Schmitt	1.17	-	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-	0.63	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength	1.35		V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	-	0.45	V
RP	Pull resistance	Pull-up and pull-down	55	390	kΩ
RK	Keeper resistance		30	150	kΩ
I_{IH}	Input high leakage current	No pull-down	-	1	µA
I_{IL}	Input low leakage current	No pull-up	-1	-	µA
V_{SHYS}	Schmitt hysteresis voltage		100		mV
$C_{I/O}$	I/O capacitance		-	5	pF

APQ8016 Digital 1.8V: UIM

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage	CMOS/Schmitt	1.26	2.1	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.36	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength	1.44	1.8	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	0	0.4	V
RP	Pull resistance	Pull-up and pull-down	10	100	kΩ
RK	Keeper resistance		10	100	kΩ
I_{IH}	Input high leakage current	No pull-down	-	2	µA
I_{IL}	Input low leakage current	No pull-up	-2	-	µA
V_{SHYS}	Schmitt hysteresis voltage		100	-	mV
$C_{I/O}$	I/O capacitance		-	5	pF

APQ8016 Digital 2.95V: SD/MMC

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage	CMOS/Schmitt	1.125	2.1	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.45	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength	1.35	1.8	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	0	0.225	V
RP	Pull resistance	Pull-up and pull-down	10	100	kΩ

Parameter		Comments	Min	Max	Unit
RK	Keeper resistance		10	100	kΩ
I_{IH}	Input high leakage current	No pull-down	-	10	µA
I_{IL}	Input low leakage current	No pull-up	-10	-	µA
V_{SHYS}	Schmitt hysteresis voltage		100	-	mV
$C_{I/O}$	I/O capacitance		-	5	pF

PM8196 GPIOs:

Parameter		Comments	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		0.65 x V_G[1]	-	V_G[1] +0.3	V
V_{IL}	Low-level input voltage		-0.3	-	0.35 xV_G[1]	V
V_{SHYS}	Schmitt hysteresis voltage		15	-	-	mV
I_L	Input leakage current[2]	V_G = max, VIN= 0 V to V_G	-200	-	+200	nA
V_{OH}	High-level output voltage	$I_{OUT} = I_{OH}$	V_G[1] – 0.5	-	V_G[1]	V
V_{OL}	Low-level output voltage	$I_{OUT} = I_{OL}$	0	-	0.45	V
I_{OH}	High-level output current	$V_{OUT} = V_{OH}$	3	-	-	mA
I_{OL}	Low-level output current	$V_{OUT} = V_{OL}$	-	-	-3	mA
C_{IN}	Input capacitance		-	-	5	pF

Notes:

[1] V_G supply options: VPH_PWR, 1.2V, 1.8V.
(GPIO_1 and GPIO_2 do not support VPH_PWR domain).

[2] GPIO pins comply with the input leakage specification only when configured as digital inputs, or set to their tri-state mode.

PM8196 MPPs:

Parameter	Comments	Min	Typ	Max	Unit
MPP configured as digital input[1]					
Logic high input voltage		0.65 * V_M[3]	-	-	V
Logic low input voltage		-	-	0.35 * V_M[3]	V
MPP configured as digital output[1]					
Logic high output voltage	Iout= IOH	V_M[3] - 0.45	-	V_M[3]	V
Logic low output voltage	Iout = IOL	0	-	0.45	V
MPP configured as analog input (analog multiplexer input)					
Input current		-	-	100	nA
Input capacitance		-	-	10	pF
MPP configured as analog output (buffered VREF output)[2]					
Output voltage error	-50 µA to +50 µA	-	-	12.5	mV
Temperature variation	Due to buffer only	-0.03	-	0.03	%

Parameter	Comments	Min	Typ	Max	Unit
MPP configured as digital input[1]					
Load capacitance		-	-	25	pF
Power-supply current		-	0.17	0.2	mA
MPP configured as current sink[2]					
Power supply voltage		-	VDD	-	V
Sink current	Programmable in 5 mA increment	0		40	Ma
Sink current accuracy	VOUT= 0.7 V to (VDD- 1 V)	-20		+20	%
Power-supply current			105	115	µA
MPP configured as level translator					
Maximum frequency		4	-	-	MHz

Notes:

[1] Input and output stages can use different power supplies, thereby implementing a level translator. See V_M supply options note [3].

[2] Only even MPPs (MPP_2 and MPP_4) can be configured as current sink and only odd MPPs (MPP_1 and MPP_3) can be configured as analog output.

[3] V_M supply options: VPH_PWR, 1.2V, 1.8V

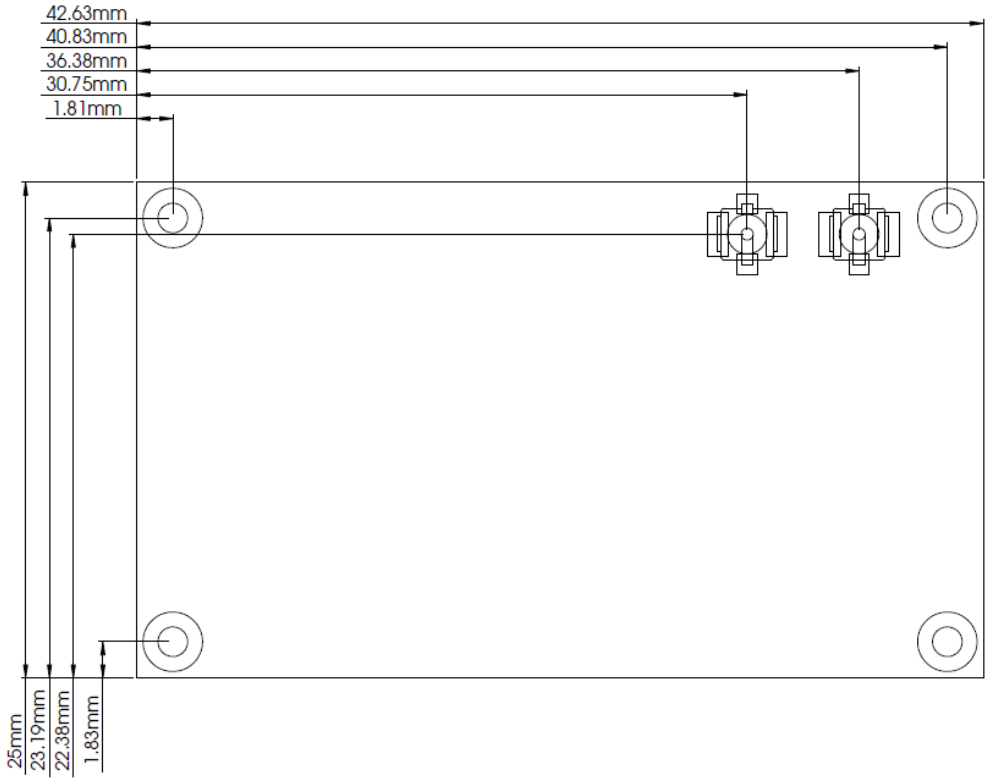
9. Environmental Specifications

	Min	Max
Commercial Operating Temperature Range	-30 ^{0}C	+85 ^{0}C
Referring Telcordia Technologies Special Report SR-332, Issue 4 Reliability Prediction Method Model: 25Deg Celsius, Class B-1, GM 25Deg Celsius, Class B-1, GF 25Deg Celsius, Class B-1, GB	 2075 Khrs > 4852 Khrs > 9275 Khrs >	

Note: Extended and Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

10. Mechanical Drawings

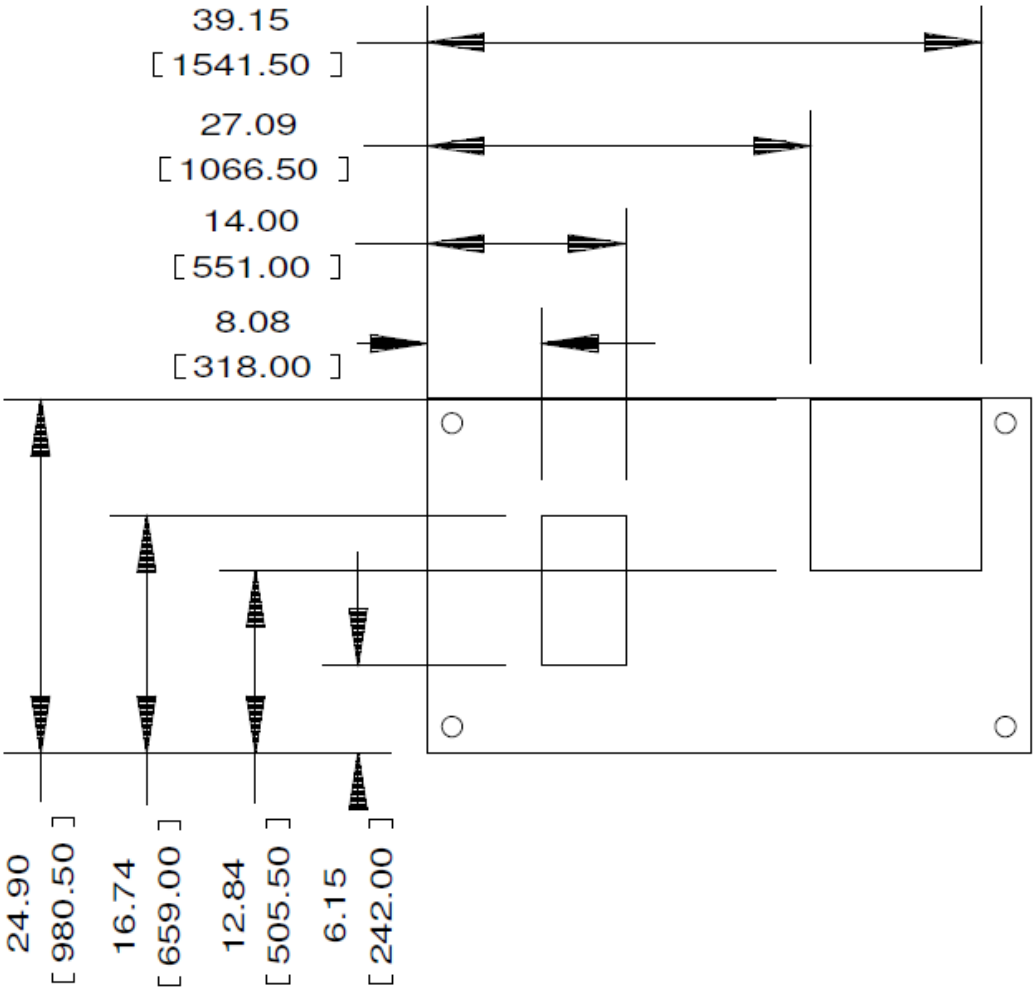
Top View



Drill diameter: 59mils = 1.4986mm

Ground pad diameter: 118mils = 2.9972mm

Heat Dissipation plates view



Note:
PCB Thickness is 1.2mm.

CAD files are available for download at http://www.variscite.com/

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