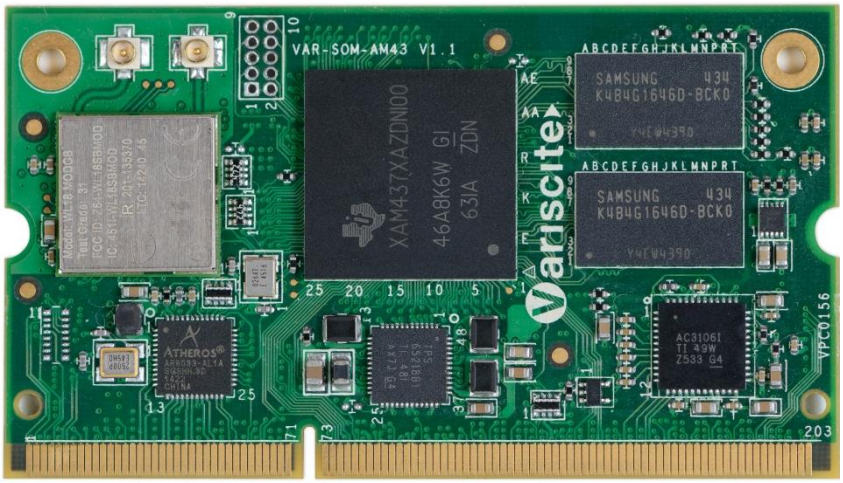
VARISCITE LTD.

VAR-SOM-AM43 v1.1 Datasheet

Texas Instruments Sitara AM437x -based System-on-Module



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VAR-SOM-AM43 Datasheet

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Document Revision History

Revision	Date	Notes
1.0	20/01/2015	Initial
1.1	13/11/2016	Section 3.1 - Removed note for pins 114,115,148,149 Corrected ball number typo pin 116 Section 4.6.2 - Updated MCASP0 Pinout table Section 4.16.1 - Updated table in accordance with TRM and VAR-AM43CustomBoard schematics
1.2	23/10/2017	Section 3.1 - Updated notes 1,2,4,5 Section 4.84 - Updated note 3 Section 4.14 - Updated note 1
1.3	02/11/2017	Section 1.2, 2.5, 4.19 - Updated Bluetooth features
1.4	25/07/2018	Section 7 - Updated Reliability Prediction data
1.5	17/05/2022	Sections: 1.2,2.5,4.19 – Updated the BT
1.6	03/07/2022	Added Ethernet PHY ADIN1300 – Updated sections 2.3,3.1,4.3.1,

Table of Contents

1. About this Document

1.1. Overview

The VAR-SOM-AM43 is a highly integrated cost-effective System-on-Module that perfectly fits various embedded and industrial products and segment. It is based on AM437x 1GHz ARM® Cortex™-A9 multipurpose processor from TEXAS INSTRUMENTS Sitara™ family.

The VAR-SOM-AM43 provides an ideal building block for simple integration with a wide range of products in target markets requiring rich connectivity in a compact, cost effective SoM with low power consumption.

Variscite also provides a complete hardware and software development kit (DVK) for the SoM in the form of a carrier board with 204-pin edge connector for the VAR-SOM-AM43 and an optional TFT display and touch panel. The carrier board of the VAR-SOM-AM43 is ideal not only as reference for the customer to develop its own custom board but also as a cost effective solution for production. Details of this carrier board and development kit can be found inside the VAR-AM43CustomBoard datasheet and the related documentation inside Variscite website: www.variscite.com

Supporting products:

- VAR-AM43CustomBoard – evaluation board
  - ✓ Carrier -Board, compatible with VAR-SOM-AM43
  - ✓ Schematics
- O.S support
  - ✓ Linux (Yocto)

Contact Variscite support services for further information:
mail to: support@variscite.com.

1.2. VAR-SOM-AM43 Features Summary

- High performance up to 1000-MHz ARM® Cortex™-A9 32-Bit RISC Microprocessor

NEON™ SIMD Coprocessor and Vector Floating Point (VFPv3) Coprocessor

SGX530 Graphics Engine

4 x 200MHz 32-bits RISC co-processors programmable real-time unit (PRU)

Up to 1 GB DDR3 RAM

Up to 32GB eMMC storage

Up to 512MB NAND Flash for storage memory / boot

LCD Display Up to 1400x1050 Parallel, 24-Bit RGB interface

Capacitive touch panel and 4/5-wire resistive touch panel interface

On-board 10/100/1000 Mbps Ethernet PHY

Second 10/100/1000 Mbps Ethernet RGMII Interface

Certified WLAN (802.11 a/b/g/n) module with optional MIMO

Bluetooth 5.1/BLE with CSA2 support

USB:

– 1 x USB 2.0 host with integrated PHY

– 1 x USB 2.0 OTG with integrated PHY

2 x CAN bus

Serial interfaces (4xSPI, 3xI2C, 5xUART, HDQ/1-Wire, QSPI)

Camera input, 12bit

Audio:

– 1 x stereo line-in

– 1 x stereo line-out

– 1 x stereo Digital Microphone-in

– 1 x stereo Analog Microphone-in

– Multichannel Audio Serial Port (McASP)

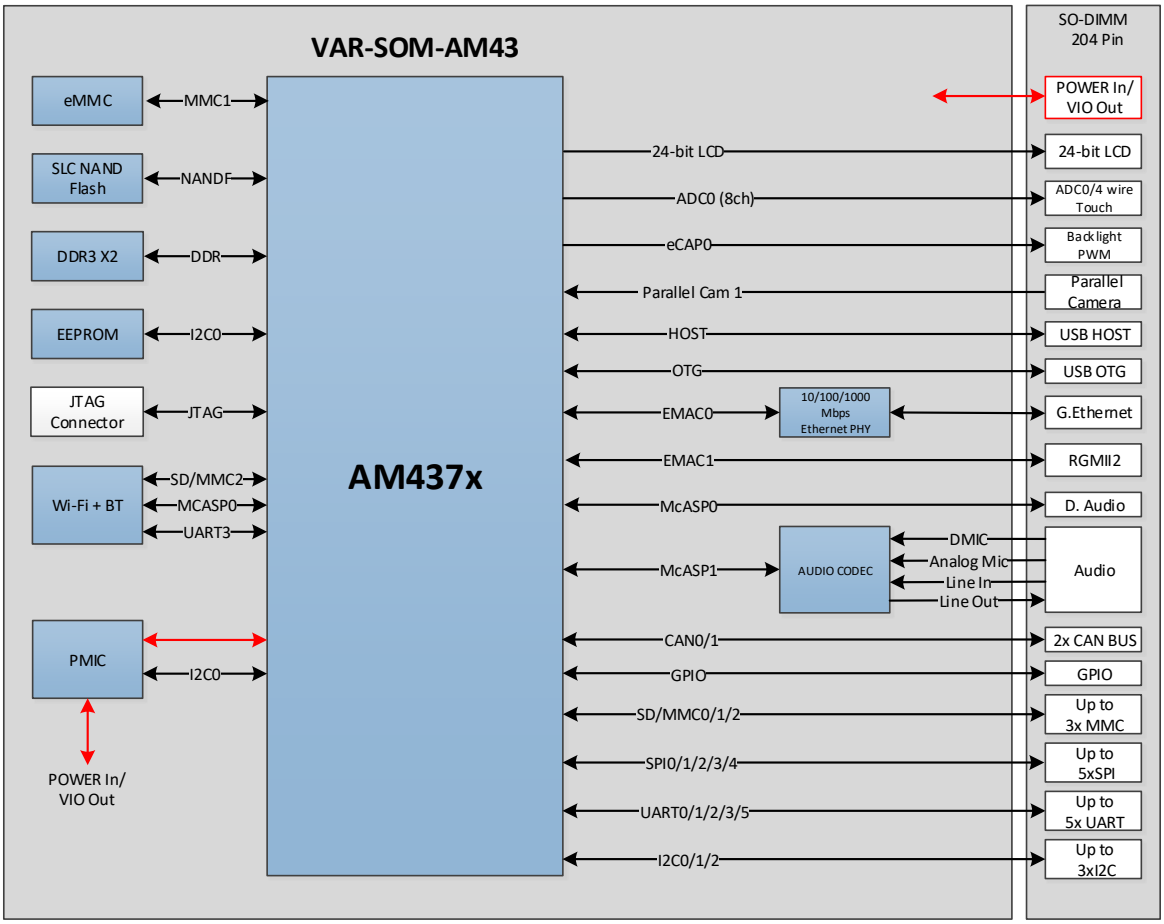
8 x ADC – inputs

Backlight PWM

Single 3.3 V power supply

67.6 mm x 38.6 mm x 3 mm DDR3 SODIMM 204pins footprint

1.3. VAR-SOM-AM43 Block Diagram



2. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-AM43

2.1. TEXAS INSTRUMENTS AM437x ARM® Cortex™-A9

2.1.1. Overview

The AM437x microprocessors based on the ARM Cortex-A9 are enhanced with image, graphics processing, peripherals and industrial interface options.
The AM437x microprocessor contains the following subsystems, controller and interfaces:

TEXAS INSTRUMENTS AM437x ARM® Cortex™-A9

- Highlights
  - Up to 1000-MHz ARM® Cortex™-A9 32-Bit RISC Microprocessor
    - NEON™ SIMD Coprocessor and Vector Floating Point (VFPv3) Coprocessor
    - 32KB of Both L1 Instruction and Data Cache
    - 256KB of L2 Cache or L3 RAM
  - 32-Bit LPDDR2, DDR3, and DDR3L Support
  - General-Purpose Memory Support (NAND, NOR, SRAM) Supporting Up to 16-bit ECC
  - SGX530 Graphics Engine
  - Display Subsystem
  - Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)
  - Real-Time Clock (RTC)
  - Up to Two USB 2.0 High-Speed Dual-Role (Host or OTG) Ports with integrated PHY
  - 10, 100, and 1000 Ethernet Switch Supporting Up to Two Ports
  - Serial Interfaces:
    - Two Controller Area Network (CAN) Ports
    - Six UARTs, Two McASPs, Five McSPI, Three I^2C Ports, One QSPI and One HDQ or 1-Wire
  - Security
    - Crypto Hardware Accelerators (AES, SHA, RNG, DES and 3DES)
    - Secure Boot
  - Two 12-Bit Successive Approximation Register (SAR) ADCs
  - Up to Three 32-Bit Enhanced Capture Modules (eCAP)
  - Up to Three Enhanced Quadrature Encoder Pulse Modules (eQEP)
  - Up to Six Enhanced High-Resolution PWM Modules (eHRPWM)

- MPU Subsystem
  - Up to 1000-MHz ARM Cortex-A9 32-Bit RISC Microprocessor
  - 32KB of Both L1 Instruction and Data Cache
  - 256KB of L2 Cache (Option to Configure as L3 RAM)
  - 256KB of On-Chip Boot ROM
  - 64KB On-Chip RAM
  - Secure Control Module (SCM)
  - Emulation and Debug
    - JTAG
    - Embedded Trace Buffer
  - Interrupt Controller
- On-Chip Memory (Shared L3 RAM)
  - 256KB of General Purpose On-Chip Memory Controller (OCMC) RAM
  - Accessible to All Masters
  - Supports Retention for Fast Wakeup
  - Up to 512KB of Total Internal RAM (256KB of ARM Memory Configured as L3 RAM + 256KB of OCMC RAM)
- External Memory Interfaces (EMIF)
  - DDR Controllers:
    - LPDDR2: 266-MHz Clock (LPDDR2-533 Data Rate)
    - DDR3 and DDR3L: 400-MHz Clock (DDR 800 Data Rate)
    - 32-Bit Data Bus
    - 2GB of Total Addressable Space
    - Supports One x32, Two x16, or Four x8 Memory Device Configurations
- General-Purpose Memory Controller (GPMC)
  - Flexible 8- and 16-Bit Asynchronous Memory Interface with Up to Seven Chip Selects (NAND, NOR, Muxed-NOR, and SRAM)
  - Uses BCH Code to Support 4-, 8-, or 16-Bit ECC
  - Uses Hamming Code to Support 1-Bit ECC
- Error Locator Module (ELM)
  - Used with the GPMC to Locate Addresses of Data Errors from Syndrome Polynomials Generated Using a BCH Algorithm
  - Supports 4-, 8-, and 16-Bit Per 512-Byte Block Error Location Based on BCH Algorithms
- Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)
  - Supports Protocols such as EtherCAT®, PROFIBUS, PROFINET, and EtherNet/IP™, EnDat 2.2, and More
  - Two Programmable Real-Time Units (PRUs) Subsystems
    - Each core is a 32-Bit Load and Store RISC Processor Capable of Running at 200 MHz

    - 12KB (PRU-ICSS1), 4KB (PRU-ICSS0) of Instruction RAM with Single-Error Detection (Parity)
    - 8KB (PRU-ICSS1), 4KB (PRU-ICSS0) of Data RAM with Single-Error Detection (Parity)
    - Single-Cycle 32-Bit Multiplier with 64-Bit Accumulator
    - Enhanced GPIO Module Provides Shift-In and Shift-Out Support and Parallel Latch on External Signal
  - 12KB (PRU-ICSS1 only) of Shared RAM with Single-Error Detection (Parity)
  - Three 120-Byte Register Banks Accessible by Each PRU
  - Interrupt Controller Module (INTC) for Handling System Input Events
  - Local Interconnect Bus for Connecting Internal and External Masters to the Resources Inside the PRU-ICSS
  - Peripherals Inside the PRU-ICSS
    - One UART Port with Flow Control Pins, Supports Up to 12 Mbps
    - One Enhanced Capture (eCAP) Module
    - Two MII Ethernet Ports that Support Industrial Ethernet, such as EtherCAT
    - One MDIO Port
  - Industrial Communication is Supported by Two PRU-ICSS Subsystems
- Power Reset and Clock Management (PRCM) Module
  - Controls the Entry and Exit of Deep-Sleep Modes
  - Responsible for Sleep Sequencing, Power Domain Switch-Off Sequencing, Wake-Up Sequencing, and Power Domain Switch-On Sequencing
  - Clocks
    - Integrated High-Frequency Oscillator Used to Generate a Reference Clock (19.2, 24, 25, and 26 MHz) for Various System and Peripheral Clocks
    - Supports Individual Clock Enable and Disable Control for Subsystems and Peripherals to Facilitate Reduced Power Consumption
    - Five ADPLLs to Generate System Clocks (MPU Subsystem, DDR Interface, USB, and Peripherals (MMC and SD, UART, SPI, I^2C), L3, L4, Ethernet, GFX (SGX530), and LCD Pixel Clock)
  - Power
    - Two Non-Switchable Power Domains (RTC and Wake-Up Logic (WAKE-UP))
    - Three Switchable Power Domains (MPU Subsystem, SGX530 (GFX), Peripherals and Infrastructure (PER))
    - Implements SmartReflex™ Class 2B for Core Voltage Scaling Based On Die Temperature, Process Variation and Performance (Adaptive Voltage Scaling (AVS)) Dynamic Voltage Frequency Scaling (DVFS)
- Real-Time Clock (RTC)
  - Real-Time Date (Day, Month, Year, and Day of Week) and Time (Hours, Minutes, and Seconds) Information
  - Internal 32.768-kHz Oscillator, RTC Logic, and 1.1-V Internal LDO
  - Independent Power-On-Reset (RTC_PWRONRSTn) Input

- Dedicated Input Pin (RTC_WAKEUP) for External Wake Events
- Programmable Alarm Can Generate Internal Interrupts to the PRCM for Wake Up or Cortex- A9 for Event Notification
- Programmable Alarm Can Be Used with External Output (RTC_PMIC_EN) to Enable the Power Management IC to Restore Non-RTC Power Domains

• Peripherals
- Up to Two USB 2.0 High-Speed OTG Ports with Integrated PHY
- Up to Two Industrial Gigabit Ethernet MACs (10, 100, and 1000 Mbps)
  - Integrated Switch
  - Each MAC Supports MII, RMII, and RGMII and MDIO Interfaces
  - Ethernet MACs and Switch Can Operate Independent of Other Functions
  - IEEE 1588v2 Precision Time Protocol (PTP)
- Up to Two Controller-Area Network (CAN) Ports
  - Supports CAN Version 2 Parts A and B
- Up to Two Multichannel Audio Serial Ports (McASP)
  - Transmit and Receive Clocks Up to 50 MHz
  - Up to Four Serial Data Pins Per McASP Port with Independent TX and RX Clocks
  - Supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and Similar Formats
  - Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 Formats)
  - FIFO Buffers for Transmit and Receive (256 Bytes)
- Up to Six UARTs
  - All UARTs Support IrDA and CIR Modes
  - All UARTs Support RTS and CTS Flow Control
  - UART1 Supports Full Modem Control
- Up to Five Master and Slave McSPI Serial Interfaces
  - McSPI0-McSPI2 Supports Up to Four Chip Selects
  - McSPI3-McSPI4 Supports Up to Two Chip Selects
- Up to 48 MHz
  - One Quad-SPI
  - Supports eXecute In Place (XIP) from Serial NOR FLASH
- One Dallas 1-Wire® and HDQ Serial Interface
- Up to Three MMC, SD, and SDIO Ports
  - 1-, 4-, and 8-Bit MMC, SD, and SDIO Modes
  - 1.8- or 3.3-V Operation on All Ports
  - Up to 48-MHz Clock
  - Supports Card Detect and Write Protect
  - Complies with MMC4.3 and SD and SDIO 2.0 Specifications

- Up to Three I2C Master and Slave Interfaces
  - Standard Mode (Up to 100 kHz)
  - Fast Mode (Up to 400 kHz)
- Up to Six Banks of General-Purpose I/O (GPIO)
  - 32 GPIOs per Bank (Multiplexed with Other Functional Pins)
  - GPIOs Can be Used as Interrupt Inputs (Up to Two Interrupt Inputs per Bank)
- Up to Three External DMA Event Inputs That Can Also be Used as Interrupt Inputs
- Twelve 32-Bit General-Purpose Timers
  - DMTIMER1 is a 1-ms Timer Used for Operating System (OS) Ticks
  - DMTIMER4–DMTIMER7 are Pinned Out
- One Public Watchdog Timer
- One Free Running High Resolution 32-kHz Counter (synctimer32K)
- SGX530 3D Graphics Engine
  - Tile-Based Architecture Delivering Up to 20M Poly/sec
  - Universal Scalable Shader Engine is a Multi- Threaded Engine Incorporating Pixel and Vertex Shader Functionality
  - Advanced Shader Feature Set in Excess of Microsoft VS3.0, PS3.0, and OGL2.0
  - Industry Standard API Support of Direct3D Mobile, OGL-ES 1.1 and 2.0, and OpenVG 1.0
  - Fine-Grained Task Switching, Load Balancing, and Power Management
  - Advanced Geometry DMA-Driven Operation for Minimum CPU Interaction
  - Programmable High-Quality Image Anti- Aliasing
  - Fully Virtualized Memory Addressing for OS Operation in a Unified Memory Architecture
- Display Subsystem
  - Display Modes
    - Programmable Pixel Memory Formats (Palletized: 1-, 2-, 4-, and 8-Bit Per Pixel; RGB 16- and 24-Bit Per Pixel; and YUV 4:2:2)
    - 256 x 24-Bit Entries Palette in RGB
    - Up to 2048 x 2048 Resolution
  - Display Support
    - Four Types of Displays Are Supported: Passive and Active Colors; Passive and Active Monochromes
    - 4- and 8-Bit Monochrome Passive Panel Interface Support (15 Grayscale Levels Supported Using Dithering Block)
    - RGB 8-Bit Color Passive Panel Interface Support (3,375 Colors Supported for Color Panel Using Dithering Block)
    - RGB 12-, 16-, 18-, and 24-Bit Active Panel Interface Support (Replicated or Dithered Encoded Pixel Values)
    - Remote Frame Buffer (Embedded in the LCD Panel) Support through the RFBI Module

- Partial Refresh of the Remote Frame Buffer through the RFBI Module
- Partial Display
- Multiple Cycles Output Format on 8-, 9-, 12-, and 16-Bit Interface (TDM)

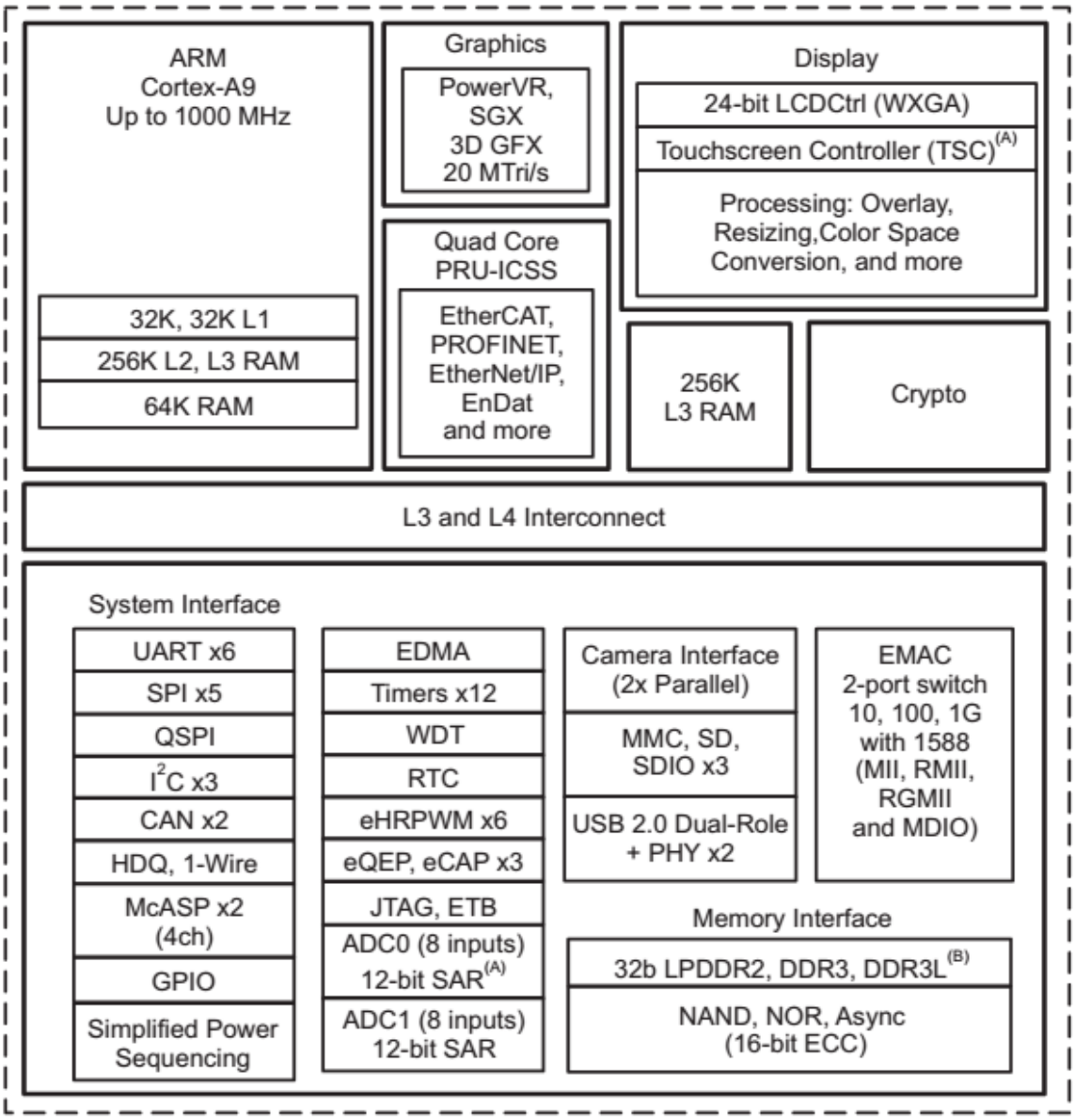
- Signal Processing
  - Overlay and Windowing Support for One Graphics Layer (RGB or CLUT) and Two Video Layers (YUV4:2:2, RGB16, and RGB24)
  - RGB 24-bit Support on the Display Interface, Optionally Dithered to RGB 18-Bit Pixel Output Plus 6-Bit Frame Rate Control (Spatial and Temporal)
  - Transparency Color Key (Source and Destination)
  - Synchronized Buffer Update
  - Gamma Curve Support
  - Multiple-Buffer Support
  - Cropping Support
  - Color Phase Rotation

- Two 12-Bit Successive Approximation Register (SAR) ADCs (ADC0, ADC1)
  - 867K Samples Per Second
  - Input Can Be Selected from Any of the Eight Analog Inputs Multiplexed Through an 8:1 Analog Switch
  - ADC0 Can Be Configured to Operate as a 4-, 5-, or 8-Wire Resistive Touch Screen Controller (TSC)
- Up to Three 32-Bit Enhanced Capture Modules (eCAP)
  - Configurable as Three Capture Inputs or Three Auxiliary PWM Outputs
- Up to Six Enhanced High-Resolution PWM Modules (eHRPWM)
  - Dedicated 16-Bit Time-Base Counter with Time and Frequency Controls
  - Configurable as Six Single-Ended, Six Dual- Edge Symmetric, or Three Dual-Edge Asymmetric Outputs
- Up to Three 32-Bit Enhanced Quadrature Encoder Pulse (eQEP) Modules

- Device Identification
  - Factory Programmable Electrical Fuse Farm (FuseFarm)
    - Production ID
    - Device Part Number (Unique JTAG ID)
    - Device Revision (Readable by Host ARM)
    - Feature Identification
- Debug Interface Support
  - JTAG and cJTAG for ARM (Cortex-A9 and PRCM) and PRU-ICSS Debug
  - Supports Real-Time Trace Pins (for Cortex-A9)
  - 64KB Embedded Trace Buffer (ETB)
  - Supports Device Boundary Scan

  - Supports IEEE 1500
- DMA
  - On-Chip Enhanced DMA Controller (EDMA) Has Three Third-Party Transfer Controllers (TPTC) and One Third-Party Channel Controller (TPCC), Which Supports Up to 64 Programmable Logical Channels and Eight QDMA Channels
  - EDMA is Used for:
    - Transfers to and from On-Chip Memories
    - Transfers to and from External Storage (EMIF, General-Purpose Memory Controller, and Slave Peripherals)
- Inter-Processor Communication (IPC)
  - Integrates Hardware-Based Mailbox for IPC and Spinlock for Process Synchronization Between the Cortex-A9, PRCM, and PRU-ICSS
- Boot Modes
  - Boot Mode is Selected via Boot Configuration Pins Latched on the Rising Edge of the PWRONRSTn Reset Input Pin
- Camera
  - Dual Port 8- and 10-Bit BT656 Interface
  - Dual Port 8- and 10-Bit Including External Syncs
  - Single Port 12-Bit
  - YUV422/RGB422 and BT656 Input Format
  - RAW Format
  - Pixel Clock Rate Up to 75 MHz
- Package
  - 491-pin BGA Package (17x17 mm) (ZDN Suffix), 0.65-mm Ball Pitch with Via Channel Array Technology to Enable Low-Cost Routing

2.1.2. Functional Block Diagram



2.2. MEMORY

2.2.1. RAM

The VAR-SOM-AM43 is available with up to 8Gbit of DDR3 memory.

2.2.2. Non-volatile Storage Memory

2.2.3. NAND Flash

The VAR-SOM-AM43 is available with up to 512MB (4Gbit) of SLC NAND FLASH memory. The NAND flash is used for flash disk purposes, O.S. run-time-image and the bootloader (boot from NAND). First block (block address 00h) of the memory device is guaranteed to be valid without ECC (up to 1,000 PROGRAM/ERASE cycles).

2.2.4. eMMC

The VAR-SOM-AM43 is available with up to Up to 32GB of storage.

2.2.5. EEPROM

The VAR-SOM-AM43 is available with a 4KB, I2C EEPROM (I2C0) for future revisions.

2.3. 10/100/1000 Mbps Ethernet Transceiver

The VAR-SOM-AM43 can be ordered with an Integrated Ethernet Transceiver,

Qualcomm Atheros AR8033 or Analog Devices ADIN1300.

Please contact sales@variscite.com for inquiries about P/N assembled on your SOM.

2.3.1. Qualcomm Atheros AR8033 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- 1000BASE-T PCS and auto-negotiation with next page support
- Green ETHOS power saving modes with internal automatic DSP power saving scheme
- IEEE 802.3az EEE
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Robust operation over up to 140 meters of CAT5 cable
- Automatic Channel Swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction IEEE 802.3u compliant auto-negotiation

- Jumbo frame supports up to 10 KB (full-duplex)
- Integrated termination circuitry at the line side

2.3.2. Analog Devices ADIN1300 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.
- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover
- Autonegotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

2.4. Audio codec via the TLV320AIC3106

The Texas Instrument's TLV320AIC3106 is a low-power, highly integrated stereo audio codec. Extensive register-based power control is included, enabling stereo 48-kHz DAC playback as low as 15mW. VAR-SOM-AM43 exposes most of the audio interfaces of the TLV320AIC3106.

• Stereo Audio DAC
  - 102-dBA Signal-to-Noise Ratio
  - 16/20/24/32-Bit Data
  - Supports Rates From 8 kHz to 96 kHz
  - 3D/Bass/Treble/EQ/De-Emphasis Effects

• Stereo Audio ADC
  - 92-dBA Signal-to-Noise Ratio
  - Supports Rates From 8 kHz to 96 kHz
  - Digital Signal Processing and Noise Filtering Available During Record

• Programmable Input/output Analog Gains
• Automatic Gain Control (AGC) for Record
• Programmable Microphone Bias Level
• Concurrent Digital Microphone and Analog Microphone Support Available

2.5. Wi-Fi & Bluetooth

The VAR-SOM-AM43 contains a certified high performance WL183xMOD 2.4/5 GHz IEEE 802.11 a/b/g/n Bluetooth 5.1/BLE with CSA2 support radio module, with optional Dual Band and MIMO support.
Features:

- WLAN With Integrated RF Front-End Module (FEM), Power Amplifier (PA), Crystal, RF Switches, Filters, Passives, and Power Management on a Single Module
- Wi-Fi-*Bluetooth* Single Antenna Coexistence
- Dual-Mode *Bluetooth* and *Bluetooth* Low Energy
- HCI Transport for *Bluetooth* over UART and SDIO for WLAN
- Temperature Compensation Mechanism to Ensure Minimal Variation in RF Performance Over the Entire Temperature Range
- WLAN Baseband Processor and RF Transceiver Supporting IEEE Std 802.11a, 802.11b, 802.11g, and 802.11n
- Supports 4-Bit SDIO Host Interface Including High-Speed (HS) and V3 Modes
- Optional 2x2 MIMO and 40-MHz Channels for High Throughput
- Wi-Fi Direct Concurrent Operation (Multi-Channel, Multi-Role)
- Support of *Bluetooth* 5.1 as well as CSA2
- Includes Concurrent Operation and Built-In Coexisting and Prioritization Handling of *Bluetooth*-BLE and WLAN
- Dedicated Audio Processor Supporting SBC Encoding + A2DP
- Up to 100-Mbps Throughput and Up to 1.4X the Range Versus a Single Antenna Configuration With 2X2 MIMO, 40-MHz Channel Bandwidth and MRC
- Lowest Wi-Fi Power Consumption in Connected Idle (< 800 uA)

2.6. TPS65218 PMIC

The Texas Instrument's TPS65218 is an integrated power-management IC dedicated to applications processors as the AM437x. The device provides:

BATTERY BACKUP SUPPLIES

- Two low-quiescent current, high efficiency step-down converters for battery backup domain
  - DCDC5: 1.0V output
  - DCDC6: 1.8V output
- VIN range from 2.2V to 5.5V
- Can be 7supplied from system power or coin-cell backup battery

BUCK CONVERTERS (DCDC1, 2, 3)

- Three adjustable step-down converter with integrated switching FETs
  - DCDC1 : 1.1V default up to 1.8A (Core)
  - DCDC2 : 1.1V default up to 1.8A (MPU)
  - DCDC3 : 1.2V default up to 1.8A (DDR)
- VIN range from 2.7V to 5.5V
- Adjustable output voltage range 0.85V-3.5V
- 100% Duty Cycle for Lowest Dropout

LOW VOLTAGE LOAD SWITCH (LS1)

- VIN range from 1.2V to 3.3V
- 350mA current limit
- 110m□ (max) switch impedance @ 1.35V

HIGH-VOLTAGE LOAD SWITCH (LS3)

- VIN range from 1.8V to 10.0V
- 100mA / 500mA selectable current limit
- 500m□ (max) switch impedance

SUPERVISOR

- Built-in supervisor function monitors
  - DCDC1, DCDC2, DCDC3 to +/-4%
  - DCDC4 and LDO1 to +/-5%

PROTECTION / DIAGNOSTICS / CONTROL

- Under voltage lockout
- Over temperature warning / shutdown
- Always-on push-button monitor
- Separate power-good output for backup and main supplies
- Open-drain interrupt output pin
- User programmable default voltages and power sequencing
- I2C interface (Address 0x24h)

TPS65218 features are utilized internally by the VAR-SOM-AM43 and are not exposed to the VAR-SOM-AM43 204 pin connector.

3. External Connectors

The VAR-SOM-AM43 exposes a 204-pin, DDR3 SODIMM mechanical standard interface. Recommended Mating connector for baseboard interfacing is JAE MM80-204B1-1 or TE Connectivity 2-2013289-1or equivalent.

Pin#:
Pin Number on the SO-DIMM204 connector
Pin Name:
Default VAR- SOM-AM43 Pin Name

Type:
Pin Type & Description:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin
- PD- Internal Pull Down
- PU - internal pull up

Pin Group:
Pin functionality group

AM437x Ball:
AM437x ball number

Mode (Tables 3.2 & 3.4):
AM437x PinMux mode option

3.1. SoM Connector Pin-out

Pin#	Pin Name	Type	Pin Group / Function	Ball#
1	RGMII2_TD0[1] [7]	O	RGMII Transmit Data bit 0	E7
2	UART3_TXD_CON [1] [5]	O	UART Transmit Data	H24
3	RGMII2_TD1[1] [7]	O	RGMII Transmit Data bit 1	D7
4	UART3_RXD_CON [1] [5]	I	UART Receive Data	H25
5	RGMII2_TD2[1] [7]	O	RGMII Transmit Data bit 2	A4
6	UART3_RTS_CON [1] [5]	O	UART Request to Send	K24
7	RGMII2_TD3[1] [7]	O	RGMII Transmit Data bit 3	C6
8	UART3_CTS_CON [1] [5]	I	UART Clear to Send	H22
9	RGMII2_TCLK[1] [7]	O	RGMII Transmit Clock	E8
10	GND	Power	Digital GND	
11	RGMII2_TCTL[1] [7]	O	RGMII Transmit Control	C3
12	RGMII2_RCLK[1] [7]	I	RGMII Receive Clock	F6
13	CAM1_PCLK	I	CAMERA1 Data Pixel Clock	AE21
14	RGMII2_RCTL[1] [7]	I	RGMII Receive Control	C5
15	CAM1_DATA7	I	CAMERA1 data bus	AE24
16	RGMII2_RD0[1] [7]	I	RGMII Receive Data bit 0	D8
17	CAM1_HSYNC	I	CAMERA1 Data Horizontal Detect	AD25
18	RGMII2_RD1[1] [7]	I	RGMII Receive Data bit 1	G8
19	GND	Power	Digital GND	
20	RGMII2_RD2[1] [7]	I	RGMII Receive Data bit 2	B4
21	CAM1_DATA6	I	CAMERA1 data bus	AD23
22	RGMII2_RD3[1] [7]	I	RGMII Receive Data bit 3	F7
23	CAM1_DATA5	I	CAMERA1 data bus	AE23
24	GND	Power	Digital GND	
25	CAM1_WEN_GPIO4_13	I	CAMERA1 Data Write Enable	AB25
26	CAM1_VSYNC	I/O	CAMERA1 Data Vertical Detect	AC23
27	CAM1_FIELD_GPIO4_12	I	CAMERA1 Data Field Indicator	AC25
28	CAM1_DATA4	I	CAMERA1 data bus	AD22
29	GND	Power	Digital GND	
30	CAM1_DATA3	I	CAMERA1 data bus	AE22
31	MDI_A_P	I/ODS	Media-dependent interface 0, Plus	AR8033.11/ ADIN1300.12
32	CAM1_DATA9	I	CAMERA1 data bus	AE18
33	MDI_A_M	I/ODS	Media-dependent interface 0, Minus	AR8033.12/ ADIN1300.13
34	CAM1_DATA2	I	CAMERA1 data bus	AD21
35	GND	Power	Digital GND	
36	CAM1_DATA1	I	CAMERA1 data bus	AC21

37	MDI_B_P	I/ODS	Media-dependent interface 1, Plus	AR8033.14/ ADIN1300.14
38	CAM1_DATA0	I	CAMERA1 data bus	AB20
39	MDI_B_M	I/ODS	Media-dependent interface 1, Minus	AR8033.15/ ADIN1300.15
40	ETH_MDIO_CLK[6]	O	MII Management CLK	B17
41	GND	Power	Digital GND	
42	ETH_MDIO_DATA[6]	I/O	MII Management DATA	A17
43	MDI_C_P	I/ODS	Media-dependent interface 2, Plus	AR8033.17/ ADIN1300.16
44	GND	Power	Digital GND	
45	MDI_C_M	I/ODS	Media-dependent interface 2, Minus	AR8033.18/ ADIN1300.17
46	CAM1_DATA8	I	CAMERA1 data bus	AB18
47	GND	Power	Digital GND	
48	CAM1_DATA10	I	CAMERA1 data bus	Y18
49	MDI_D_P	I/ODS	Media-dependent interface 3, Plus	AR8033.20/ ADIN1300.18
50	CAM1_DATA11	I	CAMERA1 data bus	AA18
51	MDI_D_M	I/ODS	Media-dependent interface 3, Minus	AR8033.21/ ADIN1300.19
52	AM437X_MMC0_SDCD	I	MMC/SD/SDIO Card Detect	R25
53	GND	Power	Digital GND	
54	MCASP0_ACLKX_SPI1_SCLK	I/O	McASP0 Transmit Bit Clock	N24
55	LED_ACT	O	LED output for 10/100/1000 BASE-T activity	AR8033.23/ ADIN1300.21 (via inv. FET)
56	GPIO5_4	I/O	Digital Input/Output	P25
57	LED_LINK_1000	O	LED output for 1000 BASE-T link	AR8033.24/ ADIN1300.26
58	MCASP0_AHCLKR_SPI1_CS0	I/O	McASP0 Receive Master Clock	M24
59	LED_LINK_10_100	O	LED output for 10/100 BASE-T link	AR8033.26/ ADIN1300 - GND
60	MCASP0_AHCLKX	I/O	McASP0 Transmit Master Clock	L24
61	UART0_CTSN	I	UART Clear to Send	L25
62	MCASP0_AXR1	I/O	McASP0 Serial Data (IN/OUT)	M25
63	AM437X_USB0_VBUS_DET	I	USB0 OTG VBUS Detect Input	F24
64	UART0_RTSN	O	UART Request to Send	J25
65	AM437X_USB1_DRVVBUS	O	USB1 DRIVER ENABLE	F25
66	UART0_RXD	I	UART Receive Data	K25
67	UART0_TXD	O	UART Transmit Data	J24
68	AM437X_LCD_BACKLIGHT	O	LCD BACKLIGHT PWM	G24
69	I2C1_SDA	I/O	I2C1 Data	T21
70	I2C1_SCL	I/O	I2C1 Clock	T20
71	UART2_TXD_GPIO0_3	O	UART Transmit Data	T22

72	GND	Power	Digital GND	
73	AM437X_LCD_HSYNC[3]	O	LCD horizontal sync	A23
74	AM437X_LCD_VSYNC[3]	O	LCD vertical sync	B23
75	AM437X_LCD_DATA0[3]	O	LCD data	B22
76	AM437X_LCD_AC_BIAS_EN	O	LCD AC bias enable	A24
77	AM437X_LCD_DATA2[3]	O	LCD data	B21
78	AM437X_LCD_PCLK	O	LCD pixel clock	A22
79	AM437X_LCD_DATA5[3]	O	LCD data	B20
80	AM437X_LCD_DATA1[3]	O	LCD data	A21
81	AM437X_LCD_DATA9[3]	O	LCD data	B19
82	AM437X_LCD_DATA4[3]	O	LCD data	A20
83	SPI2_CS0	I/O	SPI Chip Select	T23
84	SPI2_D0	I/O	SPI Data	P22
85	GND	Power	Digital GND	
86	UART2_RXD _GPIO0_2	I	UART Receive Data	P23
87	AM437X_USB1_DP	I/ODS	USB_DIFF	V24
88	AM437X_USB0_ID	I	USB0 OTG ID	U24
89	AM437X_USB1_DM	I/ODS	USB_DIFF	V25
90	SPI2_D1	I/O	SPI Data	P20
91	AM437X_USB1_VBUS	Power	USB1 VBUS	T25
92	MCASP0_FSX/SPI1_D0	I/O	McASP0 Transmit Frame Sync	N22
93	GND	Power	Digital GND	
94	SPI2_SCLK	I/O	SPI Clock	N20
95	AM437X_USB0_DP	I/ODS	USB0 OTG Data Pair	W25
96	GND	Power	Digital GND	
97	AM437X_USB0_DM	I/ODS	USB0 OTG Data Pair	W24
98	AM437X_USB0_DRVVBUS	O	USB0 OTG DRIVER ENABLE	G21
99	AM437X_USB0_VBUS	Power	USB0 OTG VBUS	U23
100	VBAT_3P3V	Power	SOM Power Supply Input	
101	GND	Power	Digital GND	
102	VBAT_3P3V	Power	SOM Power Supply Input	
103	VBAT_3P3V	Power	SOM Power Supply Input	
104	VBAT_3P3V	Power	SOM Power Supply Input	
105	VBAT_3P3V	Power	SOM Power Supply Input	
106	GND	Power	Digital GND	
107	VBAT_3P3V	Power	SOM Power Supply Input	
108	GND	Power	Digital GND	
109	GPIO2_5[4]	I/O	General Purpose Input output (see note [4])	C10
110	VDDA_ADC	Power	ADC0 Power supply Output 1.8V	AB12

111	AM437X_DCAN1_TX	I/O	CAN1 Transmit	K21
112	GNDA_ADC	Power	ADC0 Analog Ground	AC15
113				
114	GPIO5_8	I/O	General Purpose Input output	D25
115	GPIO5_13	I/O	General Purpose Input output	E24
116	GPIO1_12[7]	I/O	General Purpose Input output	E11
117	MCASP0_ACLKR	I/O	McASP0 Receive Bit Clock	L23
118	GND	Power	Digital GND	GND
119	AM437X_DCAN1_RX	I/O	CAN1 Receive	L21
120	AM437X_DCAN0_RX	I/O	CAN0 Receive	L22
121	GND	Power	Digital GND	
122	MCASP0_FSR	I/O	McASP0 Receive Frame Sync	K23
123	AM437X_LCD_DATA10[3]	O	LCD data	A18
124	AM437X_DCAN0_TX	I/O	CAN0 Transmit	K22
125	MCASP0_AXR0/SPI1_D1	I/O	McASP0 Serial Data (IN/OUT)	H23
126	AM437X_LCD_DATA8[3]	O	LCD data	A19
127	AM437X_LCD_DATA6[3]	O	LCD data	C20
128	AM437X_LCD_DATA7[3]	O	LCD data	E19
129	AM437X_LCD_DATA11[3]	O	LCD data	B18
130	GND	Power	Digital GND	
131	GPIO0_30[4] [7]	I/O	General Purpose Input output (see notes [4] [7])	A2
132	AM437X_LCD_DATA3[3]	O	LCD data	C21
133	AM437X_LCD_DATA13[3]	O	LCD data	D19
134	VDDSHV11	Power	Power Domain VDDSHV9 and VDDSHV11	
135	GPIO1_14[7]	I/O	General Purpose Input output	B11
136	AM437X_AIN5	A	Analog input	AC13
137	GPIO1_15[7]	I/O	General Purpose Input output	A11
138	GPIO2_3[4]	I/O	General Purpose Input output (see note [4])	E10
139	AM437X_MMC0_DAT1	I/O	MMC/SD/SDIO data bus	C2
140	AM437X_MMC0_DAT2	I/O	MMC/SD/SDIO data bus	B2
141	AM437X_MMC0_CLK	O	MMC/SD/SDIO clock	D1
142	AM437X_LCD_DATA12[3]	O	LCD data	C19
143	AM437X_MMC0_DAT3	I/O	MMC/SD/SDIO data bus	B1
144	AM437X_LCD_DATA15[3]	O	LCD data	D17
145	AM437X_MMC0_CMD	I/O	MMC/SD/SDIO command	D2
146	AM437X_LCD_DATA14[3]	O	LCD data	C17
147	AM437X_MMC0_DAT0	I/O	MMC/SD/SDIO data bus	C1
148	GPIO5_5	I/O	General Purpose Input output	R24
149	GPIO5_6	I/O	General Purpose Input output	P24

150	GPIO1_13[7]	I/O	General Purpose Input output	C11
151	GPIO0_31[4] [7]	I/O	General Purpose Input output (see notes [4] [7])	B3
152	AM437X_AIN2	A	Touch screen Y plus / analog I	Y13
153	MIC_IN_L	AI	MIC3 input	11
154	GPIO2_2[4]	I/O	General Purpose Input output (see note [4])	A9
155	AM437X_AIN1	A	Touch screen X minus / analog I	Y12
156	AM437X_AIN6	A	Analog input	AD13
157	MICDET	I	Microphone detect	12
158	AM437X_AIN3	A	Touch screen Y minus / analog I	AA13
159	MICBIAS	O	Microphone bias voltage output	13
160	AM437X_AIN0	A	Touch screen X plus / analog I	AA12
161	MIC_IN_R	AI	MIC3 input	14
162	AM437X_AIN4	A	Analog input	AB13
163	AM437X_AIN7	A	Analog input	AE13
164	ADC0_VREFP	AI	Analog Positive Reference Input	AD14
165	GND	Power	Digital GND	
166	ADC0_VREFN	AI	Analog Negative Reference Input	AE14
167	GPIO2_4[4]	I/O	General Purpose Input output (see note [4])	D10
168	LINEIN_RP	AI	AUDIO Line Input Right	5
169	GPIO1_7[4]	I/O	General Purpose Input output (see note [4])	B8
170	AGND_AUD	Power	Audio Ground	
171	LOWPWR_RSTN	O	RESET OUTPUT build by pins Y23 & H20	
172	LINEIN_LP	AI	AUDIO Line Input Left	3
173	GPIO4_8	I/O	Digital Input/Output	AD24
174	LINEOUT_RP	AO	AUDIO Line Output Right	31
175	AM437X_PORZN	I/O	Power On Reset	Y23
176	LINEOUT_LP	AO	AUDIO Line Output Left	29
177	GPIO1_4[4]	I/O	General Purpose Input output (see note [4])	B7
178	DMIC_CLK	O	Digital Microphone CLK	
179	AM437X_LCD_DATA16	O	LCD data	AC24
180	DMIC_DATA	I/O	Digital Microphone DATA	
181	GPIO1_5[4]	I/O	General Purpose Input output (see note [4])	A7
182	I2C0_SCL[2]	I/O	I2C0 Clock	Y22
183	GPIO1_6[4]	I/O	General Purpose Input output (see note [4])	C8
184	I2C0_SDA[2]	I/O	I2C0 Data	AB24
185	GND	Power	Digital GND	
186	AM437X_LCD_DATA21	O	LCD data	AC18
187	AM437X_LCD_DATA19	O	LCD data	AC20
188	AM437X_LCD_DATA17	O	LCD data	AA19

189	GPIO1_3[4]	I/O	General Purpose Input output (see note [4])	A6
190	GPIO4_28	I/O	Digital Input/Output	AE20
191	GPIO1_2[4]	I/O	General Purpose Input output (see note [4])	B6
192	GPIO4_29	I/O	Digital Input/Output	AD20
193	GPIO1_1[4]	I/O	General Purpose Input output (see note [4])	A5
194	GPIO4_26	I/O	Digital Input/Output	AE19
195	GPIO1_0[4]	I/O	General Purpose Input output (see note [4])	B5
196	GPIO4_27	I/O	Digital Input/Output	AD19
197	AM437X_LCD_DATA22	O	LCD data	AD18
198	AM437X_LCD_DATA18	O	LCD data	AB19
199	AM437X_LCD_DATA23	O	LCD data	AE17
200	GND	Power	Digital GND	
201	AM437X_LCD_DATA20	O	LCD data	AD17
202	GND	Power	Digital GND	
203	GND	Power	Digital GND	
204	GND	Power	Digital GND	

Notes:

1. Pins are used internally by on SOM WiFi/BT module. Pins are exposed and can be used on SOM without WiFi/BT module mounted.

2. I2C0 is internally used by PMIC (0x24h), AUDIO CODEC IC (0x1Bh) and EEPROM IC (0x50h, 0x51h).

Pin function cannot be altered

3. LCD signals are sampled on POR for selecting System boot configurations.

4. GPMC Bus signal internally used by NAND flash. Can be configured and used as GPIO only if NAND flash is not mounted.

5. UART3 is used by on SOM Bluetooth. Interface can be exported from these pins on SOM without WiFi/BT module mounted. Interface can be exported from other pins only if Bluetooth is disabled.

6. ETH_MDIO_CLK / ETH_MDIO_DATA signals are internally used by on-SOM 10/100/1000 Ethernet PHY. Do not alter pins functionality if Ethernet PHY is mounted.

7. Pin is referenced to 1.8V rail.

3.2. SO-DIMM 204 Pin Mux

The table below summarizes the additional available functionality for each pin in the SO-DIMM 200 connector.

Pin NUMBER	BALL NUMBER	SIGNAL NAME	MODE
1	E7	gpmc_a5	0x0
		gmii2_txd0	0x1
		rgmii2_td0	0x2
		rmii2_txd0	0x3
		gpmc_a21	0x4
		pr1_mii1_txd0	0x5
		eQEP1B_in	0x6
		gpio1_21	0x7
2	H24	uart3_txd	0x0
		pr0_pru0_gpo19	0x4
		pr0_pru0_gpi19	0x5
		ehrpwm4B	0x6
		gpio5_3	0x7
3	D7	gpmc_a4	0x0
		gmii2_txd1	0x1
		rgmii2_td1	0x2
		rmii2_txd1	0x3
		gpmc_a20	0x4
		pr1_mii1_txd1	0x5
		eQEP1A_in	0x6
		gpio1_20	0x7
4	H25	uart3_rxd	0x0
		pr0_pru0_gpo18	0x4
		pr0_pru0_gpi18	0x5
		ehrpwm4A	0x6
		gpio5_2	0x7
5	A4	gpmc_a3	0x0
		gmii2_txd2	0x1
		rgmii2_td2	0x2
		mmc2_dat2	0x3
		gpmc_a19	0x4
		pr1_mii1_txd2	0x5
		ehrpwm1B	0x6
		gpio1_19	0x7
6	K24	uart3_rtsn	0x0
		hdq_sio	0x1

		pr0_pru1_gpo19	0x4
		pr0_pru1_gpi19	0x5
		ehrpwm5B	0x6
		gpio5_1	0x7
7	C6	gpmc_a2	0x0
		gmii2_txd3	0x1
		rgmii2_td3	0x2
		mmc2_dat1	0x3
		gpmc_a18	0x4
		pr1_mii1_txd3	0x5
		ehrpwm1A	0x6
		gpio1_18	0x7
8	H22	uart3_ctsn	0x0
		spi4_cs1	0x2
		pr0_pru1_gpo18	0x4
		pr0_pru1_gpi18	0x5
		ehrpwm5A	0x6
		gpio5_0	0x7
9	E8	gpmc_a6	0x0
		gmii2_txclk	0x1
		rgmii2_tclk	0x2
		mmc2_dat4	0x3
		gpmc_a22	0x4
		pr1_mii_mt1_clk	0x5
		eQEP1_index	0x6
		gpio1_22	0x7
11	C3	gpmc_a0	0x0
		gmii2_txen	0x1
		rgmii2_tctl	0x2
		rmii2_txen	0x3
		gpmc_a16	0x4
		pr1_mii1_txen	0x5
		ehrpwm1_tripzone_input	0x6
		gpio1_16	0x7
12	F6	gpmc_a7	0x0
		gmii2_rxclk	0x1
		rgmii2_rclk	0x2
		mmc2_dat5	0x3
		gpmc_a23	0x4
		pr1_mii_mr1_clk	0x5
		eQEP1_strobe	0x6

		gpio1_23	0x7
13	AE21	cam1_pclk	0x0
		xdma_event_intr6	0x1
		spi1_cs3	0x2
		pr0_pru1_gpo3	0x3
		spi2_sclk	0x4
		pr0_pru1_gpi3	0x5
		ehrpwm1A	0x6
		gpio4_11	0x7
14	C5	gpmc_a1	0x0
		gmii2_rxdv	0x1
		rgmii2_rctl	0x2
		mmc2_dat0	0x3
		gpmc_a17	0x4
		pr1_mii1_rxdv	0x5
		ehrpwm0_synco	0x6
		gpio1_17	0x7
15	AE24	cam1_data7	0x0
		uart1_dtrn	0x1
		uart2_rtsn	0x2
		mmc2_dat3	0x3
		pr0_pru1_gpo15	0x4
		pr0_pru1_gpi15	0x5
		pr1_edio_data_in1	0x6
		gpio4_21	0x7
16	D8	gpmc_a11	0x0
		gmii2_rxd0	0x1
		rgmii2_rd0	0x2
		rmii2_rxd0	0x3
		gpmc_a27	0x4
		pr1_mii1_rxd0	0x5
		mcasp0_axr1	0x6
		gpio1_27	0x7
17	AD25	cam1_hd	0x0
		xdma_event_intr4	0x1
		spi0_cs3	0x2
		pr0_pru1_gpo1	0x3
		spi2_cs0	0x4
		pr0_pru1_gpi1	0x5
		ehrpwm0A	0x6
		gpio4_9	0x7

18	G8	gpmc_a10	0x0
		gmii2_rxd1	0x1
		rgmii2_rd1	0x2
		rmii2_rxd1	0x3
		gpmc_a26	0x4
		pr1_mii1_rxd1	0x5
		mcasp0_axr0	0x6
		gpio1_26	0x7
20	B4	gpmc_a9	0x0
		gmii2_rxd2	0x1
		rgmii2_rd2	0x2
		mmc2_dat7	0x3
		gpmc_a25	0x4
		pr1_mii1_rxd2	0x5
		mcasp0_fsx	0x6
		gpio1_25	0x7
		rmii2_crs_dv	0x8
21	AD23	cam1_data6	0x0
		uart1_dcdn	0x1
		uart2_ctsn	0x2
		mmc2_dat2	0x3
		pr0_pru1_gpo14	0x4
		pr0_pru1_gpi14	0x5
		pr1_edio_data_in0	0x6
		gpio4_20	0x7
22	F7	gpmc_a8	0x0
		gmii2_rxd3	0x1
		rgmii2_rd3	0x2
		mmc2_dat6	0x3
		gpmc_a24	0x4
		pr1_mii1_rxd3	0x5
		mcasp0_aclkx	0x6
		gpio1_24	0x7
23	AE23	cam1_data5	0x0
		uart1_dsrn	0x1
		uart2_txd	0x2
		mmc2_dat1	0x3
		pr0_pru1_gpo13	0x4
		pr0_pru1_gpi13	0x5
		pr1_edio_latch_in	0x6
		gpio4_19	0x7

25	AB25	cam1_wen	0x0
		xdma_event_intr8	0x1
		pr1_edio_sof	0x2
		cam0_data11	0x3
		spi2_d1	0x4
		cam1_data11	0x5
		EMU11	0x6
		gpio4_13	0x7
		ehrpwm3B	0x8
26	AC23	cam1_vd	0x0
		xdma_event_intr5	0x1
		spi1_cs2	0x2
		pr0_pru1_gpo2	0x3
		spi2_cs2	0x4
		pr0_pru1_gpi2	0x5
		ehrpwm0B	0x6
		gpio4_10	0x7
27	AC25	cam1_field	0x0
		xdma_event_intr7	0x1
		ext_hw_trigger	0x2
		cam0_data10	0x3
		spi2_cs1	0x4
		cam1_data10	0x5
		ehrpwm1B	0x6
		gpio4_12	0x7
		ehrpwm3A	0x8
28	AD22	cam1_data4	0x0
		uart1_rin	0x1
		uart2_rxd	0x2
		mmc2_dat0	0x3
		pr0_pru1_gpo12	0x4
		pr0_pru1_gpi12	0x5
		pr1_edc_latch1_in	0x6
		gpio4_18	0x7
		uart0_dcdn	0x8
30	AE22	cam1_data3	0x0
		uart1_rtsn	0x1
		spi3_sclk	0x2
		mmc2_cmd	0x3
		pr0_pru1_gpo11	0x4
		pr0_pru1_gpi11	0x5

		pr1_edc_latch0_in	0x6
		gpio4_17	0x7
32	AE18	cam0_data0	0x0
		cam1_data9	0x2
		I2C1_SDA	0x3
		pr0_pru1_gpo16	0x4
		pr0_pru1_gpi16	0x5
		ehrpwm0_synco	0x6
		gpio5_19	0x7
34	AD21	cam1_data2	0x0
		uart1_ctsn	0x1
		spi3_cs0	0x2
		mmc2_clk	0x3
		pr0_pru1_gpo10	0x4
		pr0_pru1_gpi10	0x5
		ehrpwm1_tripzone_input	0x6
		gpio4_16	0x7
36	AC21	cam1_data1	0x0
		uart1_txd	0x1
		spi3_d1	0x2
		I2C2_SCL	0x3
		ehrpwm0_synci	0x6
		gpio4_15	0x7
38	AB20	cam1_data0	0x0
		uart1_rxd	0x1
		spi3_d0	0x2
		I2C2_SDA	0x3
		ehrpwm0_tripzone_input	0x6
		gpio4_14	0x7
40	B17	mdio_clk	0x0
		timer5	0x1
		uart5_txd	0x2
		uart3_rtsn	0x3
		mmc0_sdwp	0x4
		mmc1_clk	0x5
		mmc2_clk	0x6
		gpio0_1	0x7
		pr1_mdio_mdclk	0x8
42	A17	mdio_data	0x0
		timer6	0x1
		uart5_rxd	0x2

		uart3_ctsn	0x3
		mmc0_sdcd	0x4
		mmc1_cmd	0x5
		mmc2_cmd	0x6
		gpio0_0	0x7
		pr1_mdio_data	0x8
46	AB18	cam0_data1	0x0
		cam1_data8	0x2
		I2C1_SCL	0x3
		pr0_pru1_gpo17	0x4
		pr0_pru1_gpi17	0x5
		ehrpwm3_synco	0x6
		gpio5_20	0x7
48	Y18	cam0_data2	0x0
		mmc1_clk	0x1
		cam1_data10	0x2
		qspi_clk	0x3
		gpio4_24	0x7
50	AA18	cam0_data3	0x0
		mmc1_cmd	0x1
		cam1_data11	0x2
		qspi_csn	0x3
		gpio4_25	0x7
52	R25	spi0_cs1	0x0
		uart3_rxd	0x1
		eCAP1_in_PWM1_out	0x2
		mmc0_pow	0x3
		xdma_event_intr2	0x4
		mmc0_sdcd	0x5
		EMU4	0x6
		gpio0_6	0x7
		ehrpwm2A	0x8
		timer0	0x9
54	N24	mcasp0_aclkx	0x0
		ehrpwm0A	0x1
		spi0_cs3	0x2
		spi1_sclk	0x3
		mmc0_sdcd	0x4
		pr0_pru0_gpo0	0x5
		pr0_pru0_gpi0	0x6
		gpio3_14	0x7

56	P25	spi4_sclk	0x0
		ehrpwm0_synci	0x6
		gpio5_4	0x7
58	M24	mcasp0_ahclkr	0x0
		ehrpwm0_synci	0x1
		mcasp0_axr2	0x2
		spi1_cs0	0x3
		eCAP2_in_PWM2_out	0x4
		pr0_pru0_gpo3	0x5
		pr0_pru0_gpi3	0x6
		gpio3_17	0x7
60	L24	mcasp0_ahclkx	0x0
		eQEP0_strobe	0x1
		mcasp0_axr3	0x2
		mcasp1_axr1	0x3
		EMU4	0x4
		pr0_pru0_gpo7	0x5
		pr0_pru0_gpi7	0x6
		gpio3_21	0x7
		gpio0_3	0x9
61	L25	uart0_ctsn	0x0
		uart4_rxd	0x1
		dcan1_tx	0x2
		I2C1_SDA	0x3
		spi1_d0	0x4
		timer7	0x5
		pr1_edc_sync0_out	0x6
		gpio1_8	0x7
62	M25	mcasp0_axr1	0x0
		eQEP0_index	0x1
		mcasp1_axr0	0x3
		EMU3	0x4
		pr0_pru0_gpo6	0x5
		pr0_pru0_gpi6	0x6
		gpio3_20	0x7
		gpio0_2	0x9
63	F24	pr1_mii1_col	0x5
		gpio5_9	0x7
64	J25	uart0_rtsn	0x0
		uart4_txd	0x1
		dcan1_rx	0x2

		I2C1_SCL	0x3
		spi1_d1	0x4
		spi1_cs0	0x5
		pr1_edc_sync1_out	0x6
		gpio1_9	0x7
65	F25	USB1_DRVVBUS	0x0
		gpio3_13	0x7
		gpio0_25	0x9
66	K25	uart0_rxd	0x0
		spi1_cs0	0x1
		dcan0_tx	0x2
		I2C2_SDA	0x3
		eCAP2_in_PWM2_out	0x4
		pr0_pru1_gpo4	0x5
		pr0_pru1_gpi4	0x6
		gpio1_10	0x7
67	J24	uart0_txd	0x0
		spi1_cs1	0x1
		dcan0_rx	0x2
		I2C2_SCL	0x3
		eCAP1_in_PWM1_out	0x4
		pr0_pru1_gpo5	0x5
		pr0_pru1_gpi5	0x6
		gpio1_11	0x7
68	G24	eCAP0_in_PWM0_out	0x0
		uart3_txd	0x1
		spi1_cs1	0x2
		pr1_ecap0_ecap_capin_apwm_o	0x3
		spi1_sclk	0x4
		mmc0_sdwp	0x5
		xdma_event_intr2	0x6
		gpio0_7	0x7
		ehrpwm2B	0x8
		timer1	0x9
69	T21	spi0_d1	0x0
		mmc1_sdwp	0x1
		I2C1_SDA	0x2
		ehrpwm0_tripzone_input	0x3
		pr1_uart0_rxd	0x4
		pr0_uart0_rxd	0x5
		pr1_edio_data_out0	0x6

		gpio0_4	0x7
		ehrpwm1A	0x8
70	T20	spi0_cs0	0x0
		mmc2_sdwp	0x1
		I2C1_SCL	0x2
		ehrpwm0_synci	0x3
		pr1_uart0_txd	0x4
		pr0_uart0_txd	0x5
		pr1_edio_data_out1	0x6
		gpio0_5	0x7
		ehrpwm1B	0x8
71	T22	spi0_d0	0x0
		uart2_txd	0x1
		I2C2_SCL	0x2
		ehrpwm0B	0x3
		pr1_uart0_rts_n	0x4
		pr0_uart0_rts_n	0x5
		EMU3	0x6
		gpio0_3	0x7
73	A23	dss_hsync	0x0
		gpmc_a9	0x1
		gpmc_a2	0x2
		pr1_edio_data_in3	0x3
		pr1_edio_data_out3	0x4
		pr0_pru1_gpo7	0x5
		pr0_pru1_gpi7	0x6
		gpio2_23	0x7
74	B23	dss_vsync	0x0
		gpmc_a8	0x1
		gpmc_a1	0x2
		pr1_edio_data_in2	0x3
		pr1_edio_data_out2	0x4
		pr0_pru1_gpo6	0x5
		pr0_pru1_gpi6	0x6
		gpio2_22	0x7
75	B22	dss_data0	0x0
		gpmc_a0	0x1
		pr1_mii_mt0_clk	0x2
		ehrpwm2A	0x3
		pr1_pru0_gpo0	0x5
		pr1_pru0_gpi0	0x6

		gpio2_6	0x7
76	A24	dss_ac_bias_en	0x0
		gpmc_a11	0x1
		gpmc_a4	0x2
		pr1_edio_data_in5	0x3
		pr1_edio_data_out5	0x4
		pr0_pru1_gpo9	0x5
		pr0_pru1_gpi9	0x6
		gpio2_25	0x7
77	B21	dss_data2	0x0
		gpmc_a2	0x1
		pr1_mii0_txd3	0x2
		ehrpwm2_tripzone_input	0x3
		pr1_pru0_gpo2	0x5
		pr1_pru0_gpi2	0x6
		gpio2_8	0x7
78	A22	dss_pclk	0x0
		gpmc_a10	0x1
		gpmc_a3	0x2
		pr1_edio_data_in4	0x3
		pr1_edio_data_out4	0x4
		pr0_pru1_gpo8	0x5
		pr0_pru1_gpi8	0x6
		gpio2_24	0x7
79	B20	dss_data5	0x0
		gpmc_a5	0x1
		pr1_mii0_txd0	0x2
		eQEP2B_in	0x3
		pr1_pru0_gpo5	0x5
		pr1_pru0_gpi5	0x6
		gpio2_11	0x7
80	A21	dss_data1	0x0
		gpmc_a1	0x1
		pr1_mii0_txen	0x2
		ehrpwm2B	0x3
		pr1_pru0_gpo1	0x5
		pr1_pru0_gpi1	0x6
		gpio2_7	0x7
81	B19	dss_data9	0x0
		gpmc_a13	0x1
		ehrpwm0_synco	0x2

		mcasp0_fsx	0x3
		uart5_rxd	0x4
		pr1_mii0_rxd2	0x5
		uart2_rtsn	0x6
		gpio2_15	0x7
82	A20	dss_data4	0x0
		gpmc_a4	0x1
		pr1_mii0_txd1	0x2
		eQEP2A_in	0x3
		pr1_pru0_gpo4	0x5
		pr1_pru0_gpi4	0x6
		gpio2_10	0x7
83	T23	spi2_cs0	0x0
		I2C1_SDA	0x1
		ehrpwm2_tripzone_input	0x6
		gpio3_25	0x7
		gpio0_23	0x9
84	P22	spi2_d0	0x0
		ehrpwm5_tripzone_input	0x6
		gpio3_22	0x7
		gpio0_20	0x9
86	P23	spi0_sclk	0x0
		uart2_rxd	0x1
		I2C2_SDA	0x2
		ehrpwm0A	0x3
		pr1_uart0_cts_n	0x4
		pr0_uart0_cts_n	0x5
		EMU2	0x6
		gpio0_2	0x7
90	P20	spi2_d1	0x0
		ehrpwm1_tripzone_input	0x6
		gpio3_23	0x7
		gpio0_21	0x9
92	N22	mcasp0_fsx	0x0
		ehrpwm0B	0x1
		spi1_cs2	0x2
		spi1_d0	0x3
		mmc1_sdcd	0x4
		pr0_pru0_gpo1	0x5
		pr0_pru0_gpi1	0x6
		gpio3_15	0x7

94	N20	spi2_sclk	0x0
		I2C1_SCL	0x1
		ehrpwm4_tripzone_input	0x6
		gpio3_24	0x7
		gpio0_22	0x9
98	G21	USB0_DRVVBUS	0x0
		gpio0_18	0x7
		gpio5_27	0x9
109	C10	gpmc_be0n_cle	0x0
		spi1_cs3	0x1
		timer5	0x2
		qspi_d3	0x3
		pr1_mii1_rxlink	0x4
		gpmc_a5	0x5
		spi3_cs1	0x6
		gpio2_5	0x7
111	K21	uart1_rxd	0x0
		mmc1_sdwp	0x1
		dcan1_tx	0x2
		I2C1_SDA	0x3
		pr1_uart0_rxd	0x5
		pr1_pru0_gpi16	0x6
		gpio0_14	0x7
114	D25	pr1_mii0_col	0x5
		gpio5_8	0x7
115	E24	pr1_mii1_rxlink	0x5
		gpio5_13	0x7
116	E11	gpmc_ad12	0x0
		dss_data19	0x1
		mmc1_dat4	0x2
		mmc2_dat0	0x3
		eQEP2A_in	0x4
		pr1_mii0_txd2	0x5
		pr1_pru0_gpi10	0x6
		gpio1_12	0x7
		mcasp0_aclkx	0x8
		pr1_pru0_gpo10	0x9
117	L23	mcasp0_aclkr	0x0
		eQEP0A_in	0x1
		mcasp0_axr2	0x2
		mcasp1_aclkx	0x3

		mmc0_sdwp	0x4
		pr0_pru0_gpo4	0x5
		pr0_pru0_gpi4	0x6
		gpio3_18	0x7
		gpio0_18	0x9
		gpio1_30	0x7
119	L21	uart1_txd	0x0
		mmc2_sdwp	0x1
		dcan1_rx	0x2
		I2C1_SCL	0x3
		pr1_uart0_txd	0x5
		pr1_pru0_gpi16	0x6
		gpio0_15	0x7
120	L22	uart1_rtsn	0x0
		timer5	0x1
		dcan0_rx	0x2
		I2C2_SCL	0x3
		spi1_cs1	0x4
		pr1_uart0_rts_n	0x5
		pr1_edc_latch1_in	0x6
		gpio0_13	0x7
122	K23	mcasp0_fsr	0x0
		eQEP0B_in	0x1
		mcasp0_axr3	0x2
		mcasp1_fsx	0x3
		EMU2	0x4
		pr0_pru0_gpo5	0x5
		pr0_pru0_gpi5	0x6
		gpio3_19	0x7
		gpio0_19	0x9
123	A18	dss_data10	0x0
		gpmc_a14	0x1
		ehrpwm1A	0x2
		mcasp0_axr0	0x3
		pr1_mii0_rxd1	0x5
		uart3_ctsn	0x6
		gpio2_16	0x7
124	K22	uart1_ctsn	0x0
		timer6	0x1
		dcan0_tx	0x2
		I2C2_SDA	0x3

		spi1_cs0	0x4
		pr1_uart0_cts_n	0x5
		pr1_edc_latch0_in	0x6
		gpio0_12	0x7
125	H23	mcasp0_axr0	0x0
		ehrpwm0_tripzone_input	0x1
		spi1_cs3	0x2
		spi1_d1	0x3
		mmc2_sdcd	0x4
		pr0_pru0_gpo2	0x5
		pr0_pru0_gpi2	0x6
		gpio3_16	0x7
126	A19	dss_data8	0x0
		gpmc_a12	0x1
		ehrpwm1_tripzone_input	0x2
		mcasp0_aclkx	0x3
		uart5_txd	0x4
		pr1_mii0_rxd3	0x5
		uart2_ctsn	0x6
		gpio2_14	0x7
127	C20	dss_data6	0x0
		gpmc_a6	0x1
		pr1_edio_data_in6	0x2
		eQEP2_index	0x3
		pr1_edio_data_out6	0x4
		pr1_pru0_gpo6	0x5
		pr1_pru0_gpi6	0x6
		gpio2_12	0x7
128	E19	dss_data7	0x0
		gpmc_a7	0x1
		pr1_edio_data_in7	0x2
		eQEP2_strobe	0x3
		pr1_edio_data_out7	0x4
		pr1_pru0_gpo7	0x5
		pr1_pru0_gpi7	0x6
		gpio2_13	0x7
129	B18	dss_data11	0x0
		gpmc_a15	0x1
		ehrpwm1B	0x2
		mcasp0_ahclkr	0x3
		mcasp0_axr2	0x4

		pr1_mii0_rxd0	0x5
		uart3_rtsn	0x6
		gpio2_17	0x7
		spi3_cs1	0x8
131	A2	gpmc_wait0	0x0
		gmii2_crs	0x1
		gpmc_csn4	0x2
		rmii2_crs_dv	0x3
		mmc1_sdcd	0x4
		pr1_mii1_crs	0x5
		uart4_rxd	0x6
		gpio0_30	0x7
		gpio5_30	0x9
132	C21	dss_data3	0x0
		gpmc_a3	0x1
		pr1_mii0_txd2	0x2
		ehrpwm0_synco	0x3
		pr1_pru0_gpo3	0x5
		pr1_pru0_gpi3	0x6
		gpio2_9	0x7
133	D19	dss_data13	0x0
		gpmc_a17	0x1
		eQEP1B_in	0x2
		mcasp0_fsr	0x3
		mcasp0_axr3	0x4
		pr1_mii0_rxer	0x5
		uart4_rtsn	0x6
		gpio0_9	0x7
		spi3_d0	0x8
135	B11	gpmc_ad14	0x0
		dss_data17	0x1
		mmc1_dat6	0x2
		mmc2_dat2	0x3
		eQEP2_index	0x4
		pr1_mii0_txd0	0x5
		pr1_pru0_gpi16	0x6
		gpio1_14	0x7
		mcasp0_axr0	0x8
137	A11	gpmc_ad15	0x0
		dss_data16	0x1
		mmc1_dat7	0x2

		mmc2_dat3	0x3
		eQEP2_strobe	0x4
		pr1_ecap0_ecap_capin_apwm_o	0x5
		gpio1_15	0x7
		mcasp0_axr1	0x8
		spi3_cs1	0x9
138	E10	gpmc_oen_ren	0x0
		spi0_cs2	0x1
		timer7	0x2
		qspi_d1	0x3
		gpio2_3	0x7
139	C2	mmc0_dat1	0x0
		gpmc_a22	0x1
		uart5_ctsn	0x2
		uart3_rxd	0x3
		uart1_dtrn	0x4
		pr0_pru0_gpo10	0x5
		pr0_pru0_gpi10	0x6
		gpio2_28	0x7
140	B2	mmc0_dat2	0x0
		gpmc_a21	0x1
		uart4_rtsn	0x2
		timer6	0x3
		uart1_dsrn	0x4
		pr0_pru0_gpo9	0x5
		pr0_pru0_gpi9	0x6
		gpio2_27	0x7
141	D1	mmc0_clk	0x0
		gpmc_a24	0x1
		uart3_ctsn	0x2
		uart2_rxd	0x3
		dcan1_tx	0x4
		pr0_pru0_gpo12	0x5
		pr0_pru0_gpi12	0x6
		gpio2_30	0x7
142	C19	dss_data12	0x0
		gpmc_a16	0x1
		eQEP1A_in	0x2
		mcasp0_aclkr	0x3
		mcasp0_axr2	0x4
		pr1_mii0_rxlink	0x5

		uart4_ctsn	0x6
		gpio0_8	0x7
		spi3_sclk	0x8
143	B1	mmc0_dat3	0x0
		gpmc_a20	0x1
		uart4_ctsn	0x2
		timer5	0x3
		uart1_dcdn	0x4
		pr0_pru0_gpo8	0x5
		pr0_pru0_gpi8	0x6
		gpio2_26	0x7
144	D17	dss_data15	0x0
		gpmc_a19	0x1
		eQEP1_strobe	0x2
		mcasp0_ahclkx	0x3
		mcasp0_axr3	0x4
		pr1_mii0_rxdv	0x5
		uart5_rtsn	0x6
		gpio0_11	0x7
		spi3_cs0	0x8
145	D2	mmc0_cmd	0x0
		gpmc_a25	0x1
		uart3_rtsn	0x2
		uart2_txd	0x3
		dcan1_rx	0x4
		pr0_pru0_gpo13	0x5
		pr0_pru0_gpi13	0x6
		gpio2_31	0x7
146	C17	dss_data14	0x0
		gpmc_a18	0x1
		eQEP1_index	0x2
		mcasp0_axr1	0x3
		uart5_rxd	0x4
		pr1_mii_mr0_clk	0x5
		uart5_ctsn	0x6
		gpio0_10	0x7
		spi3_d1	0x8
147	C1	mmc0_dat0	0x0
		gpmc_a23	0x1
		uart5_rtsn	0x2
		uart3_txd	0x3

		uart1_rin	0x4
		pr0_pru0_gpo11	0x5
		pr0_pru0_gpi11	0x6
		gpio2_29	0x7
148	R24	spi4_d0	0x0
		ehrpwm3_synci	0x6
		gpio5_5	0x7
149	P24	spi4_d1	0x0
		ehrpwm0_tripzone_input	0x6
		gpio5_6	0x7
150	C11	gpmc_ad13	0x0
		dss_data18	0x1
		mmc1_dat5	0x2
		mmc2_dat1	0x3
		eQEP2B_in	0x4
		pr1_mii0_txd1	0x5
		pr1_pru0_gpi11	0x6
		gpio1_13	0x7
		mcasp0_fsx	0x8
		pr1_pru0_gpo11	0x9
151	B3	gpmc_wpn	0x0
		gmii2_rxerr	0x1
		gpmc_csn5	0x2
		rmii2_rxerr	0x3
		mmc2_sdcd	0x4
		pr1_mii1_rxer	0x5
		uart4_txd	0x6
		gpio0_31	0x7
		gpio5_31	0x9
154	A9	gpmc_advn_ale	0x0
		spi0_cs3	0x1
		timer4	0x2
		qspi_d0	0x3
		gpio2_2	0x7
167	D10	gpmc_wen	0x0
		spi1_cs2	0x1
		timer6	0x2
		qspi_d2	0x3
		gpio2_4	0x7
169	B8	gpmc_ad7	0x0
		mmc1_dat7	0x1

		gpio1_7	0x7
173	AD24	cam1_data8	0x0
		xdma_event_intr3	0x1
		spi0_cs2	0x2
		pr0_pru1_gpo0	0x3
		spi2_d0	0x4
		pr0_pru1_gpi0	0x5
		EMU10	0x6
		gpio4_8	0x7
		uart0_rtsn	0x8
175	Y23	porz	0x0
177	B7	gpmc_ad4	0x0
		mmc1_dat4	0x1
		gpio1_4	0x7
179	AC24	cam1_data9	0x0
		dss_data16	0x2
		pr0_pru0_gpo17	0x3
		spi2_cs3	0x4
		pr0_pru0_gpi17	0x5
		EMU9	0x6
		gpio4_7	0x7
		uart0_ctsn	0x8
181	A7	gpmc_ad5	0x0
		mmc1_dat5	0x1
		gpio1_5	0x7
182	Y22	I2C0_SCL	0x0
		timer7	0x1
		uart2_rtsn	0x2
		eCAP1_in_PWM1_out	0x3
		gpio3_6	0x7
183	C8	gpmc_ad6	0x0
		mmc1_dat6	0x1
		gpio1_6	0x7
184	AB24	I2C0_SDA	0x0
		timer4	0x1
		uart2_ctsn	0x2
		eCAP2_in_PWM2_out	0x3
		gpio3_5	0x7
186	AC18	cam0_field	0x0
		dss_data21	0x2
		cam0_data10	0x3

		spi2_sclk	0x4
		cam1_data10	0x5
		EMU4	0x6
		gpio4_2	0x7
187	AC20	cam0_pclk	0x0
		dss_data19	0x2
		pr0_pru0_gpo14	0x3
		spi2_cs0	0x4
		pr0_pru0_gpi14	0x5
		EMU6	0x6
		gpio4_4	0x7
		I2C2_SDA	0x8
188	AA19	cam0_data9	0x0
		dss_data17	0x2
		pr0_pru0_gpo16	0x3
		spi2_cs3	0x4
		pr0_pru0_gpi16	0x5
		EMU8	0x6
		gpio4_6	0x7
189	A6	gpmc_ad3	0x0
		mmc1_dat3	0x1
		gpio1_3	0x7
190	AE20	cam0_data6	0x0
		mmc1_dat2	0x1
		qspi_d2	0x3
		ehrpwm1A	0x6
		gpio4_28	0x7
191	B6	gpmc_ad2	0x0
		mmc1_dat2	0x1
		gpio1_2	0x7
192	AD20	cam0_data7	0x0
		mmc1_dat3	0x1
		qspi_d3	0x3
		ehrpwm1B	0x6
		gpio4_29	0x7
193	A5	gpmc_ad1	0x0
		mmc1_dat1	0x1
		gpio1_1	0x7
194	AE19	cam0_data4	0x0
		mmc1_dat0	0x1
		cam1_wen	0x2

		qspi_d0	0x3
		ehrpwm3A	0x6
		gpio4_26	0x7
195	B5	gpmc_ad0	0x0
		mmc1_dat0	0x1
		gpio1_0	0x7
196	AD19	cam0_data5	0x0
		mmc1_dat1	0x1
		qspi_d1	0x3
		ehrpwm3B	0x6
		gpio4_27	0x7
197	AD18	cam0_vd	0x0
		dss_data22	0x2
		pr1_edio_outvalid	0x3
		spi2_d1	0x4
		EMU11	0x5
		EMU3	0x6
		gpio4_1	0x7
198	AB19	cam0_data8	0x0
		dss_data18	0x2
		pr0_pru0_gpo15	0x3
		spi2_cs2	0x4
		pr0_pru0_gpi15	0x5
		EMU7	0x6
		gpio4_5	0x7
		I2C2_SCL	0x8
199	AE17	cam0_hd	0x0
		dss_data23	0x2
		pr1_edio_sof	0x3
		spi2_cs1	0x4
		EMU10	0x5
		EMU2	0x6
		gpio4_0	0x7
201	AD17	cam0_wen	0x0
		dss_data20	0x2
		cam0_data11	0x3
		spi2_d0	0x4
		cam1_data11	0x5
		EMU5	0x6
		gpio4_3	0x7

4. Interface Details

4.1. Overview

This chapter describes in detail the VAR-SOM-AM43 interfaces, referring to the default SoM pin names. However, many additional interfaces are available when different pin modes are selected by the user.
PinMux Table 3.2 details the additional possible options for each pin on the VAR-SOM-AM43 connectors.
The following list describes this chapter's column header tables:
Signal:
VAR-SOM-AM43 original pin name
Pin#:
Pin Number on the SO-DIMM204 connector
Type:
Pin Type & Direction:

- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- P – Power Pin

Description:
Short Pin functionality description

4.2. Display Interfaces

The general features of the DSS module include:

- Display Controller
  - Display Modes
- Programmable pixel memory formats (Palletized: 1, 2, 4, 8-bit per pixel; RGB 16, and 24-bit per pixel; and YUV 4:2:2)
- Programmable display size (up to 2048 x 2048)
- 256 x 24-bit entries palette in RGB
- Programmable pixel rate (up to 80 MHz)
  - Display Support
- Four types of displays are supported: Passive and Active colors, Passive and Active monochromes.
- 4-/8-bit Monochrome Passive panel interface support (15 grayscale levels supported using dithering block)
- RGB 8-bit Color Passive panel interface support (3,375 colors supported for color panel using dithering block).
- RGB 12/16/18/24-bit Active panel interface support (replicated or dithered encoded pixel values).
- Remote Frame Buffer (embedded in the LCD panel) support through the RFBI module
- Partial refresh of the remote frame buffer through the RFBI module

- Partial display
- Multiple cycles output format on 8/9/12/16bit interface (TDM)
  - Signal Processing
- Overlay and Windowing support for one Graphics layer (RGB or CLUT) and two Video layers (YUV 4:2:2, RGB16 and RGB24)
- RGB 24-bit support on the display interface, optionally dithered to RGB 18-bit pixel output + 6-Bit Frame rate Control (spatial and temporal)
- Transparency color key (source and destination)
- Synchronized buffer update
- Gamma Curve Support
- Multiple-buffer support
- Cropping Support
- Merge capability of the DMA FIFO for use by a single pipeline in case of DVFS
- Color Phase rotation
  - Interrupt line and DMA line trigger signals
- The LCD DMA is a secure transaction initiator on the L3 interconnect.
- Remote Frame Buffer Interface
  - Access to RFB's "direct MPU interface"
- Sending commands to the RFB panel.
- Sending data to the RFB panel, received from the Display controller or from the MPU (through the L4 OCP slave port)
- Reading data/status from the RFB to the OCP slave port.
  - RFB interface
- 8/9/12/16-bit parallel interface (up to QVGA@30fps at nominal voltage)
- Two programmable configurations for two devices connected to the RFBI module.
- Tearing Effect control logic (Horizontal Synchronization (HSync) and Vertical Synchronization (VSync) embedded in a single signal (TE) or using two signals (HS+VS)).
  - Data formats
- Programmable pixel memory formats (12-, 16-, 18- and 24-bit-per-pixel modes in RGB format)
- Programmable output formats on one/multiple cycles per pixel (data from Display controller and from L4) (TDM)

The VAR-SOM-AM43 provides the logic to display a video frame from the memory frame buffer on a LCD panel using an up to 24-bit parallel RGB bus.

DSI signals:

SIGNAL NAME	Pin#	Description	Type
dss_data0	75	LCD_data B0	O
dss_data1	80	LCD_data B1	O
dss_data2	77	LCD_data B2	O
dss_data3	132	LCD_data B3	O
dss_data4	82	LCD_data B4	O
dss_data5	79	LCD_data B5	O
dss_data6	C20	LCD_data B6	O

dss_data7	128	LCD_data B7	O
dss_data8	126	LCD_data G0	O
dss_data9	81	LCD_data G1	O
dss_data10	123	LCD_data G2	O
dss_data11	129	LCD_data G3	O
dss_data12	142	LCD_data G4	O
dss_data13	133	LCD_data G5	O
dss_data14	146	LCD_data G6	O
dss_data15	144	LCD_data G7	O
dss_data16	179	LCD_data R0	O
dss_data17	188	LCD_data R1	O
dss_data18	198	LCD_data R2	O
dss_data19	187	LCD_data R3	O
dss_data20	201	LCD_data R4	O
dss_data21	186	LCD_data R5	O
dss_data22	197	LCD_data R6	O
dss_data23	199	LCD_data R7	O
dss_pclk	78	LCD pixel clock	O
dss_vsync	74	LCD vertical sync	O
dss_hsync	73	LCD horizontal sync	O
dss_ac_bias_en	76	LCD AC bias enable CS	O
ECAP0_IN_PWM0_OUT	68	Backlight PWM	O

4.3. Ethernet

The AM43 SOM includes two EMAC designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks.

The general features of the ethernet switch subsystem are:
- Two 10/100/1000 Ethernet ports with GMII, RMII and RGMII interfaces
- Wire rate switching (802.1d)
- Non Blocking switch fabric
- Flexible logical FIFO based packet buffer structure
- Four priority level QOS support (802.1p)
- CPPI 3.1 compliant DMA controllers
- Support for IEEE 1588v2 Clock Synchronization (2008 Annex D, E, and F)
    - Timing FIFO and time stamping logic inside the SS
- Device Level Ring (DLR) Support
- Address Lookup Engine
    - 1024 addresses plus VLANs
    - Wire rate lookup
    - VLAN support
    - Host controlled time-based aging
    - Spanning tree support

  - L2 address lock and L2 filtering support
  - MAC authentication (802.1x)
  - Receive or destination based Multicast and Broadcast limits
  - MAC address blocking
  - Source port locking
  - OUI host accept/deny feature

- Flow Control Support (802.3x)
- EtherStats and 802.3Stats RMON statistics gathering (shared)
- Support for external packet dropping engine
- CPGMAC_SL transmit to CPGMAC_SL receive Loopback mode (digital loopback) supported
- CPGMAC_SL receive to CPGMAC_SL transmit Loobback mode (FIFO loopback) supported
- Maximum frame size 2016 bytes (2020 with VLAN)
- 8k (2048 x 32) internal CPPI buffer descriptor memory
- MDIO module for PHY Management
- Programmable interrupt control with selected interrupt pacing
- Emulation Support.
- Programmable transmit Inter-Packet Gap (IPG)
- Reset isolation

4.3.1. On board 1G PHY

The onboard Ethernet PHY AR8033/ADIN1300 exports the differential pairs and led signals to the edge connector.

Gigabit Ethernet Signals:

AM437X SIGNAL NAME	DESCRIPTION	pin
GND	ground signal	29
MDI_A+	Media-dependent interface _A+	31
MDI_A-	Media-dependent interface _A-	33
GND	ground signal	35
MDI_B+	Media-dependent interface _B+	37
MDI_B-	Media-dependent interface _B-	39
GND	ground signal	41
MDI_C+	Media-dependent interface _C+	43
MDI_C-	Media-dependent interface _C-	45
GND	ground signal	47
MDI_D+	Media-dependent interface _D+	49
MDI_D-	Media-dependent interface _D-	51
GND	ground signal	53
LED_ACT	LED output for 10/100/1000 BASE-T activity	55
LED_LINK_10_100	LED output for 10/100 BASE-T link	59
LED_LINK_1000	LED output for 1000 BASE-T link	57

TABLE 1: AR8033 ETHERNET PHY LED BEHAVIOR

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_LINK_10_100	OFF	OFF	ON	ON	OFF	OFF
LED_LINK_1000	OFF	OFF	OFF	OFF	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

TABLE 2: ADIN1300 ETHERNET PHY LED BEHAVIOR

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_LINK_10_100	OFF	OFF	OFF	OFF	OFF	OFF
LED_LINK_1000	ON	ON	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

4.3.2. Optional ROUTE OUT RGMII interface.

In a configuration without a Wi-Fi module RGMII2 Interface will be routed out.

Optional additional Gigabit Ethernet signals:

AM437X SIGNAL NAME	BALL #	DESCRIPTION	PIN#
RGMII2_RCLK	F6	RGMII2_RCLK	12
RGMII2_RCTL	C5	RGMII2_RCTL	14
RGMII2_RD0	D8	RGMII2_RD0	16
RGMII2_RD1	G8	RGMII2_RD1	18
RGMII2_RD2	B4	RGMII2_RD2	20
RGMII2_RD3	F7	RGMII2_RD3	22
RGMII2_TCLK	E8	RGMII2_TCLK	9
RGMII2_TCTL	C3	RGMII2_TCTL	11
RGMII2_TD0	E7	RGMII2_TD0	1
RGMII2_TD1	D7	RGMII2_TD1	3
RGMII2_TD2	A4	RGMII2_TD2	5
RGMII2_TD3	C6	RGMII2_TD3	7
ETH_MDIO_DATA	A17	ETH_MDIO_DATA	42
ETH_MDIO_CLK	B17	ETH_MDIO_CLK	40

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs		
		1	2	3
MDIO_DATA	MDIO Data	B12	A17	D24
MDIO_MDCLK	MDIO Clock	A12	B17	C24

4.4. USB 2.0

The SOM provides with 2 USB I/F, USB0 is used as OTG, and USB1 is used as host interface.

4.4.1. USB 2.0 HOST

USB HOST1 signals:

AM437X PINS	DESCRIPTION	PIN #
USB1_DM	USB1 Data minus	89
USB1_DP	USB1 Data plus	87
USB1_DRVVBUS	USB1 Active high VBUS control output	65
USB1_VBUS	USB1 VBUS	91

4.4.2. USB 2.0 On-the-Go

USB0 OTG signals:

AM437X SIGNAL NAME	DESCRIPTION	PIN #
USB0_DM	USB0 Data minus	97
USB0_DP	USB0 Data plus	95
USB0_DRVVBUS	USB0 Active high VBUS control output	98
USB0_ID	USB0 OTG ID (Micro-A or Micro-B Plug)	88
USB0_VBUS	USB0 VBUS	99
AM437X_USB0_VBUS_DET	GPIO5_9, USB0_VBUS_DET	63

4.5. MMC/SD/SDIO

The general features of the MMCSD host controller IP are:
• Built-in 1024-byte buffer for read or write
• Two DMA channels, one interrupt line
• Clock support
  - 96-MHz functional clock source input
  - up to 384Mbit/sec (48MByte/sec) in MMC mode 8-bit data transfer
  - up to 192Mbit/sec (24MByte/sec) in High-Speed SD mode 4-bit data transfer
  - up to 24Mbit/sec (3MByte/sec) in Default SD mode 1-bit data transfer
• Support for SDA 3.0 Part A2 programming model
• Serial link supports full compliance with:
  - MMC command/response sets as defined in the MMC standard specification v4.3.
  - SD command/response sets as defined in the SD Physical Layer specification v2.00
  - SDIO command/response sets and interrupt/read-wait suspend-resume operations as defined in the SD part E1 specification v 2.00
  - SD Host Controller Standard Specification sets as defined in the SD card specification Part A2
  - v2.00

4.5.1. MMC0 Signals

SDMMC0 Interface signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs					
MMC0_CLK	SD Card Clock	141	141	141	141	141	141
MMC0_CMD	SD Card Command	145	145	145	145	145	145
MMC0_DAT0	SD Card Data Bus	147	147	147	147	147	147
MMC0_DAT1	SD Card Data Bus	139	139	139	139	139	139
MMC0_DAT2	SD Card Data Bus	140	140	140	140	140	140
MMC0_DAT3	SD Card Data Bus	143	143	143	143	143	143
MMC0_SDCD	SD Card Detect	42	42	42	54	54	54
MMC0_SDWP	SD Card Write Protect	40	40	40	40	40	40
MMC0_POW	SD Card Power Switch Control	52	117	68	52	117	68

4.5.2. MMC1 Signals

SDMMC1 Interface signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs	
MMC1_CLK	MMC/SD/SDIO Clock	48	48
MMC1_CMD	MMC/SD/SDIO Command	50	50
MMC1_DAT0	MMC/SD/SDIO Data Bus	194	194
MMC1_DAT1	MMC/SD/SDIO Data Bus	196	196
MMC1_DAT2	MMC/SD/SDIO Data Bus	190	190

MMC1_DAT3	MMC/SD/SDIO Data Bus	192	192
MMC1_SDCD	SD Card Detect	131	92
MMC1_SDWP	SD Write Protect	69	111

4.5.3. MMC2 Signals

SDMMC2 Interface signals:

AM437X SIGNAL NAME	DESCRIPTION	PINs
MMC2_CLK	MMC/SD/SDIO Clock	34
MMC2_CMD	MMC/SD/SDIO Command	30
MMC2_DAT0	MMC/SD/SDIO Data Bus	28
MMC2_DAT1	MMC/SD/SDIO Data Bus	23
MMC2_DAT2	MMC/SD/SDIO Data Bus	21
MMC2_DAT3	MMC/SD/SDIO Data Bus	15
MMC2_SDCD	SD Card Detect	151/125
MMC2_SDWP	SD Write Protect	119/70

4.6. Audio

4.6.1. TLV320AIC3106 Audio codec

Audio interfaces are featured by an on-board Texas Instrument's feature-rich TLV320AIC3106 audio codec device. Please refer to the TLV320AIC3106 data sheet for Detailed electrical characteristics of relevant interfaces.
Main supported features are:

- Stereo line in
- Stereo line out
- Stereo headphones driver
- Digital microphone
- Analog microphone

Audio interface Signals:

SIGNAL NAME	CODEC PIN#	DESCRIPTION	PIN#
LINEOUT_RP	31	RIGHT LINE OUTPUT (+)	174
LINEOUT_LP	29	LEFT LINE OUTPUT (+)	176
MIC_IN_R	14	MIC3 INPUT RIGHT	161
MIC_IN_L	11	MIC3 INPUT LEFT	153
MICBIAS	13	MICROPHONE BIAS VOLTAGE OUTPUT	159
MICDET	12	MICROPHONE DETECT	157
LINEIN1_LP	3	LINE1 ANALOG LEFT INPUT (+)	172
LINEIN1_RP	5	LINE1 ANALOG RIGHT INPUT (+)	168
DMIC_CLK	35	DIGITAL MICROPHONE CLOCK	178
DMIC_DATA	34	DIGITAL MICROPHONE DATA	180

4.6.2. MCASP0 (Multichannel Audio Serial Port)

The interface is shared with the on board Wi-Fi module.

McASP0 Signals:

AM437X SIGNAL NAME	ZDN BALL #	DESCRIPTION	PIN#
MCASP0_ACLKX	N24	McASP0 Transmit Bit Clock	54
MCASP0_FSX	N22	McASP0 Transmit Frame Sync	92
MCASP0_AXR0	H23	McASP0 Serial Data (IN/OUT)	125
MCASP0_AXR1	M25	McASP0 Serial Data (IN/OUT) _RD0	62
MCASP0_AHCLKR	M24	McASP0 Receive Master Clock	58
MCASP0_AHCLKX	L24	McASP0 Transmit Master Clock	60
MCASP0_ACLKR	L23	McASP0 Receive Bit Clock	117
MCASP0_FSR	K23	McASP0 Receive Frame Sync	122

4.7. Camera

4.7.1. CPI Camera interface #0.

The general features of the VPFE module include:

- A buffer memory for interfacing to the DMA at the chip level and preventing the CCDC module from overflowing.
- Support for conventional Bayer pattern and Foveon sensor formats
- Generates HD/VD timing signals and field ID to an external timing generator or can synchronize to the external timing generator
- Support for progressive and interlaced sensors (hardware support for up to 2 fields and firmware support for higher number of fields, typically 3-, 4-, and 5-field sensors)
- Support for up to the lesser of 75 MHz or 1/2 dma_ocp_clk sensor clock in the normal mode
- Support for REC656/CCIR-656 standard (YCbCr 422 format, either 8- or 16-bit)
- Support for YCbCr 422 format, either 8- or 16-bit with discrete H and VSYNC signals.
- Support for up to 16-bit input
- Generates optical black clamping signals
- Support for digital clamping and black level compensation
- Support for 10-bit to 8-bit A-law compression
- Support for a low-pass filter prior to writing to SDRAM. If this filter is enabled, 2 pixels each in the left and right edges of each line are cropped from the output.
- Support for generating output to range from 16-bits to 8-bits wide
- Support for downsampling via programmable culling patterns
- Ability to control output to the SDRAM via an external write enable signal
- Support for up to 16K pixels (image size) in both the horizontal and vertical direction

Parallel Camera Interface #0 signals:

AM437X SIGNAL NAME	DESCRIPTION	PINs
Cam0_data0	Camera data	32
Cam0_data1	Camera data	46
Cam0_data2	Camera data	48
Cam0_data3	Camera data	50
Cam0_data4	Camera data	194
Cam0_data5	Camera data	196
Cam0_data6	Camera data	190
Cam0_data7	Camera data	192
Cam0_data8	Camera data	198
Cam0_data9	Camera data	188
Cam0_data10	Camera data	27
Cam0_data11	Camera data	25
Cam0_hd	CCD Data Horizontal Detect	199
Cam0_pclk	CCD Data Pixel Clock	187
Cam0_vd	CCD Data Vertical Detect	197
Cam0_wen	CCD Data Write Enable	201
Cam0_field	CCD Data Field Indicator	186

4.7.2. CPI Camera interface #1.

Parallel Camera Interface #1 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs					
cam1_data0	Camera data	38	38	38	38	38	38
cam1_data1	Camera data	36	36	36	36	36	36
cam1_data2	Camera data	34	34	34	34	34	34
cam1_data3	Camera data	30	30	30	30	30	30
cam1_data4	Camera data	28	28	28	28	28	28
cam1_data5	Camera data	23	23	23	23	23	23
cam1_data6	Camera data	21	21	21	21	21	21
cam1_data7	Camera data	15	15	15	15	15	15
cam1_data8	Camera data	173	173	46	173	173	46
cam1_data9	Camera data	179	179	32	179	179	32
cam1_data10	Camera data	186	48	48	186	48	48
cam1_data11	Camera data	201	50	50	201	50	50
cam1_hd	CCD Data Horizontal Detect	17	17	17	17	17	17
cam1_pclk	CCD Data Pixel Clock	13	13	13	13	13	13
cam1_vd	CCD Data Vertical Detect	26	26	26	26	26	26
cam1_wen	CCD Data Write Enable	25	25	25	194	194	194
cam1_field	CCD Data Field Indicator	27	27	27	27	27	27

4.8. UART Interfaces

The general features of the UART/IrDA module when operating in UART mode are:

- 16C750 compatibility
- Baud rate from 300 bps up to 3.6864 Mbps
- Auto-baud between 1200 bps and 115.2 Kbps
- Software/Hardware flow control
  - Programmable Xon/Xoff characters
  - Programmable Auto-RTS and Auto CTS
- Programmable serial interface characteristics
  - 5, 6, 7, or 8-bit characters
  - Even, odd, mark (always 1), space (always 0), or no parity (non-parity bit frame) bit generation and detection
  - 1, 1.5, or 2 stop bit generation
- False start bit detection
- Line break generation and detection
- Modem control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully prioritized interrupt system controls
- Internal test and loopback capabilities

The SOM includes five UART I/F routed out.

4.8.1. UART0 Interface

UART0 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs	
UART0_ CTSn[2]	UART Clear to Send	61	179
UART 0_ RTSn[2]	UART Request to Send	64	173
UART 0_ RXD	UART Receive Data	66	66
UART 0_ TXD	UART Transmit Data	67	67
UART 0_DCDn	UART Data Carrier Detect	28	28

4.8.2. UART1 Interface

UART1 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs	
		1	2
UART 1_ CTSn[2]	UART Clear to Send	34	124
UART 1_ RTSn[2]	UART Request to Send	30	120
UART 1_RXD[2]	UART Receive Data	38	111
UART 1_TXD[2]	UART Transmit Data	36	119

UART1 full modem Interface signals:

AM437X SIGNAL NAME	DESCRIPTION	PINs
UART 1_ CTSn[2]	UART Clear to Send	34
UART 1_ RTSn[2]	UART Request to Send	30
UART 1_RXD[2]	UART Receive Data	38
UART 1_TXD[2]	UART Transmit Data	36
UART 1_DTRn[2]	UART Data Terminal Ready	15
UART1_DSRn[2]	UART Data Set Ready	23
UART 1_DCDn[2]	UART Data Carrier Detect	21
UART1_RIn[2]	UART Ring Indicator	28

4.8.3. UART2 Interface

UART2 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs			
		1	2	3	4
UART 2_ CTSn[2]	UART Clear to Send	184	126	184	126
UART 2_ RTSn[2]	UART Request to Send	182	81	182	81

UART 2_RXD[2]	UART Receive Data	86	86	141	141
UART 2_TXD[2]	UART Transmit Data	71	71	145	145

4.8.4. UART3 Interface

UART3 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs						
		1	2	3	4	5	6	7
UART 3_ CTSn[2]	UART Clear to Send	123	42	141	141	123	42	8
UART 3_ RTSn[2]	UART Request to Send	129	40	145	145	129	40	6
UART 3_RXD[2]	UART Receive Data	52	52	52	139	139	139	4
UART 3_TXD[2]	UART Transmit Data	68	68	68	147	147	147	2

4.8.5. UART5 Interface

UART5 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs					
		1	2	3	4	5	6
UART 5_ CTSn[2]	UART Clear to Send	139	146	B14	139	146	B14
UART 5_ RTSn[2]	UART Request to Send	147	144	B13	147	144	B13
UART 5_RXD[2]	UART Receive Data	81	81	81	42	42	42
UART 5_TXD[2]	UART Transmit Data	126	126	126	40	40	40

Notes:

1. UART0 Signals are used by default as a low level debug port
2. Refer to PinMux Table 3.2 for RTS/CTS Options
3. UART3 is used by on SOM Bluetooth. Interface can be exported from pins 2,4,6,8 on SOM without WiFi/BT module mounted. Interface can be exported from other pins only if Bluetooth is disabled.

4.9. SPI

The general features of the SPI controller are:
• Buffered receive/transmit data register per channel (1 word deep)
• Multiple SPI word access with one channel using a FIFO
• Two DMA requests per channel, one interrupt line
• Single interrupt line, for multiple interrupt source events
• Serial link interface supports:
  - Full duplex / Half duplex
  - Multi-channel master or single channel slave operations
  - Programmable 1-32 bit transmit/receive shift operations.
  - Wide selection of SPI word lengths continuous from 4 to 32 bits
• Up to four SPI channels
• SPI word Transmit / Receive slot assignment based on round robin arbitration
• SPI configuration per channel (clock definition, enable polarity and word width)
• Clock generation supports:
  - Programmable master clock generation (operating from fixed 48-MHz functional clock input)
  - Selectable clock phase and clock polarity per chip select.

The SOM includes four SPI I/F routed out.

SPI0 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs			
		1	2	3	
SPI0_SCLK	SPI Clock	86	86	86	
SPI0_D0	SPI Data	71	71	71	
SPI0_D1	SPI Data	69	69	69	
SPI0_CS0	SPI Chip Select	70	70	70	
SPI0_CS1	SPI Chip Select	52	52	52	
SPI0_CS2	SPI Chip Select		173	138	
SPI0_CS3	SPI Chip Select	54	17	154	

SPI1 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs			
		1	2	3	4
SPI1_SCLK	SPI Clock	68	68	54	54
SPI1_D0	SPI Data	61	61	92	92
SPI1_D1	SPI Data	64	64	125	125
SPI1_CS0	SPI Chip Select	124	66	66	
SPI1_CS1	SPI Chip Select	120	67	67	68
SPI1_CS2	SPI Chip Select	167	26	26	
SPI1_CS3	SPI Chip Select	109	13		

SPI2 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs			
		1	2	3	4
SPI2_SCLK	SPI Clock	186	13	94	94
SPI2_D0	SPI Data	201	173	84	84
SPI2_D1	SPI Data	197	25	90	90
SPI2_CS0	SPI Chip Select	187	187	187	83
SPI2_CS1	SPI Chip Select				
SPI2_CS2	SPI Chip Select	198	198	198	
SPI2_CS3	SPI Chip Select	188	188	188	

SPI3 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs			
		1	2	3	4
SPI3_SCLK	SPI Clock			142	142
SPI3_D0	SPI Data			133	133
SPI3_D1	SPI Data			146	146
SPI3_CS0	SPI Chip Select				
SPI3_CS1	SPI Chip Select	109	137	137	109
SPI3_CS2	SPI Chip Select	No	No	No	No
SPI3_CS3	SPI Chip Select	No	No	No	No

4.10. QSPI

The main features of the QSPI include:

- Programmable divider for serial data clock generation
- Six pin interface (DCLK, CS_N, DOUT, DIN, QDIN1, QDIN2)
- Programmable data length (No. of bits from 1-32)
- 4 external chip select signals
- Support for 3-, 4- or 6-pin SPI interface
    - 3-pin mode uses spi_dout as inout/spi_din not used
    - 4-pin mode for dual read uses spi_dout as in/spi_din as in
    - 6-pin mode uses spi_dout as in/spi_din as in/spi_qdin0 as in/spi_qdin1 as in
- Programmable transfer or frame size (No. of words from 1 to 4096)
- Optional interrupt generation on word or frame completion
- Programmable CS_N to DOUT delay from 0 to 3 DCLKs
- Programmable signal polarities
- Programmable active clock edge
- Software controllable interface allowing for any type of SPI transfer
- Control through OCP configuration port access

QSPI signals:

AM437X SIGNAL NAME	DESCRIPTION	PINs
QSPI3_CLK	SPI Clock	48
QSPI_CSN	SPI Chip Select	50
QSPI_D0	SPI Data	194
QSPI_D1	SPI Data	196
QSPI_D2	SPI Data	190
QSPI_D3	SPI Data	192

4.11. I2C

The general features of the I2C controller are:
• Compliant with Philips I2C specification version 2.1
• Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s).
• Multimaster transmitter/slave receiver mode
• Multimaster receiver/slave transmitter mode
• Combined master transmit/receive and receive/transmit modes
• 7-bit and 10-bit device addressing modes
• Built-in 32-byte FIFO for buffered read or writes in each module
• Programmable clock generation
• Two DMA channels, one interrupt line

The SOM includes three I2C I/F:
The I2C0 is used for on SOM devices and also routed to the external connector.

I2C0 signals:

SIGNAL NAME	DESCRIPTION	PIN	PERIPHERAL	ADDRESS
I2C0_SCL	I2C Clock	182	PMIC	0X00100100
I2C0_SDA	I2C Data	184	EEPROM	0X1010000
			CODEC	0X0011011

I2C1 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs				
		1	2	3	4	5
I2C1_SCL	I2C Clock	70	64	119	46	94
I2C1_SDA	I2C Data	69	61	111	32	83

I2C2 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs				
		1	2	3	4	5
I2C2_SCL	I2C Clock	T22	J24	L22	AC21	AB19
I2C2_SDA	I2C Data	P23	K25	K22	AB20	AC20

4.12. CAN

The general features of the DCAN controller are:
• Supports CAN protocol version 2.0 part A, B (ISO 11898-1)
• Bit rates up to 1 MBit/s
• Dual clock source
• 16, 32, 64 or 128 message objects (instantiated as 64 on this device)
• Individual identifier mask for each message object
• Programmable FIFO mode for message objects
• Programmable loop-back modes for self-test operation
• Suspend mode for debug support
• Software module reset
• Automatic bus on after Bus-Off state by a programmable 32-bit timer
• Message RAM parity check mechanism
• Direct access to Message RAM during test mode
• CAN Rx / Tx pins configurable as general purpose IO pins
• Two interrupt lines (plus additional parity-error interrupt line)
• RAM initialization
• DMA suppor

The SOM includes two CAN I/F.4 signals are routed to the edge connector.

CAN0 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs		
		1	2	3
DCAN0_TX	DCAN Receive Data	66	124	
DCAN0_RX	DCAN Transmit Data	67	120	

CAN1 signals:

AM437X SIGNAL NAME	DESCRIPTION	Valid configuration PINs		
		1	2	3
DCAN1_TX	DCAN Receive Data	141	61	111
DCAN1_RX	DCAN Transmit Data	145	64	119

4.13. Analog to Digital Convertor (ADC0)

The touchscreen controller and analog-to-digital converter subsystem (TSC_ADC_SS or ADC0) contains a single-channel ADC connected to an 8-to-1 analog multiplexer which operates as a general-purpose analog-to-digital converter (ADC) with optional support for interleaving touchscreen (TS) conversions for a 4-wire, 5-wire, or 8-wire resistive panel. The TSC_ADC_SS can be configured for use in one of the following applications:

- 8 general-purpose ADC channels
- 4-wire TSC with 4 general-purpose ADC channels
- 5-wire TSC with 3 general-purpose ADC channels
- 8-wire TSC

The SOM routes all 8bit of ADC0 to the edge connector.

ADC0 signals:

SIGNAL NAME	Pin#	Description	Type
ADC0_AIN0	160	Analog Input	A
ADC0_AIN1	155	Analog Input	A
ADC0_AIN2	152	Analog Input	A
ADC0_AIN3	158	Analog Input	A
ADC0_AIN4	162	Analog Input	A
ADC0_AIN5	136	Analog Input	A
ADC0_AIN6	156	Analog Input	A
ADC0_AIN7	163	Analog Input	A
AGND	166	Analog Negative Reference Input	AP

ADC0 positive /negative reference inputs, ADC0_VREFP, ADC0_VREFN should be supplied either from VDDA_ADC, GNDA_ADC Respectively or from an external source.

ADC0_VREFP, ADC0_VREFN signals:

SIGNAL NAME	Pin#	Min	Nom	Max
ADC0_VREFP	164	1.15V		1.8
ADC0_VREFN	166	0		0.65
ADC0_VREFP+ ADC0_VREFN			1.8	

4.13.1. Touch Screen

4-wire Touch Screen signals:

ADC0 Controller	Pin#	Touch Panel
ADC0_AIN0	160	XPUL
ADC0_AIN1	155	XNUR
ADC0_AIN2	152	YPLL
ADC0_AIN3	158	YNLR

- Touchscreen Resistance: 6 kOHm max.
- Drive Current: 25 mA max.
- Pen Touch Detect: 2 kOHm max.

4.13.2. Analog Inputs

- Full-scale Input Range: 1.8V
- Differential Non-Linearity (DNL): ±1LSB
- Integral Non-Linearity (INL): ±2LSB
- Gain Error: ±2LSB
- Offset Error: ±2LSB
- Sampling Rate: 800KSPS
- Conversion Time: 15 Clock Cycles

Analog to Digital Convertor inputs signals:

SIGNAL NAME	Pin#	Description	Type
ADC0_AIN4	162	Analog Input	A
ADC0_AIN5	136	Analog Input	A
ADC0_AIN6	156	Analog Input	A
ADC0_AIN7	163	Analog Input	A
AGND	166	Analog Negative Reference Input	AP

4.14. General Purpose I/O

The SOM provides IO pins which can be used as GPIOs.

GPIO signals:

SIGNAL NAME	PIN#	BALL#	SIGNAL NAME	PIN#	BALL#	SIGNAL NAME	PIN#	BALL#
GPIO0_2	62	M25	GPIO1_22	9	E8	GPIO4_1	197	AD18
GPIO0_2	86	P23	GPIO1_23	12	F6	GPIO4_2	186	AC18
GPIO0_3	71	T22	GPIO1_24	22	F7	GPIO4_3	201	AD17
GPIO0_3	60	L24	GPIO1_25	20	B4	GPIO4_4	187	AC20
GPIO0_4	69	T21	GPIO1_26	18	G8	GPIO4_5	198	AB19
GPIO0_5	70	T20	GPIO1_27	16	D8	GPIO4_6	188	AA19
GPIO0_6	52	R25	GPIO2_2[1]	154	A9	GPIO4_7	179	AC24
GPIO0_7	68	G24	GPIO2_3[1]	138	E10	GPIO4_8	173	AD24
GPIO0_8	142	C19	GPIO2_4[1]	167	D10	GPIO4_9	17	AD25
GPIO0_9	133	D19	GPIO2_5[1]	109	C10	GPIO4_10	26	AC23
GPIO0_10	146	C17	GPIO2_6	75	B22	GPIO4_11	13	AE21
GPIO0_11	144	D17	GPIO2_7	80	A21	GPIO4_12	27	AC25
GPIO0_12	124	K22	GPIO2_8	77	B21	GPIO4_13	25	AB25
GPIO0_13	120	L22	GPIO2_9	132	C21	GPIO4_14	38	AB20
GPIO0_14	111	K21	GPIO2_10	82	A20	GPIO4_15	36	AC21
GPIO0_15	119	L21	GPIO2_11	79	B20	GPIO4_16	34	AD21
GPIO0_18	98	G21	GPIO2_12	127	C20	GPIO4_17	30	AE22
GPIO0_18	117	L23	GPIO2_13	128	E19	GPIO4_18	28	AD22
GPIO0_19	122	K23	GPIO2_14	126	A19	GPIO4_19	23	AE23
GPIO0_20	84	P22	GPIO2_15	81	B19	GPIO4_20	21	AD23
GPIO0_21	90	P20	GPIO2_16	123	A18	GPIO4_21	15	AE24
GPIO0_22	94	N20	GPIO2_17	129	B18	GPIO4_24	48	Y18
GPIO0_23	83	T23	GPIO2_22	74	B23	GPIO4_25	50	AA18
GPIO0_25	65	F25	GPIO2_23	73	A23	GPIO4_26	194	AE19
GPIO0_30[1]	131	A2	GPIO2_24	78	A22	GPIO4_27	196	AD19
GPIO0_31[1]	151	B3	GPIO2_25	76	A24	GPIO4_28	190	AE20
GPIO1_0[1]	195	B5	GPIO2_26	143	B1	GPIO4_29	192	AD20
GPIO1_1[1]	193	A5	GPIO2_27	140	B2	GPIO5_0	8	H22
GPIO1_2[1]	191	B6	GPIO2_28	139	C2	GPIO5_1	6	K24
GPIO1_3[1]	189	A6	GPIO2_29	147	C1	GPIO5_2	4	H25
GPIO1_4[1]	177	B7	GPIO2_30	141	D1	GPIO5_3	2	H24
GPIO1_5[1]	181	A7	GPIO2_31	145	D2	GPIO5_4	56	P25
GPIO1_6[1]	183	C8	GPIO3_5	184	AB24	GPIO5_5	148	R24
GPIO1_7[1]	169	B8	GPIO3_6	182	Y22	GPIO5_6	149	P24
GPIO1_8	61	L25	GPIO3_13	65	F25	GPIO5_8	114	D25
GPIO1_9	64	J25	GPIO3_14	54	N24	GPIO5_9	63	F24
GPIO1_10	66	K25	GPIO3_15	92	N22	GPIO5_13	115	E24
GPIO1_11	67	J24	GPIO3_16	125	H23	GPIO5_19	32	AE18
GPIO1_12	116	E11	GPIO3_17	58	M24	GPIO5_20	46	AB18

GPIO1_13	150	C11	GPIO3_18	117	L23	GPIO5_23	149	D11
GPIO1_14	135	B11	GPIO3_19	122	K23	GPIO5_24	148	F11
GPIO1_15	137	A11	GPIO3_20	62	M25	GPIO5_27	98	G21
GPIO1_16	11	C3	GPIO3_21	60	L24	GPIO5_30[1]	131	A2
GPIO1_17	14	C5	GPIO3_22	84	P22	GPIO5_31	151	B3
GPIO1_18	7	C6	GPIO3_23	90	P20			
GPIO1_19	5	A4	GPIO3_24	94	N20			
GPIO1_20	3	D7	GPIO3_25	83	T23			
GPIO1_21	1	E7	GPIO4_0	199	AE17			

Note:
[1] The following pins are GPMC Bus signal internally used and routed to the external connector. They can be configured and used as GPIOs only when NAND is not mounted.

4.15. PWM0

The SOM uses PWM0 output for control the LCD backlight.

PWM0 signals:

AM437X SIGNAL NAME	ZDN BALL #	DESCRIPTION	PIN#
AM437X_LCD_BACKLIGHT	G24	Auxiliary PWM0 output	68

4.16. General System Control

4.16.1. Boot Options

Boot Mode is selected via Boot.
Configuration Pins Latched on the Rising Edge of the PWRONRSTn Reset Input Pin:
- DSS_DATA[15:0] terminals are respectively SYSBOOT[15:0] inputs.
- DSS_VSYNC terminal is SYSBOOT[16] input.
- DSS_HSYNC terminal is SYSBOOT[17] input.
- DSS_AC_BIAS_EN is SYSBOOT[18] input.

All the pins routed out for SYSTEM BOOT configuration on the rising edge of PWRONRSTn.

Boot Sequence configuration signals:

Configuration PINS	Value	Description
SYSBOOT [4:0]	00000b	BOOT_SEQUENCE: NAND,USB1,MMC0,USB0
	00001b	BOOT_SEQUENCE: MMC0,MMC1,USB1,USB0
	00100B	BOOT_SEQUENCE: MMC1,MMC0,USB1,USB0
SYSBOOT [5]	1b	0b-MII, 1b-RMII
SYSBOOT [6]	0b	0b-ECC DONE BY ROM, 1b-ECC DONE BY NAND
SYSBOOT [7]	0b	DON'T CARE
SYSBOOT [8]	0b	FOR NAND – WAIT MUX OPTION 0
SYSBOOT [9]	0b	DON'T CARE
SYSBOOT [10]	0b	
SYSBOOT [11]	0b	1B – MUXED DEVICE
SYSBOOT [13:12]	00b	00b- SET FOR NORMAL OPERATION
SYSBOOT [15:14]	01b	24MHZ CLOCK
SYSBOOT [16]	00b	USB_MS & USB_CL: DP/DM not swapped
SYSBOOT [17]	1b	1b- CLKOUT1 ENABLE (TO CODEC 12MHZ)
SYSBOOT [18]	0b	CLKOUT2 output frequency

4.16.2. System Control

The signal AM437X_PORZn reset input of the SOM. The signal SYS_RESETn produce reset to all internal SOM and external devices in case program reset or manual reset from AM437X_PORZn

Power Control signals:

SIGNAL NAME	TPS65218 and AM437x pins	DESCRIPTION	EDGE CONNECTOR
AM437X_PORZN	Y23, 8	Power on Reset. Output of PMIC and Input of SOM from External Reset.	175
LOWPWR_RSTN	PORZ & GPIO0_24	System RESET from POWER RESET and SOFTWARE sources.	171

4.17. PRU-ICSS

4.17.1. PRU-ICSS0 Interface

PRU-ICSS0-PRU0/General Purpose Inputs Signals:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR0_PRU0_GPI0	PRU-ICSS0 PRU0 DATA IN	I	N24	54
PR0_PRU0_GPI1	PRU-ICSS0 PRU0 DATA IN	I	N22	92
PR0_PRU0_GPI10	PRU-ICSS0 PRU0 DATA IN	I	C2	139
PR0_PRU0_GPI11	PRU-ICSS0 PRU0 DATA IN	I	C1	147
PR0_PRU0_GPI12	PRU-ICSS0 PRU0 DATA IN	I	D1	141
PR0_PRU0_GPI13	PRU-ICSS0 PRU0 DATA IN	I	D2	145
PR0_PRU0_GPI14	PRU-ICSS0 PRU0 DATA IN	I	AC20	187
PR0_PRU0_GPI15	PRU-ICSS0 PRU0 DATA IN	I	AB19	198
PR0_PRU0_GPI16	PRU-ICSS0 PRU0 DATA IN	I	AA19	188
PR0_PRU0_GPI17	PRU-ICSS0 PRU0 DATA IN	I	AC24	179
PR0_PRU0_GPI18	PRU-ICSS0 PRU0 DATA IN	I	H25	4
PR0_PRU0_GPI19	PRU-ICSS0 PRU0 DATA IN	I	H24	2
PR0_PRU0_GPI2	PRU-ICSS0 PRU0 DATA IN	I	H23	125
PR0_PRU0_GPI3	PRU-ICSS0 PRU0 DATA IN	I	M24	58
PR0_PRU0_GPI4	PRU-ICSS0 PRU0 DATA IN	I	L23	117
PR0_PRU0_GPI5	PRU-ICSS0 PRU0 DATA IN	I	K23	122
PR0_PRU0_GPI6	PRU-ICSS0 PRU0 DATA IN	I	M25	62
PR0_PRU0_GPI7	PRU-ICSS0 PRU0 DATA IN	I	L24	60
PR0_PRU0_GPI8	PRU-ICSS0 PRU0 DATA IN	I	B1	143
PR0_PRU0_GPI9	PRU-ICSS0 PRU0 DATA IN	I	B2	140

PRU-ICSS0-PRU0/General Purpose Outputs Signals:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR0_PRU0_GPO0	PRU-ICSS0 PRU0 DATA OUT	O	N24	54
PR0_PRU0_GPO1	PRU-ICSS0 PRU0 DATA OUT	O	N22	92
PR0_PRU0_GPO10	PRU-ICSS0 PRU0 DATA OUT	O	C2	139
PR0_PRU0_GPO11	PRU-ICSS0 PRU0 DATA OUT	O	C1	147
PR0_PRU0_GPO12	PRU-ICSS0 PRU0 DATA OUT	O	D1	141
PR0_PRU0_GPO13	PRU-ICSS0 PRU0 DATA OUT	O	D2	145
PR0_PRU0_GPO14	PRU-ICSS0 PRU0 DATA OUT	O	AC20	187
PR0_PRU0_GPO15	PRU-ICSS0 PRU0 DATA OUT	O	AB19	198
PR0_PRU0_GPO16	PRU-ICSS0 PRU0 DATA OUT	O	AA19	188
PR0_PRU0_GPO17	PRU-ICSS0 PRU0 DATA OUT	O	AC24	179
PR0_PRU0_GPO18	PRU-ICSS0 PRU0 DATA OUT	O	H25	187

PR0_PRU0_GPO19	PRU-ICSS0 PRU0 DATA OUT	O	H24	2
PR0_PRU0_GPO2	PRU-ICSS0 PRU0 DATA OUT	O	H23	125
PR0_PRU0_GPO3	PRU-ICSS0 PRU0 DATA OUT	O	M24	58
PR0_PRU0_GPO4	PRU-ICSS0 PRU0 DATA OUT	O	L23	117
PR0_PRU0_GPO5	PRU-ICSS0 PRU0 DATA OUT	O	K23	122
PR0_PRU0_GPO6	PRU-ICSS0 PRU0 DATA OUT	O	M25	62
PR0_PRU0_GPO7	PRU-ICSS0 PRU0 DATA OUT	O	L24	60
PR0_PRU0_GPO8	PRU-ICSS0 PRU0 DATA OUT	O	B1	143
PR0_PRU0_GPO9	PRU-ICSS0 PRU0 DATA OUT	O	B2	140

PRU-ICSS0-PRU1/General Purpose Inputs Signals:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR0_PRU1_GPI0	PRU-ICSS0 PRU1 DATA IN	I	AD24	173
PR0_PRU1_GPI1	PRU-ICSS0 PRU1 DATA IN	I	AD25	17
PR0_PRU1_GPI10	PRU-ICSS0 PRU1 DATA IN	I	AD21	34
PR0_PRU1_GPI11	PRU-ICSS0 PRU1 DATA IN	I	AE22	30
PR0_PRU1_GPI12	PRU-ICSS0 PRU1 DATA IN	I	AD22	28
PR0_PRU1_GPI13	PRU-ICSS0 PRU1 DATA IN	I	AE23	23
PR0_PRU1_GPI14	PRU-ICSS0 PRU1 DATA IN	I	AD23	21
PR0_PRU1_GPI15	PRU-ICSS0 PRU1 DATA IN	I	AE24	15
PR0_PRU1_GPI16	PRU-ICSS0 PRU1 DATA IN	I	AE18	32
PR0_PRU1_GPI17	PRU-ICSS0 PRU1 DATA IN	I	AB18	46
PR0_PRU1_GPI18	PRU-ICSS0 PRU1 DATA IN	I	H22	8
PR0_PRU1_GPI19	PRU-ICSS0 PRU1 DATA IN	I	K24	6
PR0_PRU1_GPI2	PRU-ICSS0 PRU1 DATA IN	I	AC23	26
PR0_PRU1_GPI3	PRU-ICSS0 PRU1 DATA IN	I	AE21	13
PR0_PRU1_GPI4	PRU-ICSS0 PRU1 DATA IN	I	K25	66
PR0_PRU1_GPI5	PRU-ICSS0 PRU1 DATA IN	I	J24	67
PR0_PRU1_GPI6	PRU-ICSS0 PRU1 DATA IN	I	B23	74
PR0_PRU1_GPI7	PRU-ICSS0 PRU1 DATA IN	I	A23	73
PR0_PRU1_GPI8	PRU-ICSS0 PRU1 DATA IN	I	A22	78
PR0_PRU1_GPI9	PRU-ICSS0 PRU1 DATA IN	I	A24	76

PRU-ICSS0-PRU1/General Purpose Outputs Signals:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR0_PRU1_GPO0	PRU-ICSS0 PRU1 DATA OUT	O	AD24	173
PR0_PRU1_GPO1	PRU-ICSS0 PRU1 DATA OUT	O	AD25	17
PR0_PRU1_GPO10	PRU-ICSS0 PRU1 DATA OUT	O	AD21	34

PR0_PRU1_GPO11	PRU-ICSS0 PRU1 DATA OUT	O	AE22	30
PR0_PRU1_GPO12	PRU-ICSS0 PRU1 DATA OUT	O	AD22	28
PR0_PRU1_GPO13	PRU-ICSS0 PRU1 DATA OUT	O	AE23	23
PR0_PRU1_GPO14	PRU-ICSS0 PRU1 DATA OUT	O	AD23	21
PR0_PRU1_GPO15	PRU-ICSS0 PRU1 DATA OUT	O	AE24	15
PR0_PRU1_GPO16	PRU-ICSS0 PRU1 DATA OUT	O	AE18	32
PR0_PRU1_GPO17	PRU-ICSS0 PRU1 DATA OUT	O	AB18	46
PR0_PRU1_GPO18	PRU-ICSS0 PRU1 DATA OUT	O	H22	8
PR0_PRU1_GPO19	PRU-ICSS0 PRU1 DATA OUT	O	K24	6
PR0_PRU1_GPO2	PRU-ICSS0 PRU1 DATA OUT	O	AC23	26
PR0_PRU1_GPO3	PRU-ICSS0 PRU1 DATA OUT	O	AE21	13
PR0_PRU1_GPO4	PRU-ICSS0 PRU1 DATA OUT	O	K25	66
PR0_PRU1_GPO5	PRU-ICSS0 PRU1 DATA OUT	O	J24	67
PR0_PRU1_GPO6	PRU-ICSS0 PRU1 DATA OUT	O	B23	74
PR0_PRU1_GPO7	PRU-ICSS0 PRU1 DATA OUT	O	A23	73
PR0_PRU1_GPO8	PRU-ICSS0 PRU1 DATA OUT	O	A22	78
PR0_PRU1_GPO9	PRU-ICSS0 PRU1 DATA OUT	O	A24	76

PRU-ICSS0/UART0 Signals:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR0_UART0_CTS_N	UART CLEAR TO SEND	I	P23	86
PR0_UART0_RTS_N	UART REQUEST TO SEND	O	T22	71
PR0_UART0_RXD	UART RECEIVE DATA	I	T21	69
PR0_UART0_TXD	UART TRANSMIT DATA	O	T20	70

4.17.2. PRU-ICSS1 Interface

PRU-ICSS1-PRU0/General Purpose Inputs Signals:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR1_PRU0_GPI0	PRU-ICSS1 PRU0 DATA IN	I	B22	75
PR1_PRU0_GPI1	PRU-ICSS1 PRU0 DATA IN	I	A21	80
PR1_PRU0_GPI10	PRU-ICSS1 PRU0 DATA IN	I	E11	116
PR1_PRU0_GPI11	PRU-ICSS1 PRU0 DATA IN	I	C11	150
PR1_PRU0_GPI16	PRU-ICSS1 PRU0 DATA IN CAPTURE ENABLE	I	B11, C24, D24, K21, L21	111, 119, 135,
PR1_PRU0_GPI2	PRU-ICSS1 PRU0 DATA IN	I	B21	77
PR1_PRU0_GPI3	PRU-ICSS1 PRU0 DATA IN	I	C21	132
PR1_PRU0_GPI4	PRU-ICSS1 PRU0 DATA IN	I	A20	82
PR1_PRU0_GPI5	PRU-ICSS1 PRU0 DATA IN	I	B20	79

PR1_PRU0_GPI6	PRU-ICSS1 PRU0 DATA IN	I	C20	127
PR1_PRU0_GPI7	PRU-ICSS1 PRU0 DATA IN	I	E19	128
PR1_PRU0_GPI8	PRU-ICSS1 PRU0 DATA IN	I	B9	NO
PR1_PRU0_GPI9	PRU-ICSS1 PRU0 DATA IN	I	F10	NO

PRU-ICSS1-PRU0/General Purpose Outputs Signals:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR1_PRU0_GPO0	PRU-ICSS1 PRU0 DATA OUT	O	B22	75
PR1_PRU0_GPO1	PRU-ICSS1 PRU0 DATA OUT	O	A21	80
PR1_PRU0_GPO10	PRU-ICSS1 PRU0 DATA OUT	O	E11	116
PR1_PRU0_GPO11	PRU-ICSS1 PRU0 DATA OUT	O	C11	150
PR1_PRU0_GPO2	PRU-ICSS1 PRU0 DATA OUT	O	B21	77
PR1_PRU0_GPO3	PRU-ICSS1 PRU0 DATA OUT	O	C21	132
PR1_PRU0_GPO4	PRU-ICSS1 PRU0 DATA OUT	O	A20	82
PR1_PRU0_GPO5	PRU-ICSS1 PRU0 DATA OUT	O	B20	79
PR1_PRU0_GPO6	PRU-ICSS1 PRU0 DATA OUT	O	C20	127
PR1_PRU0_GPO7	PRU-ICSS1 PRU0 DATA OUT	O	E19	128
PR1_PRU0_GPO8	PRU-ICSS1 PRU0 DATA OUT	O	B9	NO
PR1_PRU0_GPO9	PRU-ICSS1 PRU0 DATA OUT	O	F10	NO

PRU-ICSS1/eCAP Signal:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	
PR1_ECAP0_ECAP_CAP	ENHANCED CAPTURE INPUT OR	IO	A11, G24	137, 68

PRU-ICSS1/ECAT Signal:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR1_EDC_LATCH0_IN	DATA IN	I	AE22, K22	30, 124
PR1_EDC_LATCH1_IN	DATA IN	I	AD22, L22	28, 120
PR1_EDC_SYNC0_OUT	DATA OUT	O	L25	61
PR1_EDC_SYNC1_OUT	DATA OUT	O	J25	64
PR1_EDIO_DATA_IN0	DATA IN	I	AD23	21
PR1_EDIO_DATA_IN1	DATA IN	I	AE24	15
PR1_EDIO_DATA_IN2	DATA IN	I	B23	74
PR1_EDIO_DATA_IN3	DATA IN	I	A23	73
PR1_EDIO_DATA_IN4	DATA IN	I	A22	78
PR1_EDIO_DATA_IN5	DATA IN	I	A24	76
PR1_EDIO_DATA_IN6	DATA IN	I	B9, C20	120
PR1_EDIO_DATA_IN7	DATA IN	I	E19	128
PR1_EDIO_DATA_OUT	DATA OUT	O	T21	69
PR1_EDIO_DATA_OUT	DATA OUT	O	T20	70

PR1_EDIO_DATA_OUT	DATA OUT	O	B23	74
PR1_EDIO_DATA_OUT	DATA OUT	O	A23	73
PR1_EDIO_DATA_OUT	DATA OUT	O	A22	78
PR1_EDIO_DATA_OUT	DATA OUT	O	A24	76
PR1_EDIO_DATA_OUT	DATA OUT	O	B9, C20	120
PR1_EDIO_DATA_OUT	DATA OUT	O	E19	128
PR1_EDIO_LATCH_IN	LATCH IN	I	AE23	23
PR1_EDIO_OUTVALID	DATA OUT VALID	O	AD18	197
PR1_EDIO_SOF	START OF FRAME	O	AB25,	25,199

PRU-ICSS1/MDIO Signal:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR1_MDIO_DATA	MDIO DATA	IO	A17	42
PR1_MDIO_MDCLK	MDIO CLK	O	B17	40

PRU-ICSS1/MII0 Signals:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR1_MII0_COL	MII COLLISION DETECT	I	D25	114
PR1_MII0_CRS	MII CARRIER SENSE	I	B12, G20	NO
PR1_MII0_RXD0	MII RECEIVE DATA BIT 0	I	B18	129
PR1_MII0_RXD1	MII RECEIVE DATA BIT 1	I	A18	123
PR1_MII0_RXD2	MII RECEIVE DATA BIT 2	I	B19	81
PR1_MII0_RXD3	MII RECEIVE DATA BIT 3	I	A19	126
PR1_MII0_RXDV	MII RECEIVE DATA VALID	I	D17	144
PR1_MII0_RXER	MII RECEIVE DATA ERROR	I	D19	133
PR1_MII0_RXLINK	MII RECEIVE LINK	I	C19	142
PR1_MII0_TXD0	MII TRANSMIT DATA BIT 0	O	B11, B20	135, 79
PR1_MII0_TXD1	MII TRANSMIT DATA BIT 1	O	A20, C11	82, 150
PR1_MII0_TXD2	MII TRANSMIT DATA BIT 2	O	C21, E11	132,
PR1_MII0_TXD3	MII TRANSMIT DATA BIT 3	O	B21, D11	77
PR1_MII0_TXEN	MII TRANSMIT ENABLE	O	A21, F11	80
PR1_MII_MR0_CLK	MII RECEIVE CLOCK	I	C17	146
PR1_MII_MT0_CLK	MII TRANSMIT CLOCK	I	B10, B22	75

PRU-ICSS1/MII1 Signals:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR1_MII1_COL	MII COLLISION DETECT	I	F24	63
PR1_MII1_CRS	MII CARRIER SENSE	I	A2	131
PR1_MII1_RXD0	MII RECEIVE DATA BIT 0	I	D8	16
PR1_MII1_RXD1	MII RECEIVE DATA BIT 1	I	G8	18

PR1_MII1_RXD2	MII RECEIVE DATA BIT 2	I	B4	20
PR1_MII1_RXD3	MII RECEIVE DATA BIT 3	I	F7	22
PR1_MII1_RXDV	MII RECEIVE DATA VALID	I	C5	14
PR1_MII1_RXER	MII RECEIVE DATA ERROR	I	B3	151
PR1_MII1_RXLINK	MII RECEIVE LINK	I	C10,E24	109,115
PR1_MII1_TXD0	MII TRANSMIT DATA BIT 0	O	E7	1
PR1_MII1_TXD1	MII TRANSMIT DATA BIT 1	O	D7	3
PR1_MII1_TXD2	MII TRANSMIT DATA BIT 2	O	A4	5
PR1_MII1_TXD3	MII TRANSMIT DATA BIT 3	O	C6	7
PR1_MII1_TXEN	MII TRANSMIT ENABLE	O	C3	11
PR1_MII_MR1_CLK	MII RECEIVE CLOCK	I	F6	12
PR1_MII_MT1_CLK	MII TRANSMIT CLOCK	I	E8	9

PRU-ICSS1/UART0 Signals:

SIGNAL NAME	DESCRIPTION	TYPE	ZDN	PIN
PR1_UART0_CTS_N	UART CLEAR TO SEND	I	K22, P23	124, 86
PR1_UART0_RTS_N	UART REQUEST TO SEND	O	L22, T22	120, 71
PR1_UART0_RXD	UART RECEIVE DATA	I	K21, T21	111, 69
PR1_UART0_TXD	UART TRANSMIT DATA	O	L21, T20	119, 70

4.18. JTAG

The SoM includes JTAG interface to provide a debug and test control. Seven signals are routed from the APQ directly to J4 (1.27 pitch 5x2 pin header Sullins P/N: GRPB052VWVN-RC or compatible).

JTAG Signals:

AM437x SIGNAL NAME	ZDN BALL	DESCRIPTION	JTAG PIN#
GND		Ground Power	1
JTAG_TRSTN	Y25	JTAG TEST RESET (ACTIVE LOW)	2
JTAG_EMU0	N23	MISC EMULATION PIN	3
JTAG_TMS	Y24	JTAG TEST MODE SELECT	4
GND		Ground Power	5
JTAG_TDI	Y20	JTAG TEST DATA INPUT	6
JTAG_EMU1	T24	MISC EMULATION PIN	7
JTAG_TCK	AA25	JTAG TEST CLOCK	8
SYS_RESETn	G22	System Reset	9
JTAG_TDO	AA24	JTAG TEST DATA OUTPUT	10

4.19. Wi-Fi and Bluetooth

The VAR-SOM-AM43 contains a certified high performance WL183xMOD 2.4/5 GHz IEEE 802.11 a/b/g/n Bluetooth 5.1/BLE with CSA2 support radio module, with optional Dual Band and MIMO support. The two antennas connect through U.FL JACK connectors.
Antenna cable connected to module must have 50-Ω impedance.

4.20. Power

4.20.1. Power Supply pins

Power Signals:

SIGNAL NAME	TPS65218 and AM437x pins	DESCRIPTION	EDGE CONNECTOR
VBAT		Power input for PMIC VIN and V3_3SW voltage	100,102,103, 104,105,107
VDDSHV11	H8,H9,H11,G11	VDDSHV9, VDDSHV11Power domains Output voltage	134
VDDA_ADC	AB12	ADC0 Power supply Output	110
ADC0_VREFP	AD14	Analog Positive Reference Input	164

4.20.2. GND pins

GND Pins:

SIGNAL NAME	TYPE	DESCRIPTION	EDGE CONNECTOR
GND	Ground Power	Power	10,19,24,29,35,41,44,47,53,72, 85,93,96,101,106,108,118,121,130, 165,185, 200,202,203,204
AGND_AUD	Audio Ground	Reference GND for audio signals	170
GNDA_ADC	ADC0 Analog Ground	ADC0 Analog Ground	112
ADC0_VREFN	ADC0 Analog Ground Reference	Analog Negative Reference Input	166

5. Absolute Maximum Characteristics

SIGNAL NAME	Min	Typ	Max	Unit
Main Power Supply, VBAT	-0.3	3.3	3.8	V
Digital IOs:	-0.5V	1.8, 3.3	VIO + 0.3 V	V
Analog IOs:	-0.5V	1.8	V1.8D + 0.3V	V
ADC0_VREFP	164	1.15V	1.8	V
ADC0_VREFN	166	0	0.65	V

6. Operating Characteristics

6.1. Normal Operational Conditions

Unless otherwise specified, all DC and AC specifications in this data sheet are valid for the following voltages and temperature ranges.

Parameter	Symbol	Min.	Typical	Max.	Units
Input Power Supply	3.3V	3.15	3.3	3.45	V_{DC}

6.2. Power Consumption

	Min	Typ	Max	Unit
Main Power Supply – Excluding Wi-Fi			4.95	W
Wi-Fi transmit			1.0	W
Gbit Ethernet			0.4	W

6.3. DC Electrical Characteristics

Parameter	**Min**	**Typ**	**Max**	**Unit**
LVCMOS pins (VDDSHVx = 3.3 V; x=1-11)				
VIH	1.17			V
VIL			0.63	V
VOH	1.35			V
VOL			0.45	V
LVCMOS pins (VDDSHVx = 1.8 V; x=1-11)				
VIH	2			V
VIL			0.8	V
VOH	2.85			V
VOL			0.45	V
Analog IOs: AIN 0-7				
VDC	0		1.8	V
EXCEPTIONS	**Min**	**Typ**	**Max**	**Unit**
TCK (VDDSHV3 = 3.3 V)				
VIH	2.15			V
VIL			0.46	V

VHYS	0.4			V
PWRONRSTn (VDDSHV3 = 1.8 V or 3.3 V)(1)				
VIH	1.35			V
VIL			0.5	V
VHYS	0.07			V

Parameter		**Min**	**Typ**	**Max**	**Unit**
SUPPLY NAME	DESCRIPTION				
USB0_VBUS	Voltage range for USB VBUS comparator input	0.000	5.000	5.250	V
USB1_VBUS	Voltage range for USB VBUS comparator input	0.000	5.000	5.250	V
USB0_ID	Voltage range for the USB ID input	(1)			V
USB1_ID	Voltage range for the USB ID input	(1)			V

(1) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSSA_USB with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.

7. Environmental Specifications

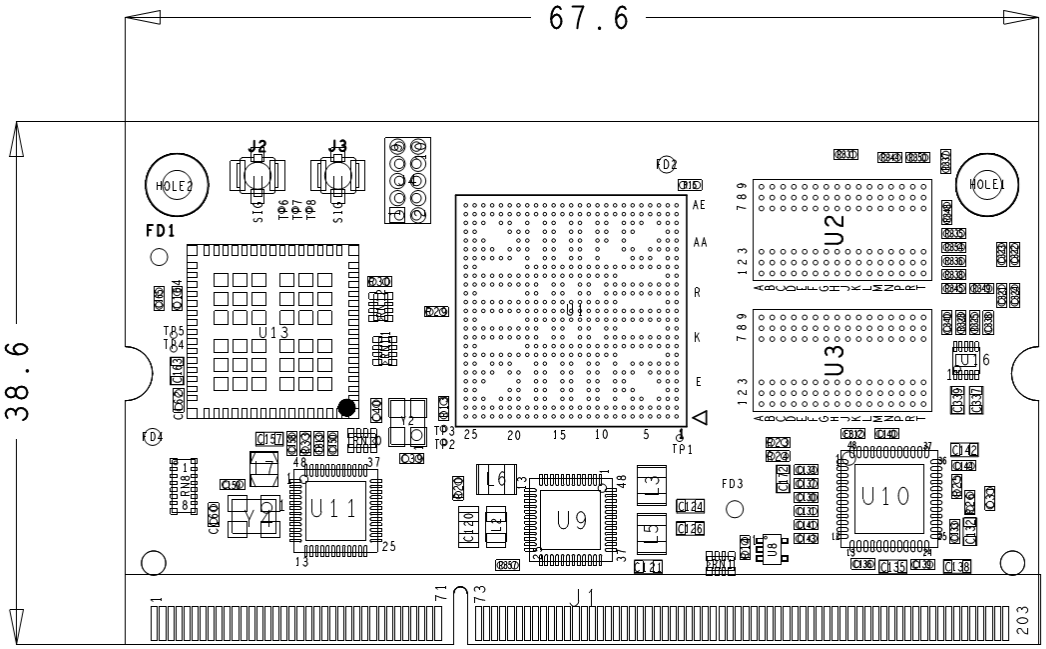
Parameter	MIN	MAX
Commercial Operating temperature	0°C	+70 °C
Extended Operating temperature	-20°C	+70 °C
Industrial Operating temperature	-40°C	+85 °C
Referring Telcordia Technologies Special Report SR-332, Issue 3 Reliability Prediction Method Model: With WiFi module 25Deg Celsius, Class B-1, GM 25Deg Celsius, Class B-1, GF 25Deg Celsius, Class B-1, GB Without WiFi module 25Deg Celsius, Class B-1, GM 25Deg Celsius, Class B-1, GF 25Deg Celsius, Class B-1, GB	 1333 Khrs > 3094 Khrs > 6047 Khrs > 2573 Khrs > 5600 Khrs > 11201 Khrs >	
Shock Resistance	50G/20 ms	
Vibration	20G/0 - 600 Hz	

Note: Extended and Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

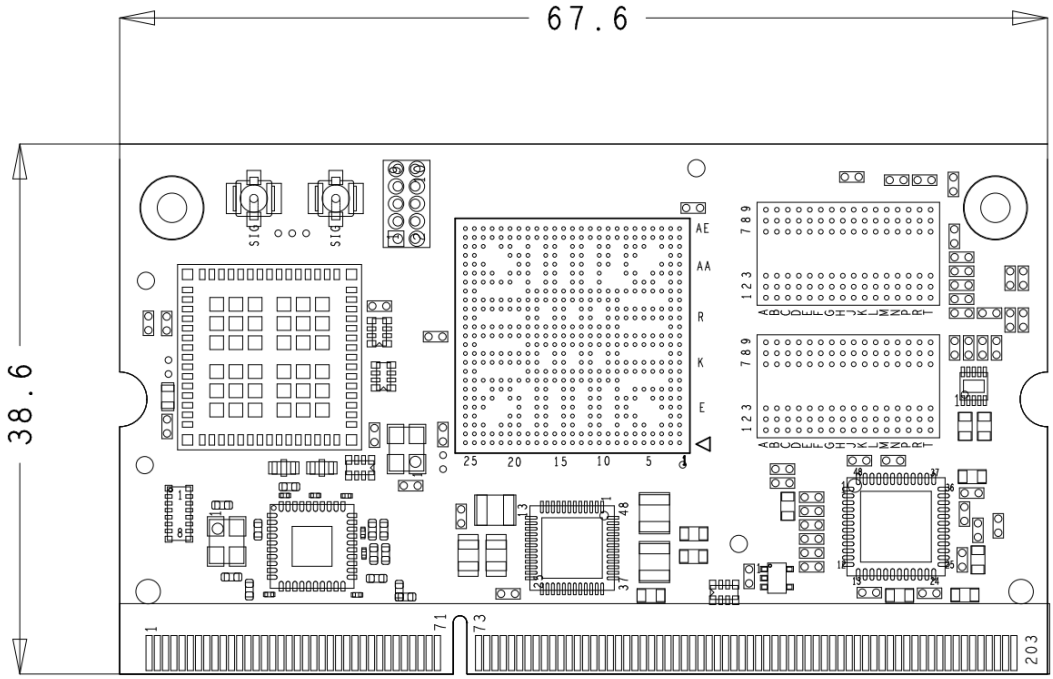
8. Mechanical Specifications

8.1. Drawing

V1.1 (AR8033 PHY)



V1.2 (ADIN1300 PHY)

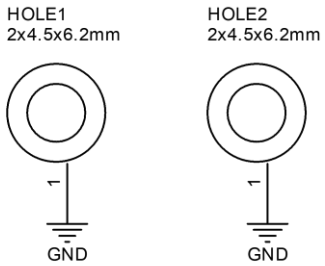


CAD file are available for download at http://www.variscite.com/

8.2. SoM Fastening

For extra mechanical strength, required for operating in extreme vibration & shock conditions, The VAR-SOM-AM43 can be fasten to the carrier board, using the two mechanical holes.

All the holes are to be located symmetrically. The holes plated inside and connected to GND.



In TOP side a pad has diameter 180mil (accordance to top of screw).

In BOTTOM side a pad has diameter 244mil (according to STANDOFF).

A drill diameter 85mil.

The STANDOFF has good thermal and electrical conductivity. It help for the SOM cooling, good GND connection and reduce EMI.

Part	Description	Manufacturer, PN
Standoff	SMT SPACER M2x0.4mm, H=3mm	PennEngineering, P/N: SMTSO-M2-3-ET
Screw	M2x0.4mm, length = 4mm	Essentra Components, NSE-1207-M2-4
Washer	FLAT M2 STEEL	B&F Fastener Supply, MFWZ 002
Washer	SPLIT LOCK M2 STEEL	B&F Fastener Supply, MLWZ 002

9. Literature

1. AM437x ARM® Cortex™-A9 Microprocessors (MPUs), (literature number SPRS851)
2. AM437x ARM® Cortex™-A9 Microprocessors (MPUs) Technical Reference Manual (literature Number: SPRUHL7)

10. RoHS compliance

VAR-SOM-AM43 System-on-Module complies with the European Union Restriction on Use of Hazardous Substance Directive 2002/95/EC (“RoHS 1”), Directive 2011/65/EU (“RoHS 2”) as well as the China Management Methods for controlling Pollution by Electronic information Products (“China RoHS”) as defined and detailed inVariscite’s website:

http://www.variscite.com/company/product-compliance-policy

11. Ordering Information

Please refer to www.variscite.com

12. Warranty Terms

Variscite guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Variscite's sole liability shall be for Variscite, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

12.1. Disclaimer of Warranty

THIS WARRANTY IS MADE IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

12.2. Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL VARISCITE BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL VARISCITE BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT.

13. About Variscite

For over a decade Variscite has developed, produced and manufactured a powerful range of System on Modules, consistently setting market benchmarks in terms of speed and innovation.

The company's portfolio is based on leading SoC vendors including Texas Instruments, Freescale, and Marvell.

All Variscite production is performed at fully ISO 13485 compliant facilities, satisfying international customer and regulatory requirements for a broad range of industries including medical devices and related services. The company's production facilities are equipped with the most advanced SMT machines that ensure punctual deliveries and high quality products.

Having first entered the embedded market in 2003 with specialized designs for a variety of industrial applications, Variscite has continued to innovate and be first-to-market. Just some System on Module launch highlights include the release of the first Cortex-A8 SOM back in 2009 and on 2011, Breaking the speed record again with the first TI OMAP4460-based, 1.5GHz Cortex-A9 System on Module.

It's no surprise that within a decade Variscite has taken a leading position in the design and manufacture of system on modules. Variscite serves more than 1,500 customers in over 50 countries worldwide, delivering a cost effective, high performance portfolio that combines interface flexibility with advanced power management.

A trusted provider of development and consulting services for a variety of embedded platforms, Variscite transforms clients' visions into successful products.

Our Mission

To innovate with future-proof solutions, well ahead of the market

To provide comprehensive, rapid and premier technical support throughout the design cycle

To deliver a one-stop-shop for total System on Module solutions and design services

13.1. Contact Information

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