VARISCITE LTD.

VAR-SOM-MX25 Datasheet

Freescale™ i.MX25x based System-on-Module

Rev1.1A

VARISCITE LTD.

VAR-SOM-MX25 Data Sheet

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Revision History

Revision	Date	Notes
1.0	06/12/2009	First Release - Preliminary
1.1	17/10/2010	-Table 3.1 Pin 34,48,51,126 Function update Pin 53,63 - Description Typo Correction. -Tables 4-5,4-11,4-13,4-14,4-17,4-21 - Pin number correction. - Adding LCDC bus signals functions in 18pbb configuration.
	02/02/10	Removing Pin 184 (GPIO4[12]) Now - NC
	08/03/10	Adding I2C Address used by SOM

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1 Overview

This chapter gives a short overview of the VAR-SOM-MX25

1.1 General Information

The VAR-SOM-MX25 is a highly integrated, cost optimized, low-power System-On-Module, which serves as a building block for embedded solutions. The module is based on the Freescale™ i.MX25x high performance, low power multimedia applications processors family. It includes all vital peripherals/interfaces, and is ready to run any embedded operating system such as Linux, WinCE and Windows Mobile.

Supported products & documents:

- Windows Embedded CE 6.0 R3 BSP
- Linux BSP based on kernel 2.6.31
- VAR-MX25CustomBoard
- VAR-DVK-MX25
  - ✓ VAR--MX25CustomBoard populated with VAR-SOM-MX25
  - ✓ *7", TFT LCD*
  - ✓ Windows CE 6.0 run-time image
  - ✓ Linux Kernel 2.6.31 sources files
  - ✓ Schematics

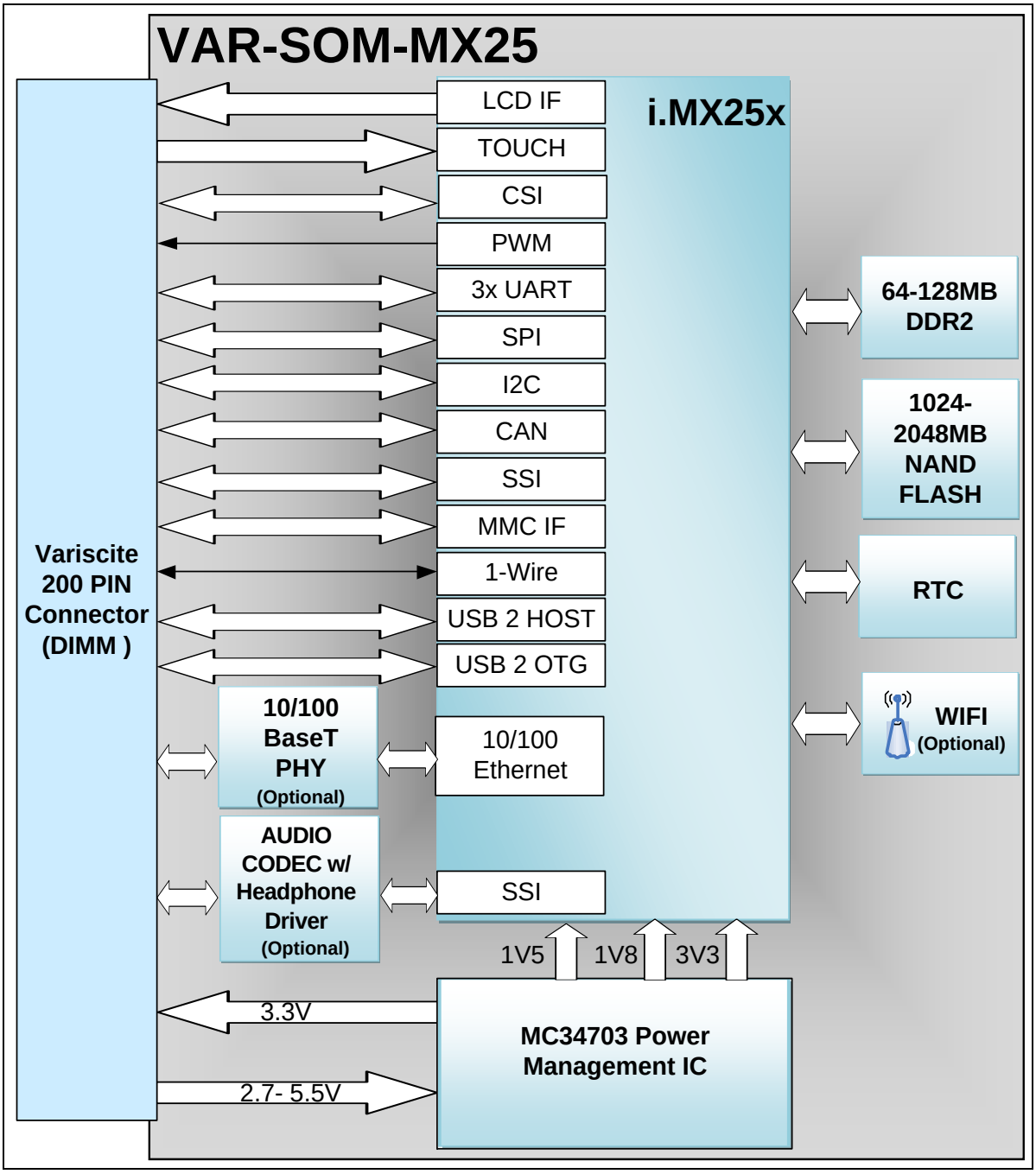
Contact support for further information: mailto:support@variscite.com.

1.2 Feature Summary

- Freescale™ i.MX25x SoC
  - 400-MHz ARM ARM926EJ-S™ Core
  - 16kB/16KB Inst/ Data L1 cache
  - Internal 128KB SRAM
- 64-128MB, 266MHz DDR2 SDRAM.
- 128-2048 MBytes Flash Disk
- 10/100BaseT Ethernet port.
- LCD interface.
- Touch Screen interface.
- CMOS Sensor Interface.
- SD card/SDIO/MMC card interface.
- Power
  - Single 2.6-5.5V power supply (One lithium-ion cell battery)
  - Typical power consumption: 1W
- 3 UART ports serve as interfaces with GSM/GPRS modem, Bluetooth devices as well as IRDA & debug port.
- Audio
  - ADC and DAC Sampling Frequency: 8KHz – 96KHz
  - Microphone input
  - Line Out
  - Synchronous Serial Interface supports I2S & AC97
- USB
  - FS USB 2.0 Host interface
  - HS USB 2.0 OTG interface
- RTC
- Serial controllers
  - SPI interface
  - Synchronous Serial Interface
  - I2C interface
  - 1 – Wire/ HDQ
  - CAN interface

1.3 Block Diagram

Figure 1



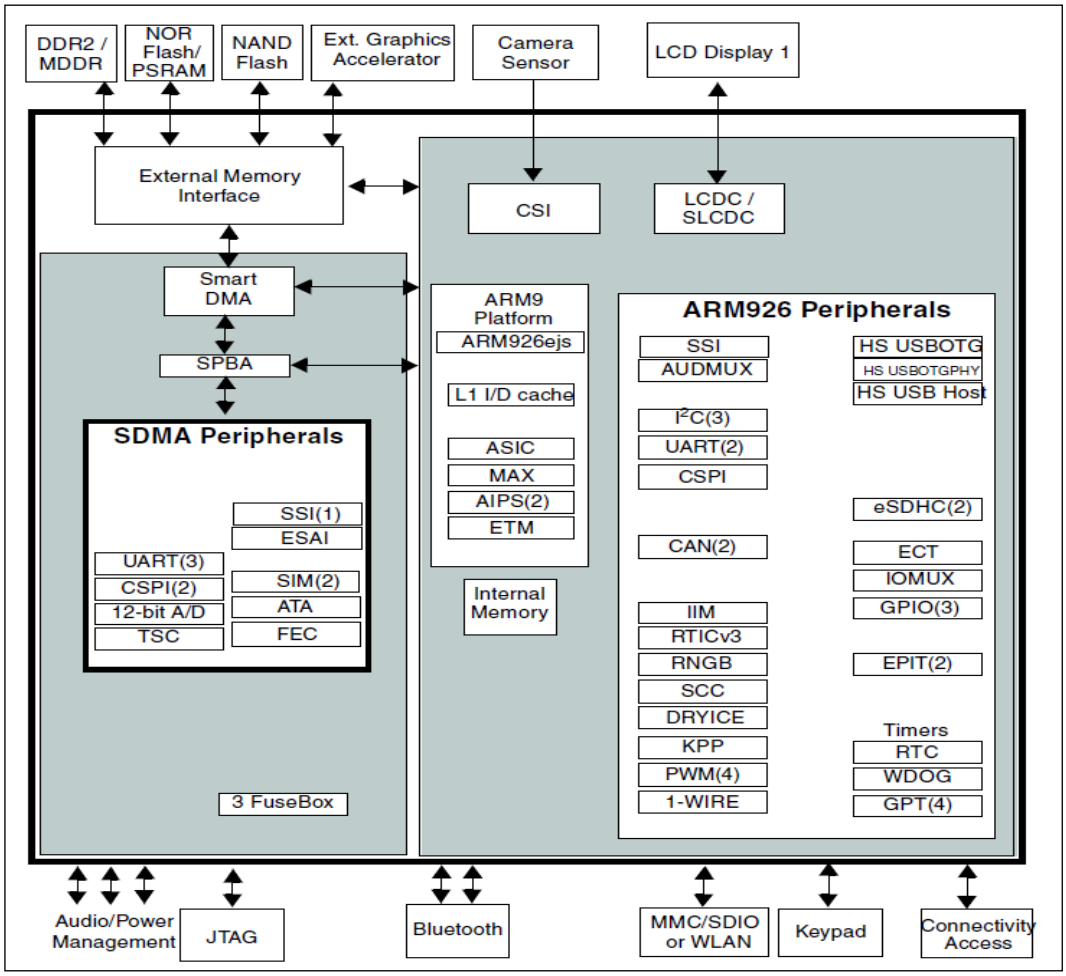
2 HW Components

This chapter briefly describes the components of the VAR-SOM-MX25 HW.

2.1 FreescaleTM i.MX25x

2.1.1 Freescale™ i.MX25x Block Diagram

Figure 2-1



2.1.2 MPU Subsystem

The MPU subsystem integrates 400 MHz ARM 926EJ-S™ arm core

2.1.3 On-Chip Memory

- Level 1 cache

- Instruction (16 KB)
- Data (16 KB)

- Level 2 memory

  - Boot ROM, including HAB (32 KB)
  - Internal RAM (128 KB)
  - Secure RAM (2 KB)

- 128 KB s multi-purpose SRAM

2.1.4 DMA Controller

i.MX25x SDMA main features:

- Multi-channel DMA, supporting up to 32 time-division multiplexed DMA channels.
- Hardware or software driven triggers for each channel.
- 48 hardware driven triggers that can be mapped to any channel.
- Memory access, including linear addressing, FIFO addressing and 2D addressing.

2.1.5 Multimedia support

- LCD Controller

  - Display controller supporting black-and-white, grayscale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels.
  - Color and monochrome displays up to 800 × 600 resolution
  - 256K colors/Gray scale levels

- CSI – CMOS Sensor Interface

  - Configurable interface logic, supporting most commonly available CMOS sensors.
  - Support for the CCIR656 video interface, as well as traditional sensor interfaces.
  - 8-bit data port for YCC, YUV, or RGB data input.
  - 8-bit/10-bit/16-bit data port for Bayer data input.

- SSI Synchronous Serial Interface.

  The full-duplex serial port allows the i.MX25 to communicate with a variety of serial devices. These serial devices can be standard CODer-DECoder (CODECs), Digital Signal Processors (DSPs), microprocessors, peripherals, and popular industry audio CODECs that implement both the inter-IC sound bus (I2S) and Intel AC97 standards.

2.1.6 Peripherals

The i.MX25 device supports a comprehensive set of peripherals, providing flexible and high-speed interfacing, in addition to on-chip programming resources. Table 2-1 provides a list and descriptions of the peripherals available on i.MX25x devices.

Table 2-1 – i.MX25 Peripherals

Type	Name	Description
Serial Communication	CSPI - Configurable serial peripheral interface	This module is a serial interface equipped with data FIFOs. Each master/slave-configurable SPI module is capable of interfacing with either serial port interface master or slave devices. The CSPI ready (SPI_RDY) and slave select (SS) control signals enable fast data communication with fewer software interrupts.
	I2C module	Inter-IC Communication (I2C) is an industry standard, bidirectional serial bus that provides a simple and efficient method of data exchange, minimizing the interconnection between devices. I2C is suitable for applications requiring occasional communications over a short distance between many devices. The interface operates up to 100 kbps with maximum bus loading and timing.
	USBOTG USBHOST	The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 Low Pin Count specification. The module has DMA capabilities for handling data transfer between internal buffers and system memory. OTG HS PHY and HOST FS PHY are also integrated.
	FlexCAN	The controller area network (CAN) protocol is primarily designed to be used as a vehicle serial data bus running at 1 Mbps.
	UART (Universal Asynchronous)	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words • one or two stop bits • programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz (This is a higher maximum baud rate than the 1.875 MHz required by both the TIA/EIA-232-F standard and (prior) Freescale™ UART modules). 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA-1.0 support (up to SIR speed of 115200 bps)Option to operate as 8-pin full UART, DCE, or DTE
	1-Wire Interface	1-Wire support is provided for interfacing with an on-board EEPROM, and with smart battery interfaces, e.g. Dallas DS2502.

Removable Media	Multimedia Card/Secure Digital/Secure Digital I/O(MMC/SDIO) Card Interface (eSDHC)	The features of the eSDHC module, when serving as a host, include the following: • Conforms to the SD host version 2.0 controller standard specification • Compatible with the JEDEC MMC system specification version 4.2 • Compatible with the SD memory card specification version 2.0 • Compatible with the SDIO specification version 1.2 • Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full/high-speed mode • Host clock frequency variable between 32 KHZ and 52 MHz • Up to 200-Mbps data transfer for SD/SDIO cards, using four parallel data lines • Up to 416-Mbps data transfer for MMC cards, using eight parallel data lines
Miscellaneous	4 GPT timers	Each GPT is a 32-bit free-running or set-and-forget mode timer with a programmable prescaler, and a compare-and-capture register. A timer counter value can be captured using an external event, and it can also be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals, with minimal processor intervention. The counter has output comparison logic, and can provide the status and interrupt when compared. This timer can be configured to either run on an external or internal clock.
	Watchdog timer	One watchdog timer (WDT)
	AUDMUX	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data-routing. This connects host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals, and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.
	General-purpose input/output (GPIO)	General-purpose input/output pins controlled by four 32 bit GPIO controllers.
	FEC	The Ethernet media access controller (MAC) is designed to support both 10 and 100 Mbps Ethernet networks, compliant with IEEE 802.3® standard. An external transceiver interface, and transceiver functions are required to complete the interface to the media
	Control module	I/O multiplexing and chip-configuration control.

2.2 MC34704 PMIC

The VAR-SOM-MX25 uses the MC34704 companion chip. The PMIC supplies all required power rails and power sequencing for the on-board VAR-SOM-MX25 devices, in addition to dedicated 3.3V power rails for a VAR-SOM-MX25 based board.

2.3 Memory

2.3.1 266MHZ DDR2 SDRAM

The VAR-SOM-MX25 supports 266 MHz, 64-128MB DDR2 memory.

2.3.2 Non volatile storage memory

The VAR-SOM-MX25 supports 128-2048MB NAND Flash. The NAND flash is used as a Flash Disk, storing the operating system's run-time-images and the Boot loader (Boot from NAND).

2.4 SMSC LAN8700 Ethernet PHY

The VAR-SOM-25x integrates the SMSC LAN87000 device, for 10/100 BaseT Ethernet connectivity. The SMSC LAN8700 is an analog IF IC, with HP Auto-MDIX support for high performance embedded Ethernet applications.

The LAN8700 is compliant with IEEE 802.3-2005 standards and supports both IEE 802.3-2005 complaint and vendor specific register function. It contains a full-duplex 10-BASE-T/100BASE-Tx transceiver, and supports 10-Mbps (10BASE-T) operation on category 3 and category 5 unshielded twisted–pair cable, in addition to 100-Mbps (100BASE-Tx) operation on category 5 unshielded twisted pair cable.

Qualified and Suggested Magnetics:

Please refer to the SMSC web site for more updated information about supported magnetic.

http://www.smsc.com/media/Downloads/Application_Notes/an813.pdf

2.5 Audio CODEC (Optional)

The VAR-SOM-MX25 Audio Interface is supported by Wolfson Microelectronics WM8731L Device . The device has a low power CODEC with an integrated headphone driver. Please refer to WM8731 data sheet for more details.

http://www.wolfsonmicro.com/uploads/documents/en/WM8731_Rev4.3.pdf

2.6 RTC (Optional)

On-board RTC functionality is supported by the Intersil ISL12057 device. 3V backup voltage is required on module's pin#126 for RTC data maintenance during system shutdown.

3 SOM Connectors

The VAR-SOM-MX25 exposes an SO–DIMM 200 pin mechanical standard interface. The recommended mating connector for base board interfacing is FCI 10033853-052FSLF or equivalent.

SOM connector signal list:

Table 3-1 – VAR-SOM-MX25 Pin Out

Pin #	Pin Default Function	Type	Main Function Description	GPIO #
1	CAN_Rx1	I	CAN BUS Rx Data	GPIO1[3]
2	CAN_Tx1	O	CAN BUS TxData	GPIO1[2]
3	LCDC_LD1	O	Display Data BUS [1]	GPIO2[16]
4	LCDC_LD0	O	Display Data BUS [0]	GPIO2[15]
5	LCDC_LD3	O	Display Data BUS [3]	GPIO2[18]
6	LCDC_LD2	O	Display Data BUS [2]	GPIO2[17]
7	LCDC_LD5	O	Display Data BUS [5]	GPIO1[19]
8	LCDC_LD4	O	Display Data BUS [4]	GPIO2[19]
9	GPIO4[5]	I/O		
10	CSPI1_RDY	O	CSPI RDY	GPIO2[22]
11	LCDC_LD7	O	Display Data BUS [7]	
12	LCDC_LD6	O	Display Data BUS [6]	
13	LCDC_LD9	O	Display Data BUS [9]	
14	LCDC_LD8	O	Display Data BUS [8]	
15	LCDC_LD11	O	Display Data BUS [11]	
16	LCDC_LD10	O	Display Data BUS [10]	
17	GPIO4[6]	I/O		
18	CSI_D5	I	CMOS Interface Data[5]	GPIO2[30]
19	LCDC_LD13	O	Display Data BUS [13]	
20	LCDC_LD12	O	Display Data BUS [12]	
21	LCDC_LD15	O	Display Data BUS [15]	
22	LCDC_LD14	O	Display Data BUS [14]	
23	LCDC_LD17	O	Display Data BUS [17]	GPIO1[5]

24	LCDC_LD16	O	Display Data BUS [16]	GPIO1[4]
25	CSI_MCLK_MMC2_ DAT0	O	CMOS Sensor Interface MCLK, MMC2_DAT0 (1)	GPIO1[8]
26	LCDC_LHSYNC	O	LCD Horizontal Sync	GPIO1[22]
27	NC			
28	LCDC_LPCLK	O	LCD Pixel Clock	GPIO1[24]
29	UART1_CTS	I	UART#3 CTS	GPIO4[24]
30	NC			
31	UART1_RTS	O	UART#1 RTS	GPIO4[24]
32	MMC1_CLKO	O	MMC#1 Clock	GPIO2[24]
33	UART1_Rx	I	UART#1 Rx	GPIO4[22]
34	GND		Digital GND	
35	UART1_Tx	O	UART#1 Tx	GPIO4[23]
36	MMC1_DAT0	I/O	MMC#1 Data 0	GPIO2[25]
37	CSPI1_CLK	O	CSPI#1 Clock	GPIO1[18]
38	MMC1_DAT1	I/O	MMC#1 Data 1	GPIO2[26]
39	CSPI1_SIMO	O	CSPI#1 SIMO (Tx)	GPIO1[14]
40	MMC1_DAT2	I/O	MMC#1 Data 2	GPIO2[27]
41	CSPI_SOMI	I	CSPI#1 SOMI (Rx)	GPIO1[15]
42	MMC1_DAT3	I/O	MMC#1 Data 3	GPIO2[28]
43	MMC1_CMD	I/O	MMC#1 Command	GPIO2[23]
44	CSI_D6_MMC2_CMD	I	CMOS Sensor Interface Data[6] , MMC2_ CMD(1)	GPIO1[31]
45	NC			
46	LCDC_LVSYNC	O	LCD Vertical Sync	GPIO1[23]
47	GND	Power	Digital GND	
48	GND		Digital GND	
49	WIPER	Analog Input	Touch Wiper	
50	CSI_D4	I	CMOS Interface Data[4]	GPIO1[29]
51	GND	O	PWM1	GPIO1[26]

52	NC			
53	CSI_D7__MMC2_CLK	I	CMOS Sensor Interface Data[7] , MMC2_CLK(1)	GPIO1[6]
54	NC			
55	CSI_D3	I/O	CMOS Interface Data[3]	GPIO1[27]
56	CSI_D2	I/O	CMOS Interface Data[2]	GPIO1[27]
57	NC			
58	GND	Power	Digital GND	
59	CSI_PIXCLK_MMC2_DAT3	I/O	CMOS Sensor Interface PIXCLK MMC2_DAT3(1),	GPIO1[11]
60	GND	Power	Digital GND	
61	I2C1_DATA	I/O	I2C#1 SDA (data), Internally pulled up.	GPIO1[13]
62	CSPI_CS1	O	SPI#1 Slave Select 1	
63	I2C1_CLOCK	O	I2C#1 SCL (clock) , Internally pulled up.	GPIO1[12]
64	LCDC_LDRDY	O	LCD AC bias/Data enable	GPIO1[25]
65	UART2_CTS	I	UART#2 CTS	GPIO4[29]
66	CSPI1_CS0	O	CSPI#1 Slave Select 0	GPIO1[16]
67	UART2_RTS	O	UART#2 RTS	GPIO4[28]
68	NC			
69	UART2_Tx	O	UART#2 Tx	GPIO4[27]
70	NC			
71	UART2_Rx	I	UART#2 Rx	GPIO4[26]
72	CSI_D9	I	CMOS Interface Data[9]	GPIO4[21]
73	TSPX(1)	I	Touch Screen X Plus	
74	CSI_D8	I	CMOS Interface Data[8]	GPIO1[7]
75	TSPY	I	Touch Screen Y Plus	
76	CSI_VSYNC_MMC2_DAT1	I/O	CMOS Sensor Interface VSYNC_,MMC2_DAT01(1)	GPIO1[9]
77	TSMX	I	Touch Screen X Minus	
78	CSI_HSYNC_MMC2_DAT2	I/O	CMOS Sensor Interface HSYNC , MMC2_DAT2 (1)	GPIO1[10]
79	TSMY	I	Touch Screen Y Minus	

80	GND	Power	Digital GND	
81	GND	Power	Digital GND	
82	OWire	I/O	OWire Line	GPIO3[14]
83	GND	Power	Digital GND	
84	UART3_Tx	O	UART#3 Tx	GPIO2[31]
85	NC			
86	UART3_RTS	O	UART#3 RTS, CMOS Sensor Interface Data[0]	GPIO2[31]
87	PWM1	PWM1	I.MX25x PWM4_PWM0 PWM#1	
88	UART3_CTS	I	UART#3 CTS, CMOS Sensor Interface Data[1]	GPIO3[0]
89	NC			
90	UART3_Rx	I	UART3_Rx	GPIO2[29]
91	MMC1_CD	I	MMC#1 Card Detect	GPIO3[17]
92	SYS_BOOT5	I	System Boot Option 5 [High – Burn Flash]	
93	NC			
94	NC			
95	NC			
96	NC			
97	POR	O	RESET OUT	
98	SSI5_SCK	I/O	Synchronous Serial Interface 5 Clock	GPIO3[3]
99	NC			
100	SSI5_STxFS	O	Synchronous Serial Interface 5 TxF	GPIO3[4]
101	NC			
102	SSI5_SRxD	I	Synchronous Serial Interface 5 Tx Data	GPIO3[2]
103	USBHOST_DP	I/O	USB 2.0 Host Data Positive	N/A
104	SSI5_STxD	O	Synchronous Serial Interface 5 Tx Data	GPIO3[1]

105	USBHOST_DM	I/O	USB 2.0 Host Data Negative	N/A
106	GND	Power	Digital GND	
107	NC			
108	NC			
109	GPIO3_16	I/O	i.MX25x GPIO3_16	
110	VBAT	Power In	VAR-SOM-MX25 supply voltage. Voltage range: 2.6–5.5V	
111	MMC1_WP	O	MMC1 Write Protect	GPIO2[20]
112	VBAT	Power In	VAR-SOM-MX25 supply voltage. Voltage range: 2.6–5.5V	
113	GND	Power	Digital GND	
114	VBAT	Power In	VAR-SOM-MX25 supply voltage. Voltage range: 2.6–5.5V	
115	GND	Power		
116	VBAT	Power In	VAR-SOM-MX25 supply voltage. Voltage range: 2.6–5.5V	
117	REG5_3V3	Power Out	3.3V Output. Up to 500mA	
118	USB_OTG_VBUS	I	USB 2.0 On-The-Go VBUS	
119	GPIO3_15	I/O	i.MX25x GPIO3[15]	
120	USB_OTG_DP	I/O	USB 2.0 On-The-Go Data Positive	
121	NC			
122	USB_OTG_DN	I/O	USB 2.0 On-The-Go Data Negative	
123	REGENB	O	Regulator Enable-Always ‘1’	
124	USB_OTG_ID	I	USB 2.0 On-The-Go Data Host/Client ID	
125	NC			
126	RTC_VBAT			
127	RESET_IN_N	I	Hardware Reset , Active Low	
128	NC			
129	NC			

130	NC			
131	NC			
132	NC			
133	NC			
134	NC			
135	NC			
136	NC			
137	NC			
138	NC			
139	NC			
140	NC			
141	NC			
142	NC			
143	NC			
144	NC			
145	NC			
146	NC			
147	NC			
148	NC			
149	NC			
150	NC			
151	GND	Power	Digital GND	
152	NC			
153	NC			
154	NC			
155	NC			
156	GND	Power	Digital GND	
157	NC			
158	REG5_3V3	Power Out	3.3V Output. Up to 500mA	
159	GND	Power	Digital GND	
160	REG5_3V3	Power		

		Out		
161	LINK_LED	O	'1' Link On	N/A
162	GND	Power	Digital GND	
163	SPEED_LED	O	'1' – 100Mbps '0' – 10Mbps	N/A
164	NC			
165	ETH_TxN	Analog Output	Ethernet Tx Negative	N/A
166	NC			
167	ETH_TxP	Analog Output	Ethernet Tx Positive	N/A
168	NC			
169	V3P3A	Ethernet Power Out	3.3V Output to Ethernet Magnetics	N/A
170	NC			
171	ETH_RxN	Analog Input	Ethernet Rx Negative	N/A
172	NC			
173	ETH_RxP	Analog Input	Ethernet Rx Positive	
174	GPIO4[7]	I/O		GPIO4[7]
175	GND	Power	Digital GND	
176	GPIO4[8]	I/O		GPIO4[8]
177	NC			
178	GPIO4[9]	O		GPIO4[9]
179	NC			
180	GPIO4[10]	O		GPIO4[10]
181	NC			
182	GPIO4[11]	O		GPIO4[11]
183	NC			
184	NC			
185	NC			
186	CODEC_AUXADC1	Analog	I.MX25x INAUX0 –A2D	

		Input		
187	NC			
188	CODEC_AUXADC2	Analog Input	I.MX25x INAUX1 – A2D	
189	LCDC_LCONTRAST	O	I.MX25x PWM4_PWM0 PWM#0	N/A
190	HP_LOUT	O	Left Channel Line Output	N/A
191	NC			
192	HP_ROUT	O	Right Channel Line Output	N/A
193	NC			
194	MIC_IN_P	I	Microphone Input (AC coupled)	N/A
195	AUD_AVDD	Power Out	Analog VDD	
196	MIC_BIAS	I	Microphone Bias	N/A
197	AUDIO_LIN_R	I	Right Channel Line Input (AC coupled)	N/A
198	AUD_GND	Power	Audio GND	N/A
199	AUDIO_LIN_L	I	Left Channel Line Input (AC coupled)	N/A
200	AUD _GND	Power	Audio GND	N/A

4 Interfaces

4.1 Display interface

4.1.1 LCD and DVI Subsystem Interface

Below are the main i.MX25x LCDC interface features. Please refer to the latest i.MX25x Multimedia Applications Processor Reference Manual.

i.MX25x LCDC interface main features:

- Maximum screen resolution of 800 X 600
- Support for single-screen (non-split) monochrome or color LCD panels, and for self-refresh type LCD panels
- Palette table for remapping data from memory for 4 and 8 bpp color support.
- Hardware panning (soft horizontal scrolling)
- 8-bit pulse width modulator for software contrast control
- Graphic window support for viewfinder functions in the color display
- 256 transparency levels for alpha blending between graphic windows and background planes

VAR-SOM-MX25 LCD interface signals:

Table 4-1 - LCD interface signals

Signal	Pin #	Type	Description
LCDC_LCLK	28	O	LCD Pixel clock
LCDC_HSYNC	26	O	LCD Horizontal Sync
LCDC_VSYNC	46	O	LCD Vertical Sync
LCDC_ACBIAS	64	O	LCD AC Bias/Data enable
LCDC_LD0	4	O	LCD Data line
LCDC_LD1	3	O	LCD Data line
LCDC_LD2	6	O	LCD Data line
LCDC_LD3	5	O	LCD Data line
LCDC_LD4	8	O	LCD Data line
LCDC_LD5	7	O	LCD Data line
LCDC_LD6	12	O	LCD Data line
LCDC_LD7	11	O	LCD Data line
LCDC_LD8	14	O	LCD Data line

LCDC_LD9	13	O	LCD Data line
LCDC_LD10	16	O	LCD Data line
LCDC_LD11	15	O	LCD Data line
LCDC_LD12	20	O	LCD Data line
LCDC_LD13	19	O	LCD Data line
LCDC_LD14	22	O	LCD Data line
LCDC_LD15	21	O	LCD Data line
LCDC_LD16	24	O	LCD Data line
LCDC_LD17	23	O	LCD Data line

4.1.2 LCD Data ,18bpp Interface Configuration Example

Table 4-2 - LCD 18 bit configuration Example

LCDC BUS PIN	18 Bit Configuration Function
LCDC_LD0	B0
LCDC_LD1	B1
LCDC_LD2	B2
LCDC_LD3	B3
LCDC_LD4	B4
LCDC_LD5	B5
LCDC_LD6	G0
LCDC_LD7	G1
LCDC_LD8	G2
LCDC_LD9	G3
LCDC_LD10	G4
LCDC_LD11	G5
LCDC_LD12	R0
LCDC_LD13	R1
LCDC_LD14	R2
LCDC_LD15	R3
LCDC_LD16	R4
LCDC_LD17	R5

4.2 Audio

4.2.1 Analog

Analog Audio signals are routed directly from the Wolfson WM8731 IC. The interface supports:

- Direct headphones driver
- Microphone input (with MIC bias).
- Audio Line in

Please refer to the device data sheet available on Wolfson-micro website .

http://www.wolfsonmicro.com/uploads/documents/en/WM8731_Rev4.3.pdf

VAR-SOM-MX25 Audio interface signals:

Table 4-2 - Audio interface signals

Signal	Pin #	Type	Description
HP_LOUT	190	O	Left Channel Headphone Output
HP_ROUT	192	O	Right Channel Headphone Output
MIC_IN_P	194	I	Line IN
MIC_BIAS	196	I	Mic Bias Voltage
MIC_N	197	I	Negative Audio Line In
MIC_P	199	I	Positive Audio Line In
AUD_AVDD	195	Power Out	3.3V Audio power supply
AUD_GND	198, 200	Power	Audio Ground

4.2.2 Synchronous Serial Interface

i.MX25x SSI features:

• Independent (asynchronous) or shared (synchronous) transmit and receive sections.

• Normal mode operation, using frame sync

- Network mode operation, allowing multiple devices to share the port with up to 32 time slots
- Gated Clock mode operation, without requiring a frame sync
- 2 sets of Transmit and Receive FIFOs.
- Programmable data interface modes such as I2S, LSB, MSB aligned together
- Programmable I2S modes (Master, Slave or Normal).
- AC97 support

VAR-SOM-MX25 synchronous Serial Interface signals:

Table 4-3 - Serial Interface signals

Signal	Pin #	Type	Description
SSI5_SCK	98	O	Synchronous Serial Interface 5 Clock
SSI5_STxFS	100	O	Synchronous Serial Interface 5 TxF
SSI5_SRxD	102	I	Synchronous Serial Interface 5 Tx Data
SSI5_STxD	104	O	Synchronous Serial Interface 5 Tx Data

4.3 ADC

The VAR-SOM-MX25 supports two 12-bit, 125-KHZ ADC inputs. Please refer to the latest i.MX25x Multimedia Applications Processor Reference Manual for detailed interface specifications.

ADC input pins:

Table 4-4 - ADC input pins

Signal	Pin #	Type	Description
CODEC_AUXADC1	186	I	i.MX25x Auxiliary ADC IN 1
CODEC_AUXADC2	188	I	i.MX25x Auxiliary ADC IN 2

4.4 Camera Interface

The VAR-SOM-MX25 uses the i.MX25x internal Camera CMOS Sensor Interface (CSI). Please refer to the latest i.MX25x Multimedia Applications Processor Reference Manual for detailed interface specifications.

The CSI Main Features:

- Configurable interface logic to support most commonly available CMOS sensors.
- Support for the CCIR656 video interface, in addition to the traditional sensor interface.
- 8-bit data port for YCC, YUV, or RGB data input.
- 8-bit/10-bit/16-bit data port for Bayer data input.
- Full control of 8-bit/pixel, 10-bit/pixel or 16-bit/pixel data format to 32-bit receive FIFO packing.

Table 4-5 - CMOS Sensor Interface signals

Signal	Pin #	Type	Description
CSI_PCLK(1)	59	I	Parallel interface pixel clock
CSI _HS(1)	78	I/O	Line trigger input/output signal
CSI _VS(1)	76	I/O	Frame trigger input/output signal
CSI_D0(2)	86	I	CSI Data[0]
CSI _D1(2)	88	I	CSI Data[1]
CSI _D2	56	I	CSI Data[2]
CSI _D3	55	I	CSI Data[3]
CSI _D4	50	I	CSI Data[4]
CSI _D5	18	I	CSI Data[5]
CSI _D6(1)	44	I	CSI Data[6]
CSI_D7(1)	53	I	CSI Data[7]
CSI _D8	74	I	CSI Data[8]
CSI _D9	72	I	CSI Data[9]

Notes:

(1) Muxed with MMC2 Bus

(2) Muxed with URAT3 control pins.

(3) MMC2 & CSI Can't be used if WLAN assembly option is selected

4.5 Ethernet

The VAR-SOM-MX25 provides one full-featured 10/100 Mbit Ethernet port, using the SMSC LAN8700IC Ethernet PHY & Embedded i.MX25x Ethernet MAC controller.

Please refer to the latest i.MX25x Multimedia Applications Processor Reference Manual & SMSC LAN8700/LAN8700i data sheet for more detailed interface specifications.

Table 4-6 - Ethernet Signals

Signal	Pin #	Type	Description
ETH_TxN	165	O	Transmit Negative
ETH_TxP	167	O	Transmit Positive
ETH_RxN	171	I	Receive Negative
ETH_RxP	173	I	Receive Positive
LINK_LED	161	O	Activity Indicator
LINK_SPEED	163	O	Speed Indicator
VCC33A	169	O	3.3 V Output to Ethernet Magnetics

4.6 UARTs

The VAR-SOM-MX25 has 3 UART ports. The default debug serial port is UART 3.

Each UART includes a programmable baud-rate generator for up to 4.15 Mbit/s (115.2K in IrDA Mode)

Receive and transmit FIFO fill and drain operations can be done using programmed I/O or DMA transfers. To minimize CPU overhead for UART communications, device driver software can configure interrupts and DMA for data transfers to or from memory.

Table 4-7 - UART1 Signals

Signal	Pin #	Type	Description
UART1_Tx	35	O	UART Transmit
UART1_Rx	33	I	UART Receive
UART1_RTS	31	O	UART HW Flow Control RTS
UART1_CTS	29	I	UART HW Flow Control CTS

Table 4-8 - UART 2 Signals

Signal	Pin #	Type	Description
UART2_Tx	69	O	UART Transmit
UART2_Rx	71	I	UART Receive
UART2_RTS	67	O	UART HW Flow Control RTS
UART2_CTS	65	I	UART HW Flow Control CTS

Table 4-9 - UART3 Signals

Signal	Pin #	Type	Description
UART3_Tx	84	O	UART Transmit
UART3_Rx	90	I	UART Receive
UART3_RTS	86	O	UART HW Flow Control RTS
UART3_CTS	88	I	UART HW Flow Control CTS

4.7 CAN BUS (FlexCAN)

The VAR-SOM-MX25 supports 2.0B CAN interface based on the i.MX25xx FlexCAN controller.

The FlexCAN module supports the following main features:

- Full implementation of the CAN protocol specification, version 2.0B
- Flexible message buffers of 0-8 bytes data length
- Each message buffer is configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx mask registers for each message buffer
- Includes 1056 bytes of RAM for message buffer storage (64 message buffers)
- Includes 256 bytes of RAM for individual Rx mask registers (64 mask registers, one for each message buffer)
- Low-power modes, with programmable wake-up on bus activity

Table 4-10 - CAN Signals

Signal	Pin #	Type	Description
CAN_Rx	1	I	UART Receive
CAN_Tx	2	O	UART Transmit

4.8 USB 2.0

4.8.1 USB 2.0 Host

The VAR-SOM-MX25 uses the internal i.MX25x Full Speed HOST PHY.

Please refer to the latest i.MX25x Multimedia Applications Processor Reference Manual for more detailed interface specifications.

Table 4-11 - USB 2.0 Host signals

Signal	Pin #	Type	Description
USBHOST_DP	103	I/O	USB Host Data Positive
USBHOST_DN	105	I/O	USB Host Data Negative

4.8.2 USB 2.0 On-The-Go

The VAR-SOM-MX25 uses the internal i.MX25x High Speed OTG PHY.
Please refer to the latest i.MX25x Multimedia Applications Processor Reference Manual for more detailed interface specifications.

Table 4-12 - USB 2.0 OTG signals

Signal	Pin #	Type	Description
USB_OTG_DN	122	I/O	USB OTG Data Negative
USB_OTG_DP	120	I/O	USB OTG Data Positive
USB_OTG_VBUS	118	O	USB OTG VBUS 5V Enable
USB_OTG_ID	124	I	USB 2.0 On-The-Go Data Host/Client ID

4.9 SPI

The VAR-SOM-MX25 provides one Serial Peripheral Interface (CSPI).

Key features of the CSPI module include:

- Full-duplex synchronous serial interface, Master/Slave configurable
- Two Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited data transfers
- 32-bit wide by 8-entry FIFO for data, both transmitted and received
- The Chip Select (SS) and SPI Clock (SCLK) polarity and phase functions are configurable
- Direct Memory Access (DMA) support

Table 4-13 - CSPI1 signals

Signal	Pin #	Type	Description
CSPI1_RDY	10	O	CSPI READY Signal (Optional)
CSPI1_CLK	37	I/O	i.MX25x CSPI1 Clock
CSPI1_SIMO	39	I/O	i.MX25x CSPI1 Signal
CSPI1_SOMI	41	I/O	i.MX25x CSPI1 Signal
CSPI1_CS0	68	I/O	i.MX25x CSPI1 Signal
CSPI1_CS1	62	O	i.MX25x CSPI1 Chip Select 1 Signal

4.10 I2C

The VAR-SOM-MX25 I2C provides the functionality of a standard I2C slave and master.

On Module RTC, Power management and Audio IC use the following I2C address

- 0x1A - AUDIO CODEC
- 0xD0 - RTC
- 0x54 - MC37704 (Power)

Those addresses can't be used by user base board VAR-SOM-MX25 I2C1 signals:

Table 4-14 - I2C Signals

Signal	Pin #	Type	Description
I2C2_SCL	63	I/O	I2C2 I^2C Clock
I2C2_SDA	61	I/O	I2C2 I^2C Data

4.11 SD / MMC (eSDHC)

The VAR-SOM-MX25 has two SD/MMC interfaces, based on the i.MX25x enhanced Secured Digital Host Controller (eSDHC). It provides the interface between the VAR-SOM-MX25 and MMC/SD/SDIO/CE-ATA cards.

The MMC2 interface is muxed with the CSI (CMOS Sensor Interface).

The eSDHC main features are:

- Designed to work with MMC, MMC plus, MMC RS, SD memory, miniSD memory, SDIO, miniSDIO, SD Combo, and CE-ATA cards.
- Supports 1-bit , 4-bit , or 8-bit MMC modes, 1-bit or 4-bit SD and SDIO modes, and 1-bit, 4-bit, or 8-bit CE-ATA devices

  -Variable card bus clock frequencies, up to 52 MHz

  -Up to 416 Mbps of data transfer for MMC cards in 8-bit mode

  -Up to 200 Mbps of data transfer for SD/SDIO cards in 4-bit mode

  -Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes, and also supports interrupt period

- Supports single-block and multi-block read and write

  -Block sizes of 1–4096 bytes

  -Supports pauses during the data transfer at block gap

  -Supports Auto CMD12, for multi-block transfer

- Supports internal and external DMA capabilities

Table 4-15 - MMC1 signals

Signal	Pin #	Type	Description
MMC1_DAT0	36	I/O	MMC1 Data
MMC1_DAT1	38	I/O	MMC1 Data
MMC1_DAT2	40	I/O	MMC1 Data
MMC1_DAT3	42	I/O	MMC1 Data
MMC1_CLKO	32	O	MMC Clock

MMC1_CMD	43	O	MMC command
MMC1_CD	91	I	MMC Card Detect
MMC1_WP	111	O	MMC Write protect

Table 4-16 - MMC2 signals

Signal	Pin #	Type	Description
MMC2_DAT0	25	I/O	MMC2 Data
MMC2_DAT1	76	I/O	MMC2 Data
MMC2_DAT2	78	I/O	MMC2 Data
MMC2_DAT3	59	I/O	MMC2 Data
MMC2_CLK	53	O	MMC2 Clock
MMC2_CMD	44	O	MMC2 command

4.12 PWM

The VAR-SOM-MX25 exposes the i.MX25x PWM4_PWM0 & PWM1_0 signals. Both can be used as configurable PWM lines.

Table 4-17 - PWM Signals

Signal	Pin #	Type	Description
LCD_CONTRAST	189	O	pulse width modulation
PWM1	87	O	pulse width modulation

4.13 Touch Screen

The VAR-SOM-MX25 touch interface is based on the i.MX25x integrated TSC.

The controller's main features are:

- Compatible with 4 & 5 wire resistant Touch Screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement averaging to filter noise
- Maximum X & Y sample rate (without averaging): 12 kHz

Figure 4-1

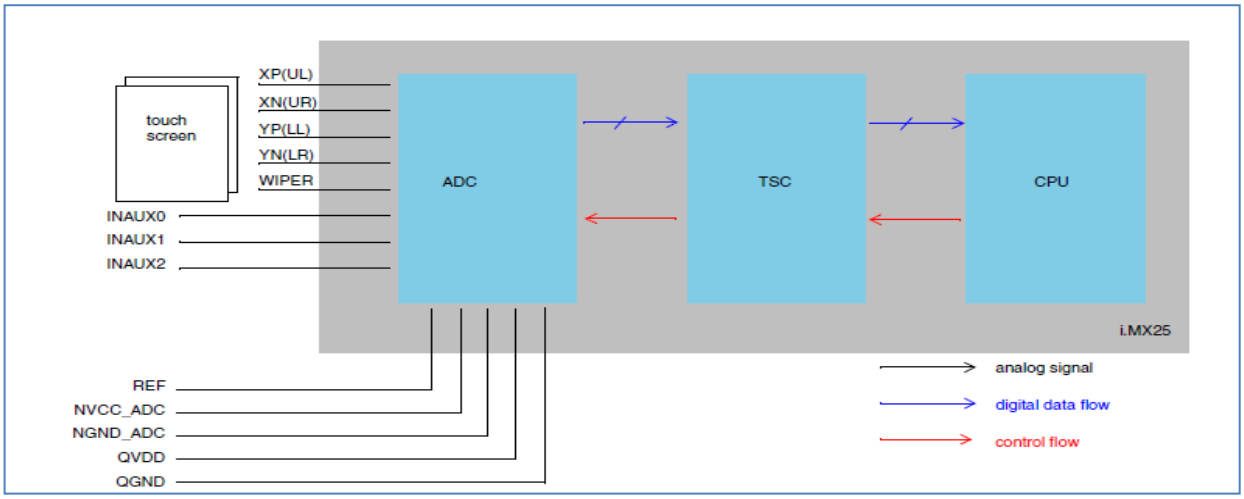


Table 4-18 - Touch Screen Signals

Signal	Pin #	Type	Description
TSPX	73	Analog	TSC interface X Plus
TSMY	75	Analog	TSC interface Y Minus
TSMX	77	Analog	TSC interface X Minus
TSPY	79	Analog	TSC interface Y Plus
Wiper	49	Analog	TSC Wiper (5 pin Mode)

4.14 Boot Option

The VAR-SOM-MX25 provdies a dedicated signal, which configures the boot sequence of the i.MX25x processor. This signal defines the order of the boot devices. Consequently, it permits the NAND flash burning PC utility to burn the boot-loader.

Table 4-19 - Boot Options

Signal	Pin #	Type	Description
SYS_BOOT5	92	I	System Boot Option 5 [‘1’ – burn flash]

4.15 General Purpose IOs

Most of the SoM I/O pins can be used as GPIOs. Each GPIO can be configured as an input/output or interrupt source.

Please refer to Chapter 3 for a complete SOM connector signal list and for GPIO multiplexing.

4.16 General System signals

The reset signals are connected to the MC34704 PMIC.

RESET_IN_N is connected to the MC34704 RST# input pin and is used for modules's cold-hardware-reset.

RESET OUT is the MC34704 POR output and is used to reset external peripherals.

Table 4 -20 - Resets Signals

Signal	Pin #	Type	Description
RESET_IN_N	127	I	Hardware Reset (internal 4.7K Ohm Pull up)
RESET_OUT	97	**O**	POR

4.17 RTC

The VAR-SOM-MX25 has an on-board RTC clock. The RTC keeps on running as long as the RTC_BACKUP is above 2.5v.

4.18 Power supply pins

Table 4-20 - Power Supply Pins

Signal	Pin #	Description
VBAT	110,112,114,116	VAR-SOM-MX25 single DC-IN supply voltage. Voltage range: 2.6–5.5V
3V3	158,160,117	3.3V Output, Up to 500mA
V3P3A	169	3.3 V Output to Ethernet Magnetics
AUD_AVDD	195	Audio 3.3V Power supply
REGEN	123	External Regulators Enable
RTC_BACKUP	126	Coin battery input for RTC backup

Table 4-21 - GND Pins

Signal	Pin #	Description
GND	34,47,48,51,58,60,81,83,106,113,115,151,156,159,162,175	Digital Ground
AUDIO GND	198,200	AUDIO Ground

5 Absolute maximum Characteristics

Table 5-1 - Absolute maximum Characteristics

Power supplies	Min	Max	Units
Main Power supply, DC-IN	-0.3	6	V
3.3V output supply, in total		500	mA

6 Operational Characteristics

Table 6-1 - Operational Characteristics

Power supplies	Min	Max	Units
Main Power supply, DC-IN	2.6	5.5	V
RTC Backup battery voltage	2.5	3.2	V
Digital I/O Levels	3.3		V

7 Power Consumption

Table 7-1 - Power Consumption

Power supplies	Min	Max	Units
Main Power supply, DC-IN	0.8	1.5	W

- Depends on module's configuration

8 Environmental Specifications

Table 8-1 - Environmental Specifications

	Min	Max	Units
Commercial operating temperature range	0^0C	+70	^{0}C
Extended operating temperature range	-25	+85	^{0}C
MTBF	100000>		hrs
Shock resistance	50G / 20		ms
Relative humidity, Operational	10	90	%
Relative humidity, Storage	5%	95	%
Vibration	20G / 0 - 600		Hz

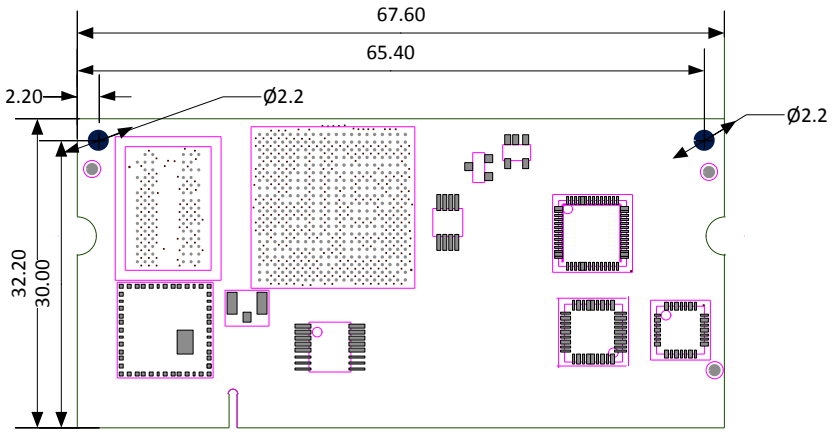
9 Mechanical Drawings

VAR-SOM-MX25 mechanics footprint is based on the standard SO-DIMM200 footprint (JEDEC MO-224, 1.8mm -2.5 DDQ key position). The recommended mating connector for base board interfacing is FCI 10033853-052FSLF.

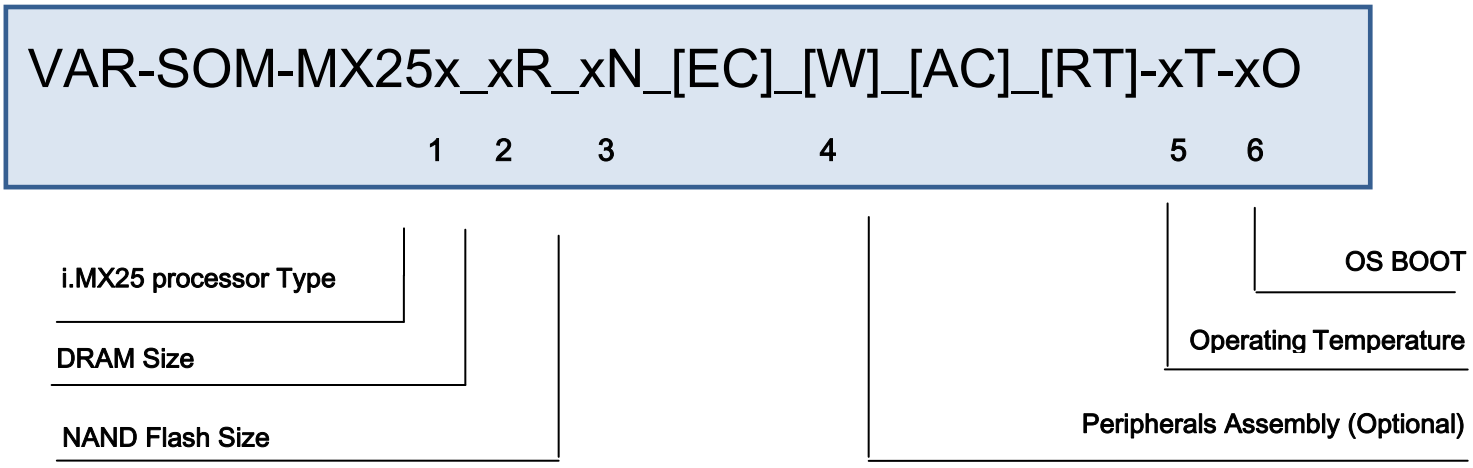
Components can be placed up to 1mm high under the VAR-SOM-MX25 module using the recommended connector.

Please request for a mechanical DXF file at support@variscite.com

TOP drawing:



10 Ordering Information



1. **i.MX25x processor Type**

   7: i.MX257

2. **DRAM Size**

   64:64MB
   128:128MB

3. **NAND Flash Size**

   1024: 512MB
   2048:2048MB

4. **Peripherals Assembly (Optional)**

   EC: 10/100BaseT Ethernet PHY
   W: 802.11 b/g WLAN
   AC: Audio Codec
   RT: RTC

5. **Operating Temperature**

   CT: 0-75°C
   ET: -25-85°C

6. **OS BOOT**

   C: CE EBoot
   L: Linux UBOOT

Example
VAR-SOM-I.MX257_64R_1024N_EC_W_AC_RT_CT_CO

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