VAR-DT8MCustomBoard

CONTENT

Revision History

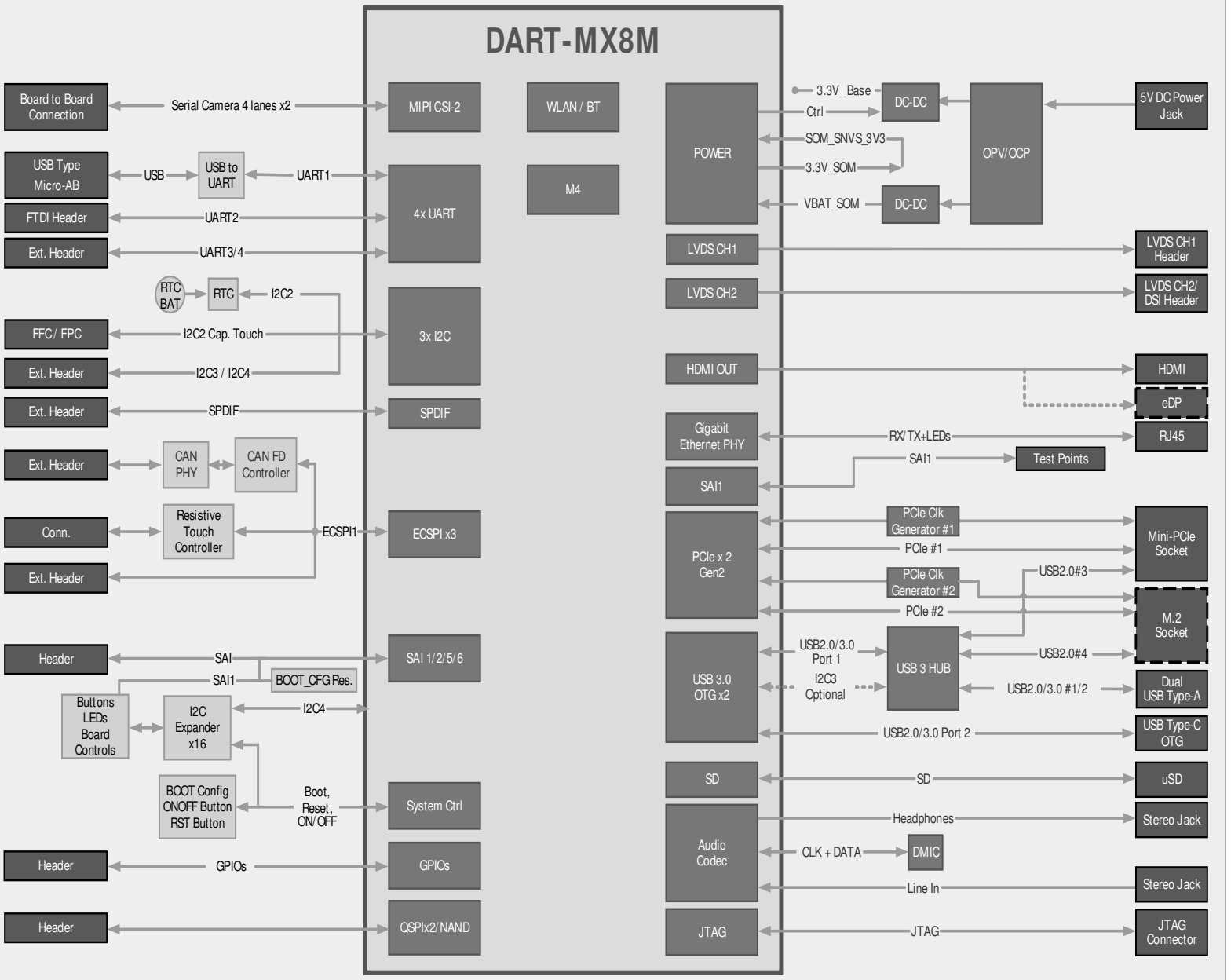
Document	Carrier	Description
1.0	2.0	Changes from DOC 1.9 Carrier 1.4D include: * Optimisation for DART-MX8MP: - Added external ethernet PHY - Control IOs used on previous version over SAI1 now controlled via I2C expander - Added DSI header option for DART-MX8MP stock item exposed pins; Pinout compatible to Symphony J7+J8 - Native USB ID usage added important note - USB Type C active discharge replaced with bleeder - USB Type C crossbar differential switch simplified. - Removed DT8M NAND option - Added QSPI header J41 - located in location of J25 - J27 & J28 pinout aligned to Symphony - Added PD on J1.38 for BSP CustomV2.0 signal. - Added additional CAN PHY on iMX8MP - U44 footprint modified from SOIC to DFN - SD card power switch modified - Main power switch type align to Symphony - DART-MX8M DP connector replaced with 40pin eDP REF. design - HDMI path simplified - PINMUX page deleted - reference to XLS - Aded reference design for 12Mb/s CAN-FD transciever - Added M.2. PCIe reference design - Add option on bottom to route PCIe port 1 to M.2 connector - Replace boot config drivers to 3state type - Replace MCP2518 crystal to 40MHz and connect RX_INT - Updated Block Diagrams - VCC_SOM Increased to 3.8V (R145 changed to 18K) - D9, C58 Removed. VCC_BASE_3V3 goes up just after NVCC_3V3
1.1	2.1	* GPLED4 controlled via FET Q14 to support DART-MX8M-PLUS 1.8V voltage level * Updated GPIO expanders U56,U57 footprint * Added note for U53 recommended P/N
1.2	3.0	* Due to EOL: - Changed BOM P/N: U23,U45,U46,U56,U59,U57 - Added optional resistors R291-R294 - Changed Assembly: U31 Not assembled, R167 assembled - Changed Ethernet PHY to ADIN1300: Changed Ethernet2 schematics, Added R295 * Changed J5 P/N and schematics to support ADIN1300 PHYs * Updated comments on schematic nets * R94-R97, R114-R117 assembled with Ferrite Bead
1.3	3.0A	* Due to EOL: U60,U62 changed to NFL18ZT207H1A3D * Due to Allocation Problems: U45,U59 changed to SN65HVD232QDR
1.4	3.0B	* DART-MX95 Block Diagram & Connectors added
1.5	3.0C	* DART-MX93 Block Diagram & Connectors added * DART-MX91 Block Diagram & Connectors added

Title: 01. Cover			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 1 of 17	

02A. Block Diagram – DART-MX8M

VAR-DT8MCustomBoard V2.x

Doc rev 1.0



I2C BUS ADDRESS:

I2C1: Internal to SOM

I2C2: PU – 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU – 5K on SOM
0x60 SOM – Int. power ctrl.
0x2D USB3 HUB
0xXX Header J12

I2C4: PU – 10K on U8
10K on custom
0x3C CSI P2 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

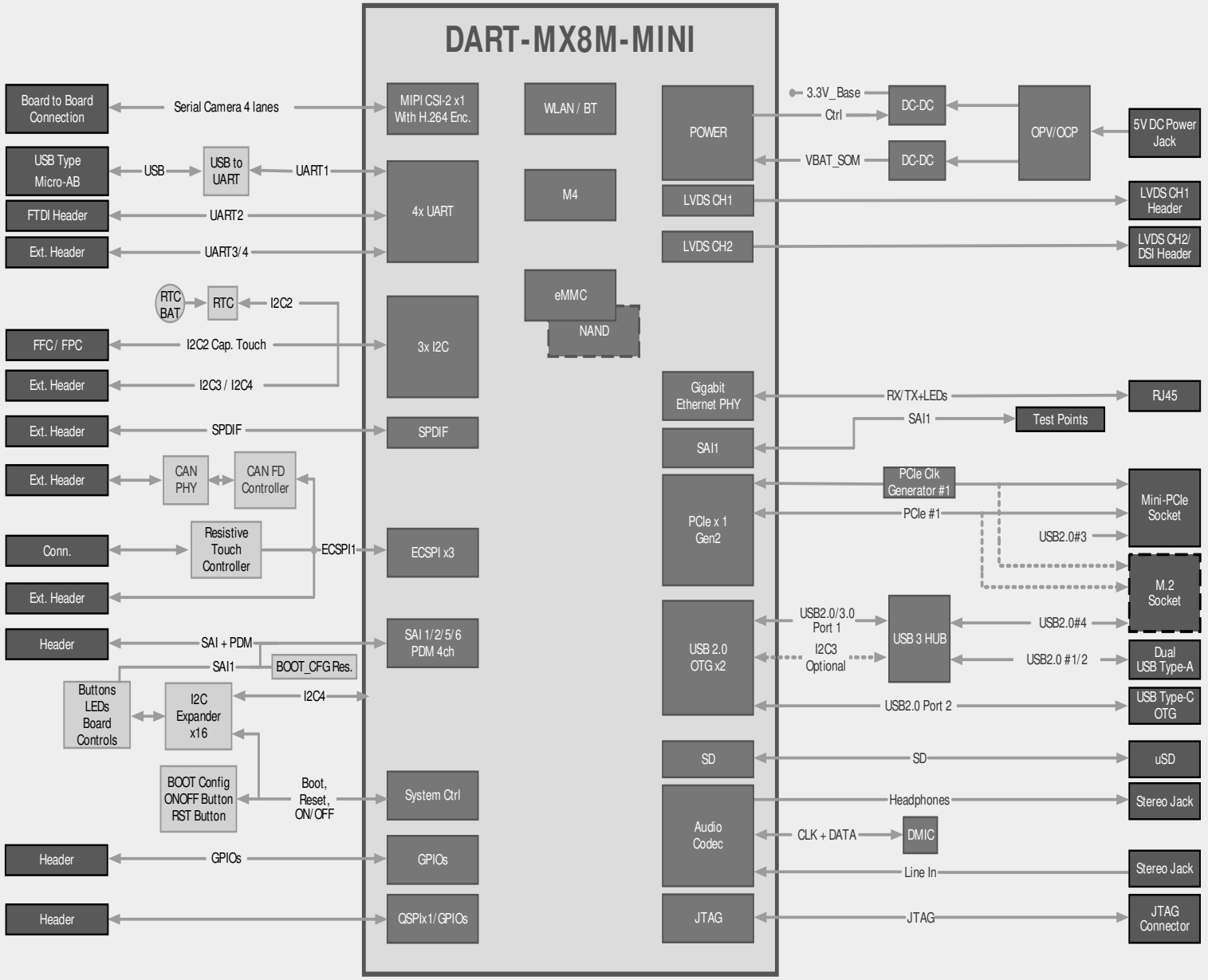
Variscite

Title: 02A. Block Diagram with DART-MX8M			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 2 of 17	

02B. Block Diagram – DART-MX8M-MINI

VAR-DT8MCustomBoard V2.x

Doc rev 1.0



I2C BUS ADDRESS:

```
I2C1:   Internal to SOM

I2C2:   PU - 10K on U8
            10K on custom
        0x54 BOARD ID EEPROM Page0
        0x55 BOARD ID EEPROM Page1
        0x68 RTC
        0x38 CAPACITIVE TOUCH CTRLR
        0x3D USB-C CC Logic PTN5150AHXMP
        0x3C CSI P1 Camera (1V8) OV5640


I2C3:   PU - 5K on SOM
        0x1A SOM - Int. CODEC
        0x2D USB3 HUB
        0xXX Header J12

I2C4:   PU - 10K on U8
            10K on custom
        0x3C CSI P1 Camera (1V8) OV5640
        0xXX Header J12
        0xXX mPCIe J23 & J32
```

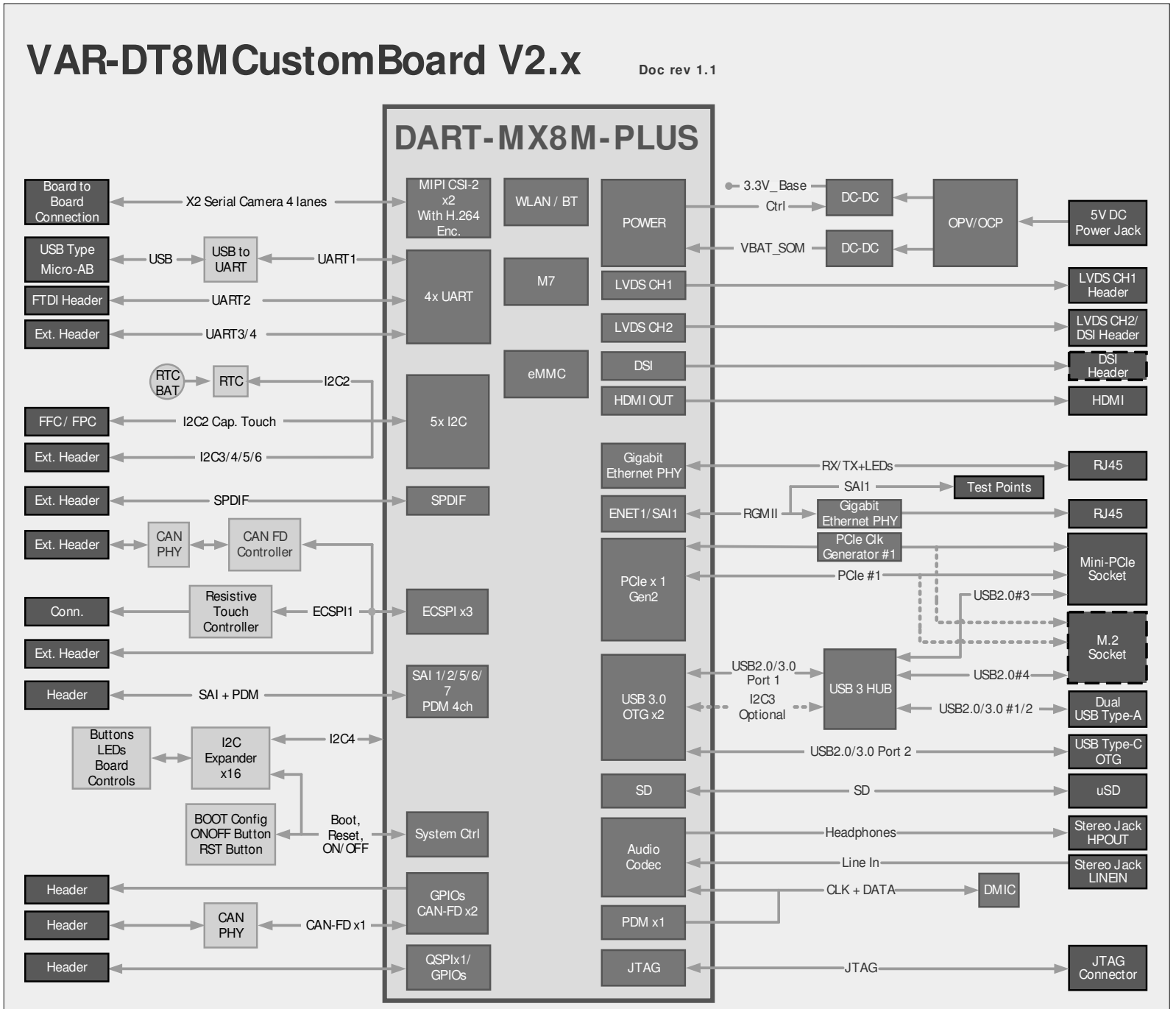
Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

Variscite

Title: 02B. Block Diagram with DART-MX8M-MINI			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 3 of 17	

02C. Block Diagram – DART-MX8M-PLUS



I2C BUS ADDRESS:

I2C1: Internal to SOM

I2C2: PU – 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU – 5K on SOM

0x2D USB3 HUB
0xXX Header J12

I2C4: PU – 10K on U8
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

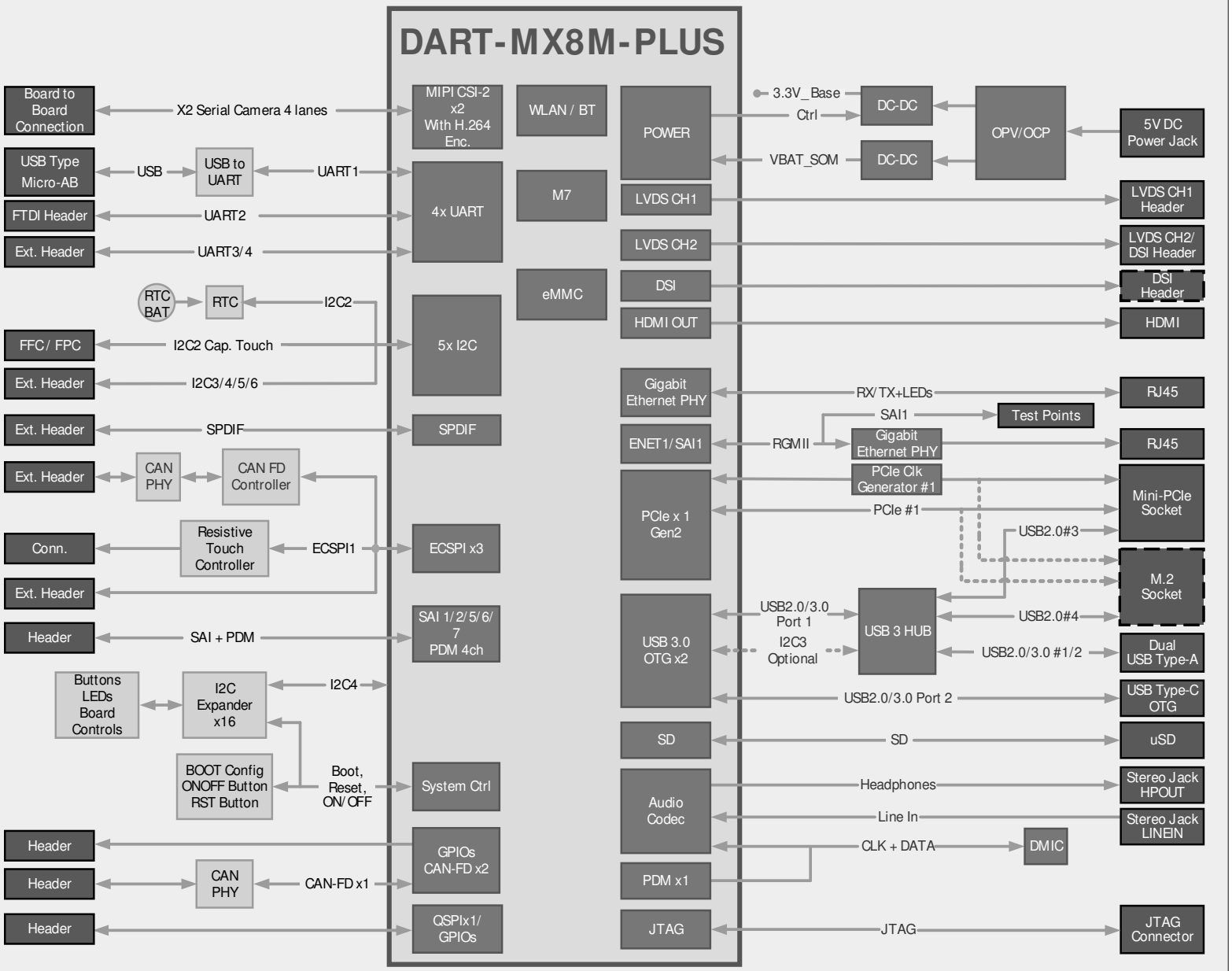
Variscite

Title: 02C. Block Diagram with DART-MX8M-PLUS			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 4 of 17	

02D. Block Diagram – DART-MX95

VAR-DT8MCustomBoard V2.x

Doc rev 1.1



I2C BUS ADDRESS:

I2C1: Internal to SOM

I2C2: PU – 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU – 5K on SOM
0x2D USB3 HUB
0xXX Header J12

I2C4: PU – 10K on U8
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

Variscite

Title: 02D. Block Diagram with DART-MX95			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
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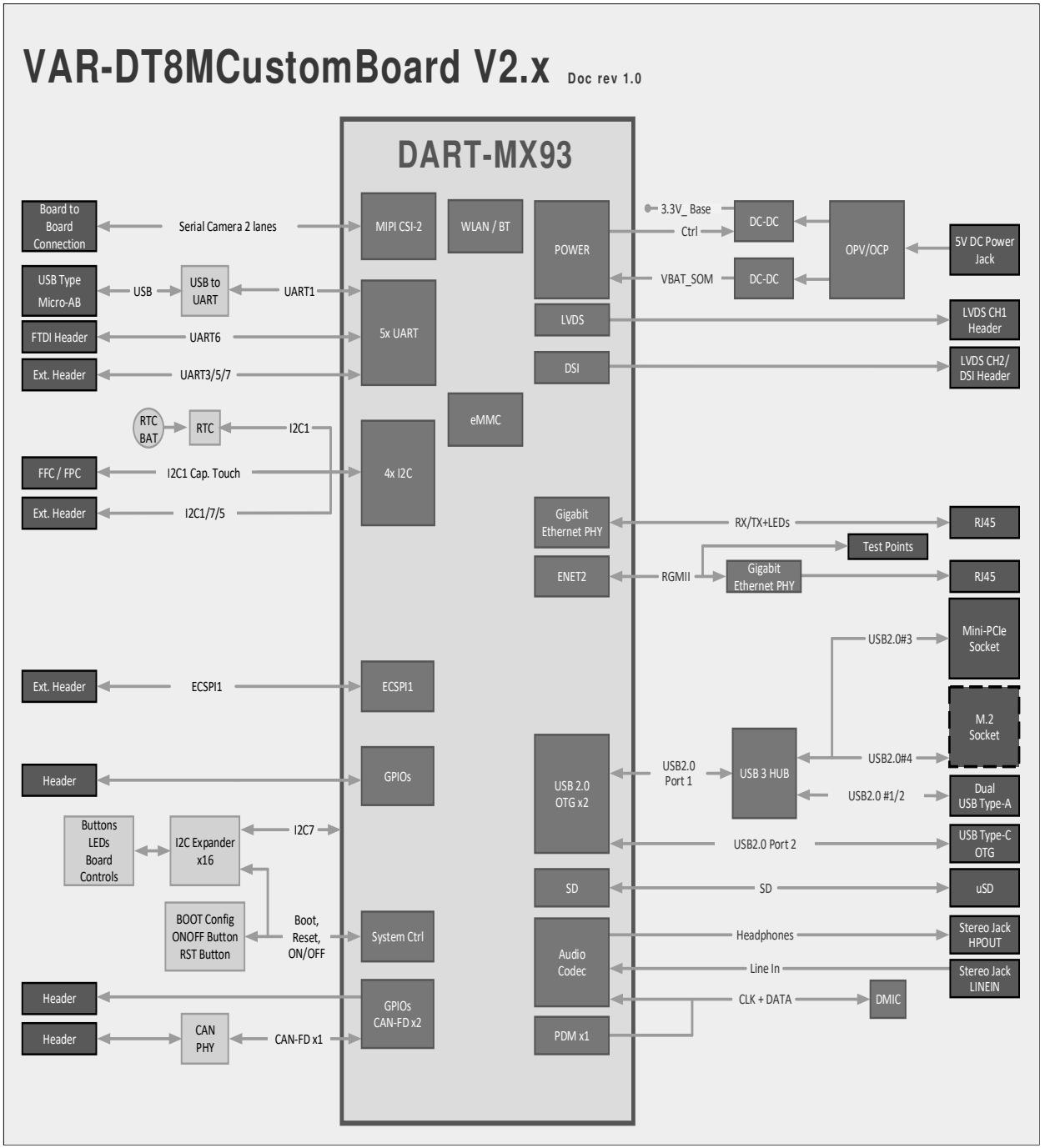
02E. Block Diagram – DART-MX93



I2C BUS ADDRESS:

I2C3: Internal to SOM

I2C1: PU – 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C5: 0x2D USB3 HUB
0xXX Header J12

I2C7: PU – 10K on U8
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

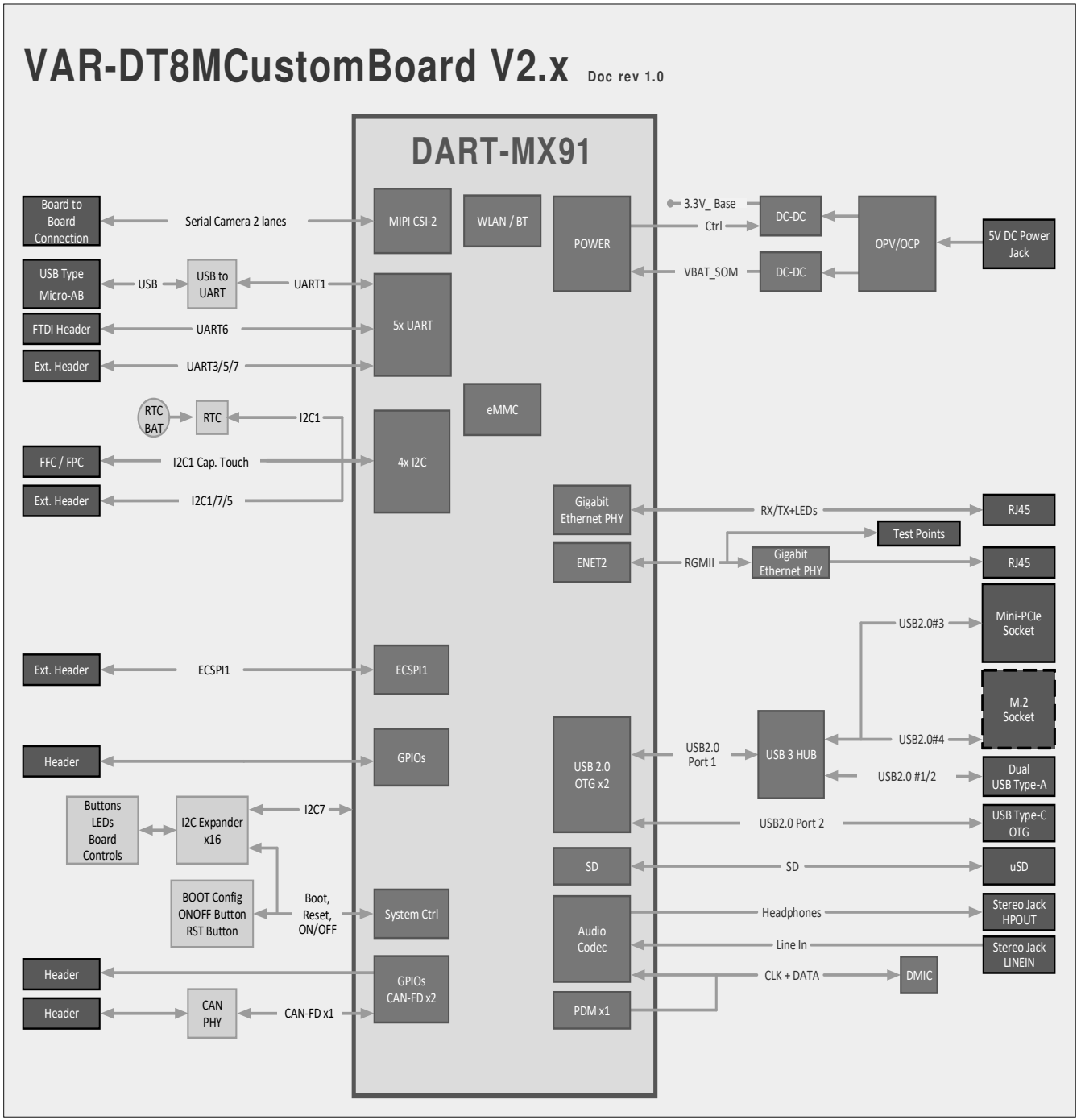
Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. LVDS routed as 100 ohm Diff pairs
3. Other fast changing signals routed as 50 ohm

Variscite

Title: 02E. Block Diagram with DART-MX93			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 4 of 17	

02F. Block Diagram – DART-MX91



I2C BUS ADDRESS:

I2C3: Internal to SOM

I2C1: PU – 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C5: 0x2D USB3 HUB
0xXX Header J12

I2C7: PU – 10K on U8
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. LVDS and DSI not exist. Headless mode only.
3. Other fast changing signals routed as 50 ohm

Variscite

Title: 02F. Block Diagram with DART-MX91			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
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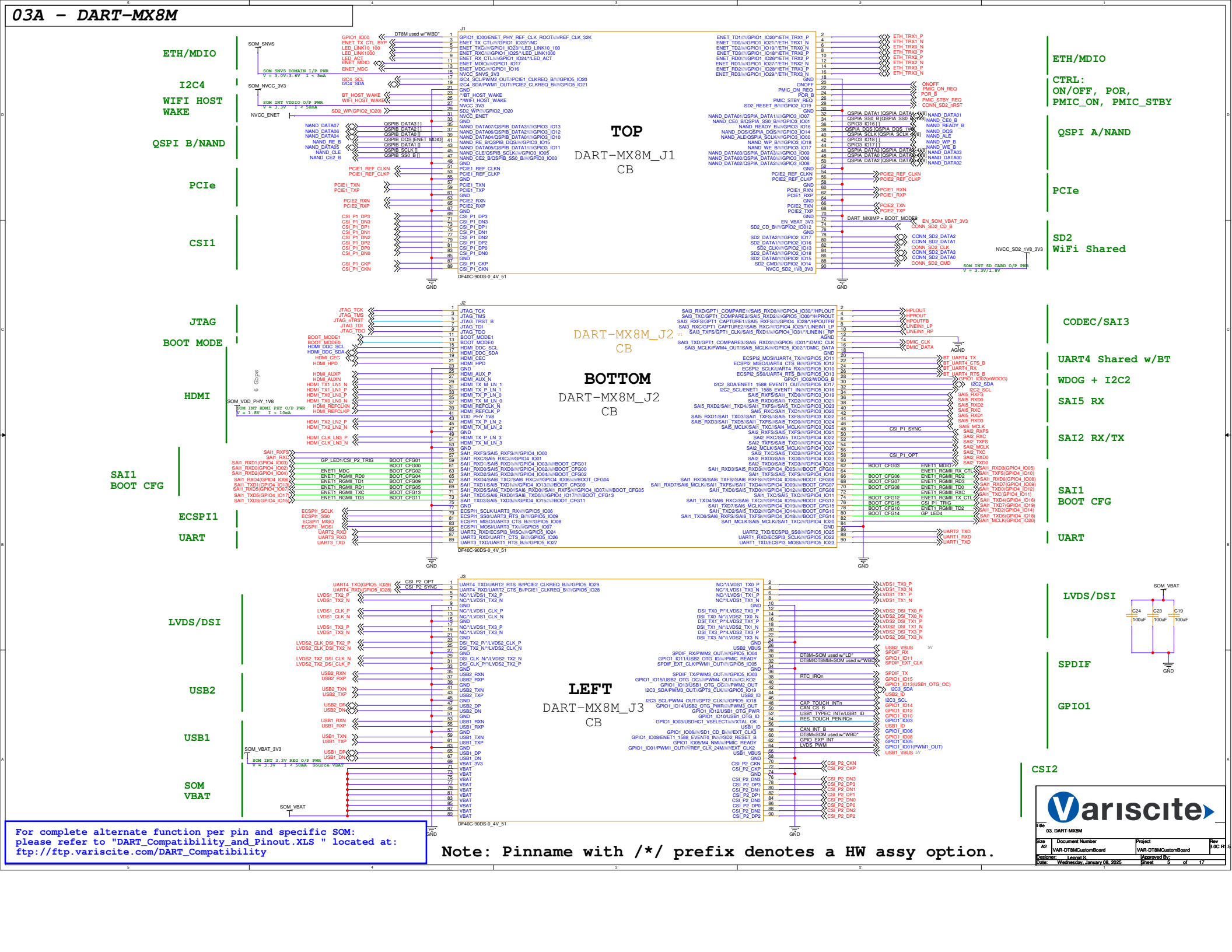
03A – DART-MX8M



For complete alternate function per pin and specific SOM:
please refer to "DART_Compatibility_and_Pinout.XLS " located at:
ftp://ftp.variscite.com/DART_Compatibility

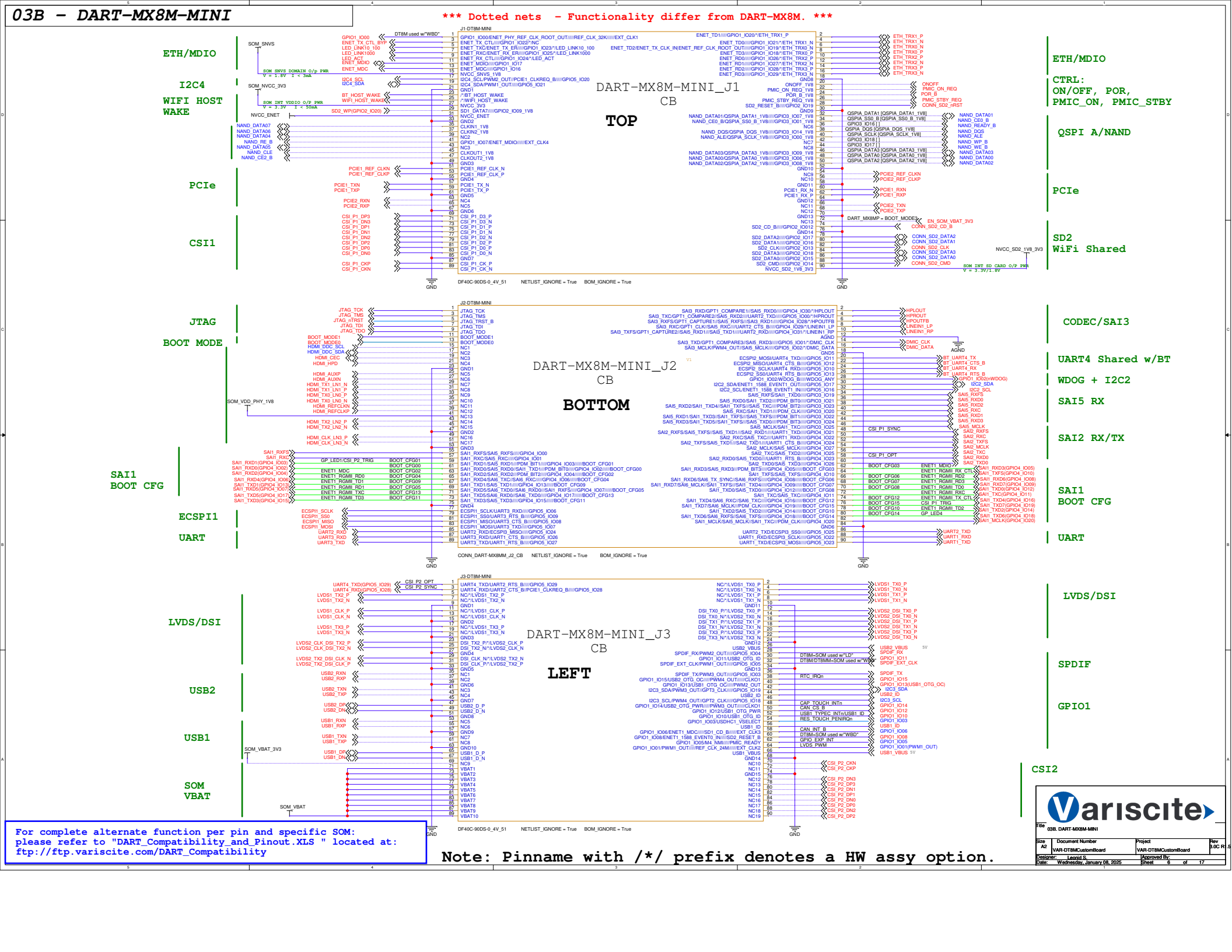
Note: Pinname with /*/ prefix denotes a HW assy option.

Variscite

Title	03. DART-MX8M		
Size: A2	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 5 of 17	

03B - DART-MX8M-MINI

*** Dotted nets - Functionality differ from DART-MX8M. ***

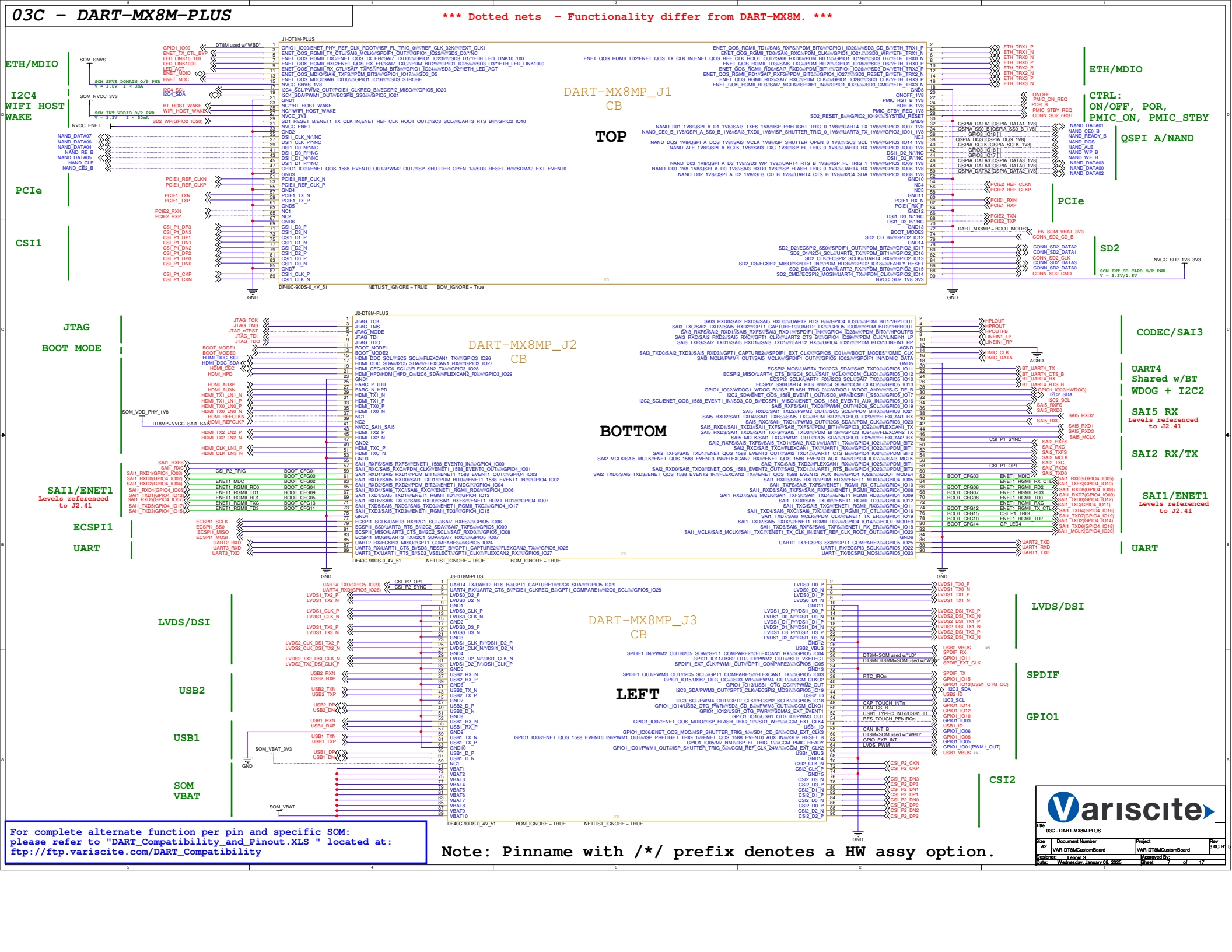


Variscite

Title	03B. DART-MX8M-MINI		
Size: A2	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 6 of 17	

03C - DART-MX8M-PLUS

*** Dotted nets - Functionality differ from DART-MX8M. ***



For complete alternate function per pin and specific SOM:
please refer to "DART_Compatibility_and_Pinout.XLS " located at:
ftp://ftp.variscite.com/DART_Compatibility

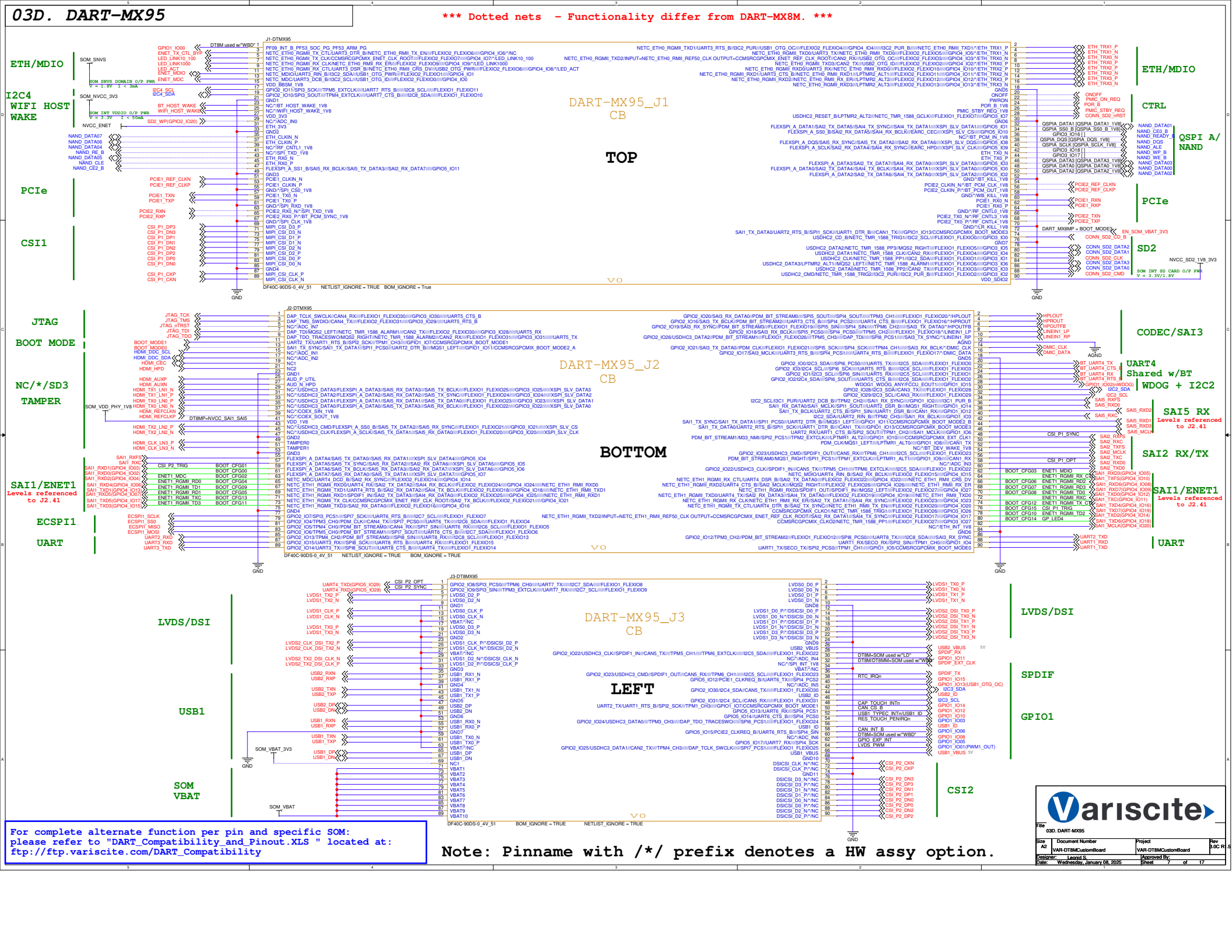
Note: Pinname with /*/ prefix denotes a HW assy option.

Variscite

Title	03C - DART-MX8M-PLUS		
Size: A2	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 7 of 17	

03D. DART-MX95

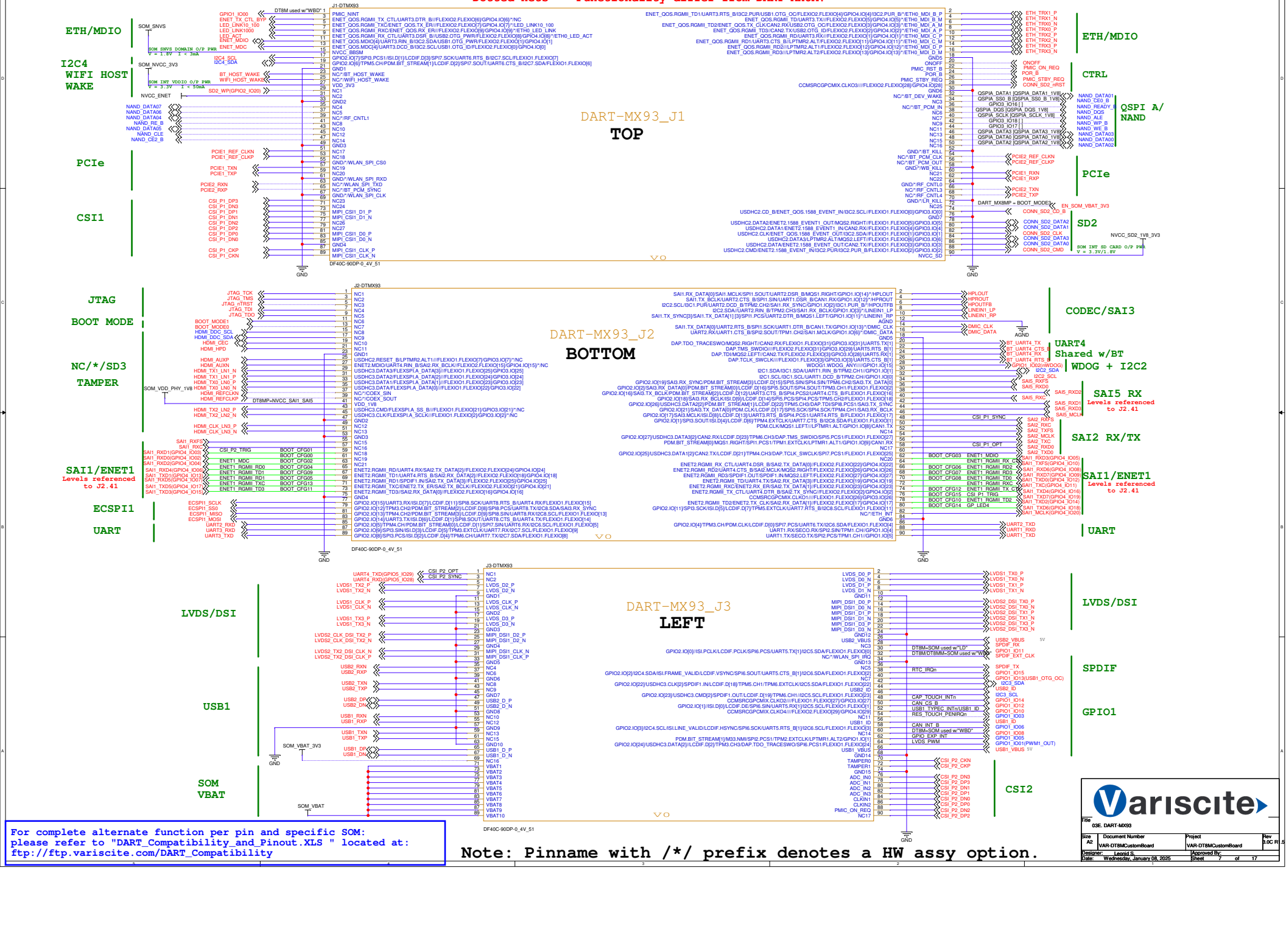
*** Dotted nets - Functionality differ from DART-MX8M. ***



Title	03D. DART-MX95		
Size: A2	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 7 of 17	

03E. DART-MX93

*** Dotted nets - Functionality differ from DART-MX8M. ***

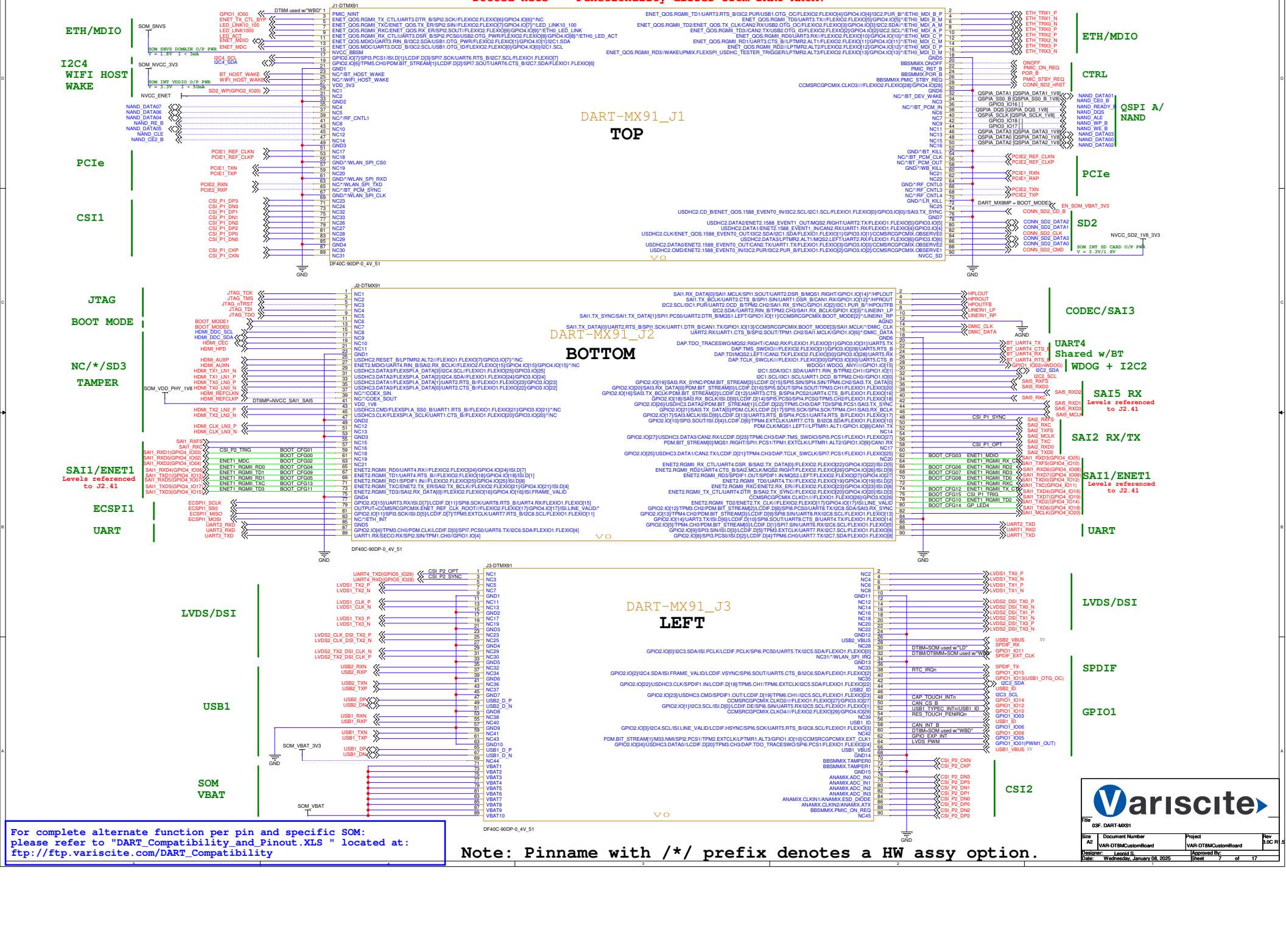


For complete alternate function per pin and specific SOM:
please refer to "DART_Compatibility_and_Pinout.XLS " located at:
ftp://ftp.variscite.com/DART_Compatibility

Note: Pinname with /*/ prefix denotes a HW assy option.

03F. DART-MX91

*** Dotted nets - Functionality differ from DART-MX8M. ***



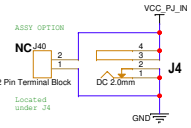
For complete alternate function per pin and specific SOM:
please refer to "DART_Compatibility_and_Pinout.XLS " located at:
ftp://ftp.variscite.com/DART_Compatibility

Variscite

Title	03F. DART-MX91		
Size: A2	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 7 of 17	

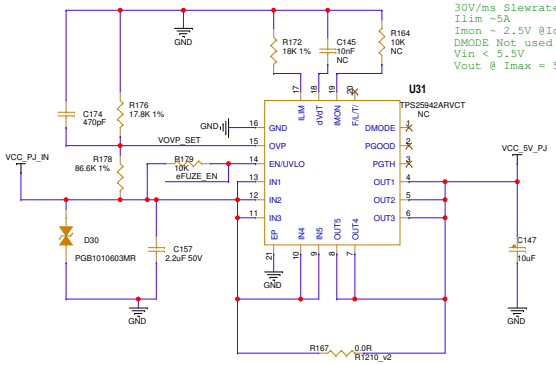
04. Power, RTC,Board ID

5VDC/4A POWER JACK

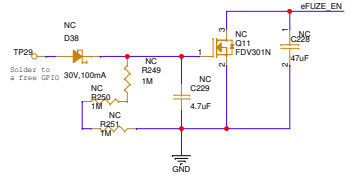


PWR JACK 5V IN OVP/OCP

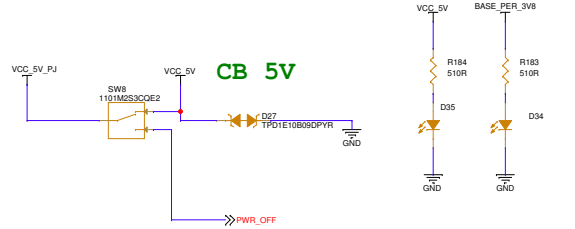
30V/ms Slewrate based on int. circuitry
Ilim ~5A
Imon ~ 2.5V @Iout=5A
DMODE Not used
Vin < 5.5V
Vout @ Imax = 5.2V



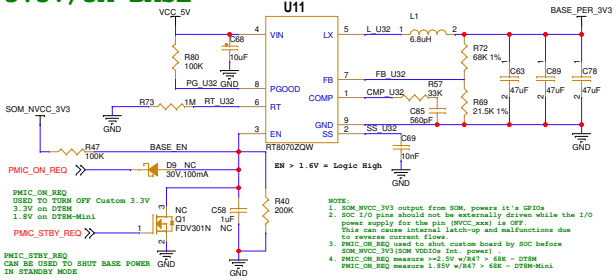
Variscite Internal use circuit.



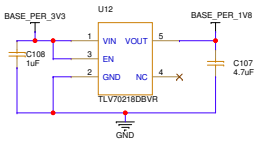
POWER SW/(ON/OFF)



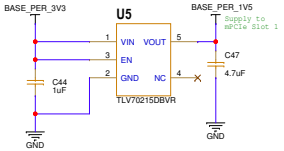
3.3V/3A BASE



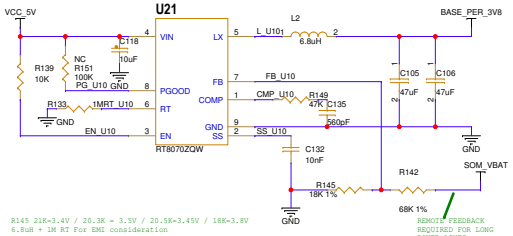
1.8V/0.3A BASE



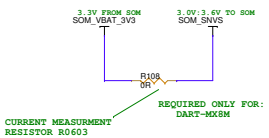
1.5V/0.3A #1 BASE



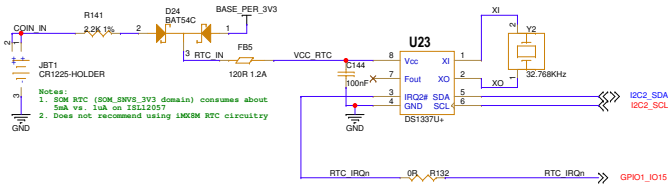
3.8V/3A FROM PWR JACK



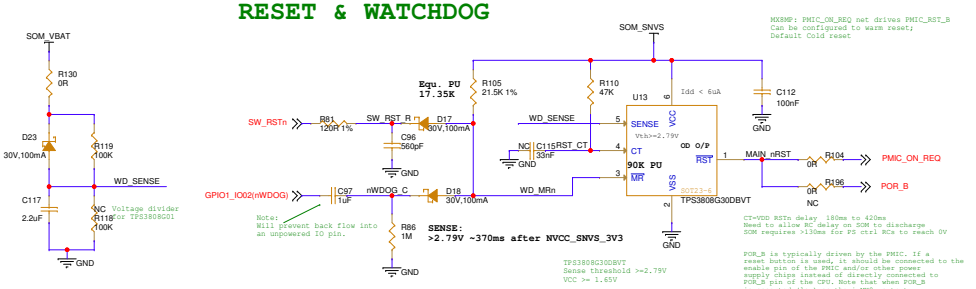
SOM SNVS



RTC BATTERY

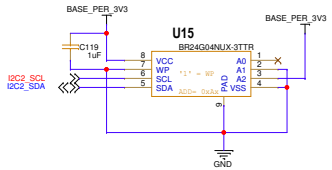


RESET & WATCHDOG

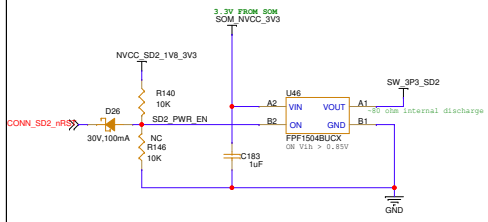


SOM PWR

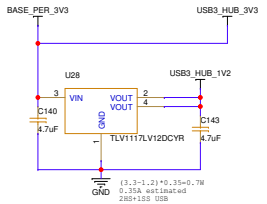
BOARD ID



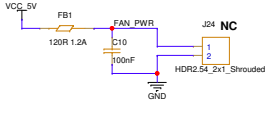
SD POWER



USB3 HUB POWER



FAN : 5V/0.2A



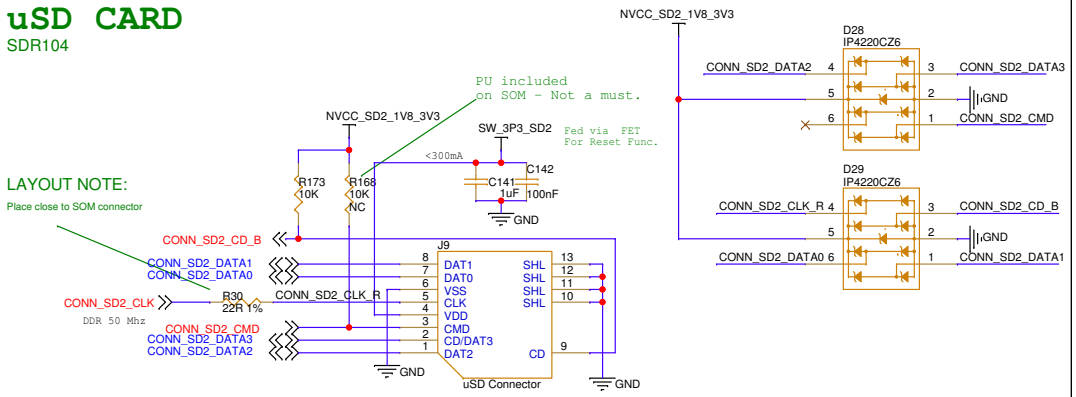
Variscite

Title: 04. Power, RTC,Board ID			
Size: A2	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R..5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 8 of 17	

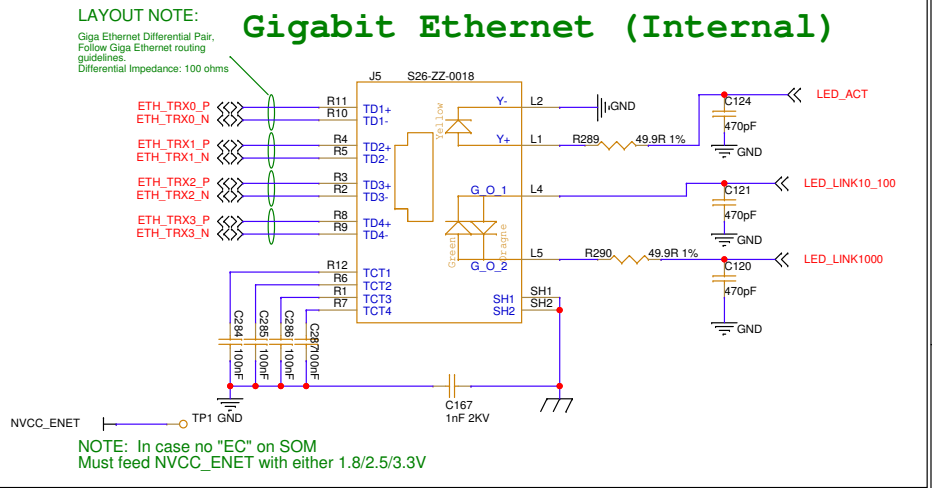
05. ETH, uSD, AUDIO, MIPI-CSI

uSD CARD

SDR104

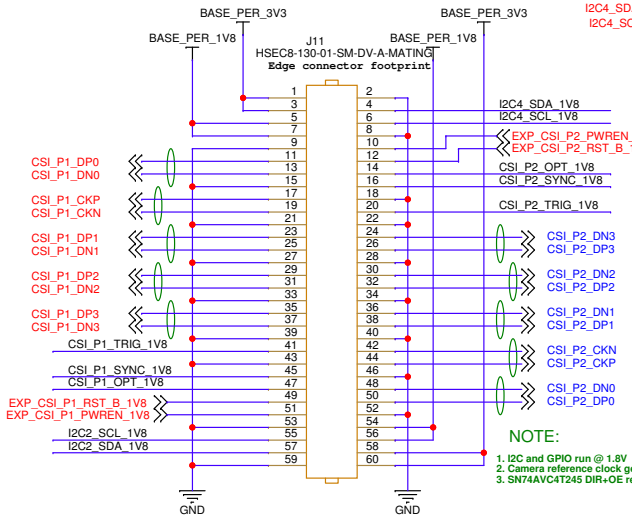


Gigabit Ethernet (Internal)



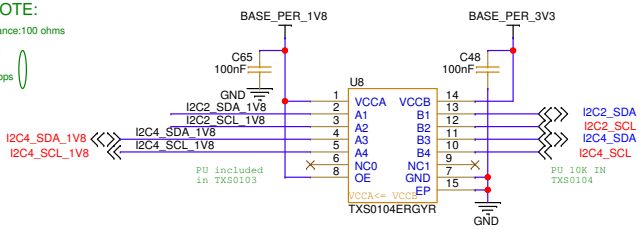
MIPI-CSI0 + MIPI-CSI1

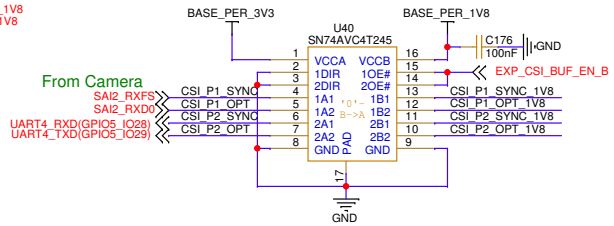
Connects to Variscite Custom MIPI-CSI2 Camera Board
Qualified with x2 OV5640.



LAYOUT NOTE:

Differential Impedance:100 ohms
SE 50 ohms
HS mode: DIFF
LP mode: SE
Lane rate 1.5Gbps

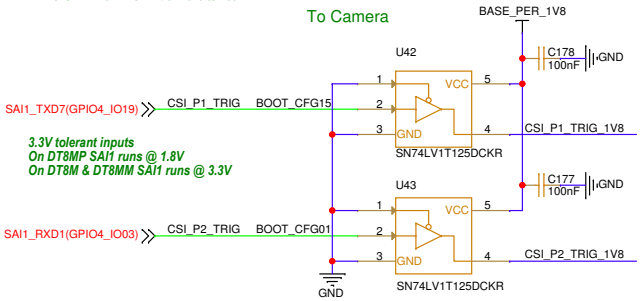




Note:
Camera control signals shared with Header
To use on the header disable buffer.
Please enable Pullup in DTS

NOTE:

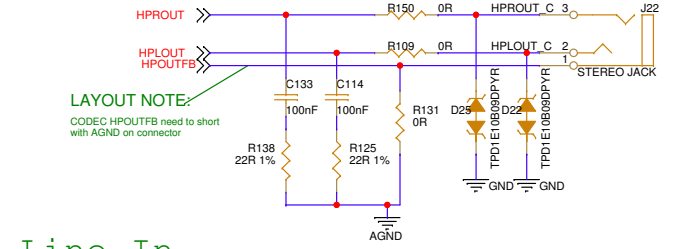
1. I2C and GPIO run @ 1.8V
2. Camera reference clock generated on camera board
3. SN74AVC4T245 DIR+OE ref'd to VccA



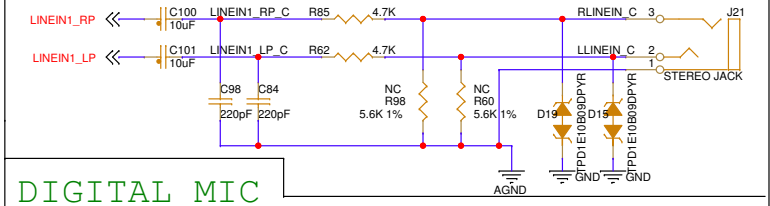
3.3V tolerant inputs
On DT8MP SAI1 runs @ 1.8V
On DT8M & DT8MM SAI1 runs @ 3.3V

AUDIO

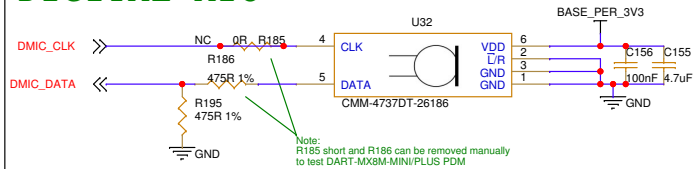
Headphones



Line In



DIGITAL MIC

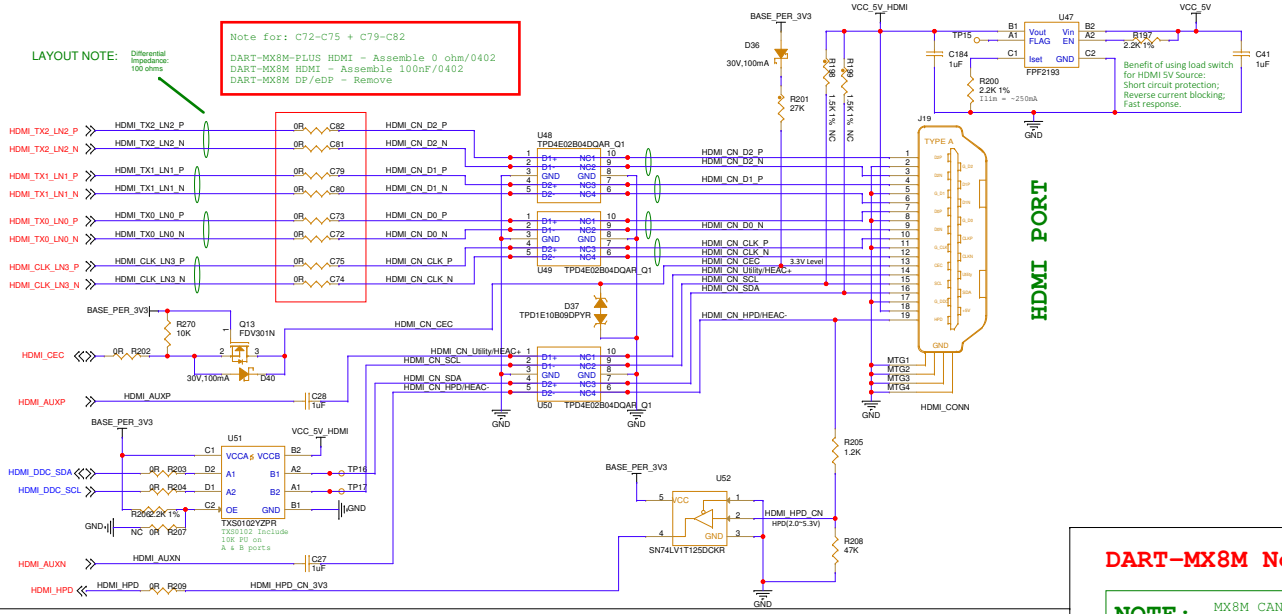


Variscite

Title: 05. ETH, uSD, AUDIO, MIPI-CSI			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 9 of 17	

06. HDMI, eDP – DART-MX8M-PLUS Optimised

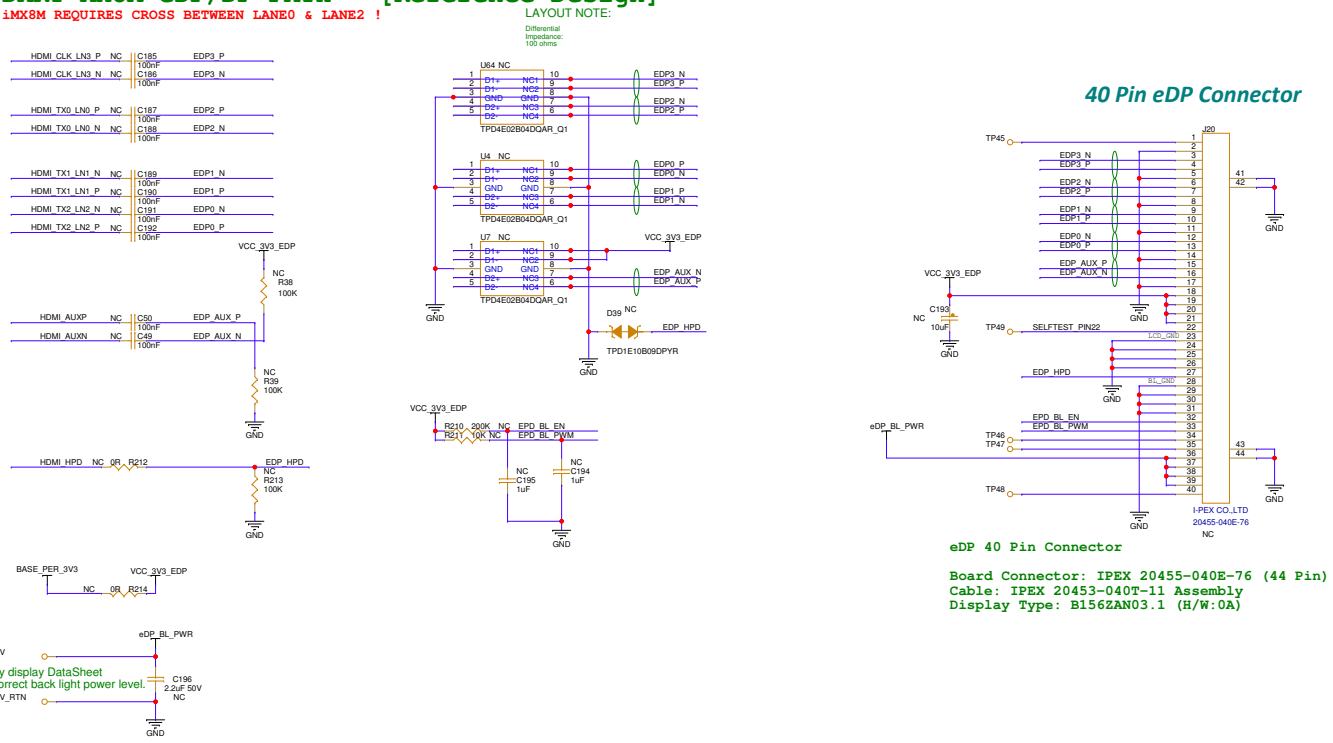
HDMI PATH



HDMI PORT

DART-MX8M eDP/DP PATH – [Reference Design]

iMX8M REQUIRES CROSS BETWEEN LANE0 & LANE2 !



40 Pin eDP Connector

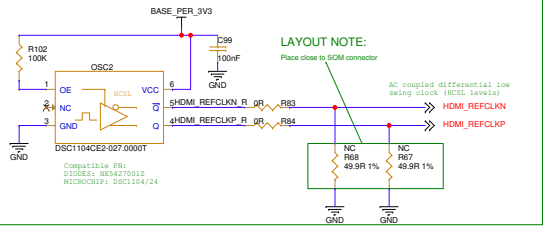
eDP 40 Pin Connector

Board Connector: IPEX 20455-040E-76 (44 Pin)
Cable: IPEX 20453-040T-11 Assembly
Display Type: B156ZAN03.1 (H/W:0A)

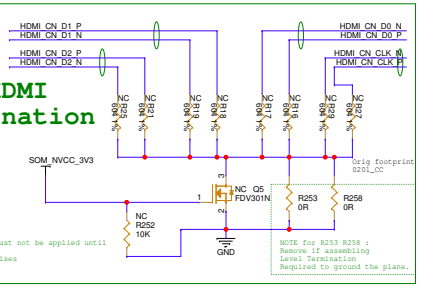
DART-MX8M Notes and required circuitry:

NOTE: MX8M CAN CONNECT DIRECTLY TO :
HDMI_CN_SCL & HDMI_CN_SDA
HDMI_CN_CEC
HDMI_CN_HPD

HDMI REFCLK



DART-MX8M HDMI Level Termination



Variscite

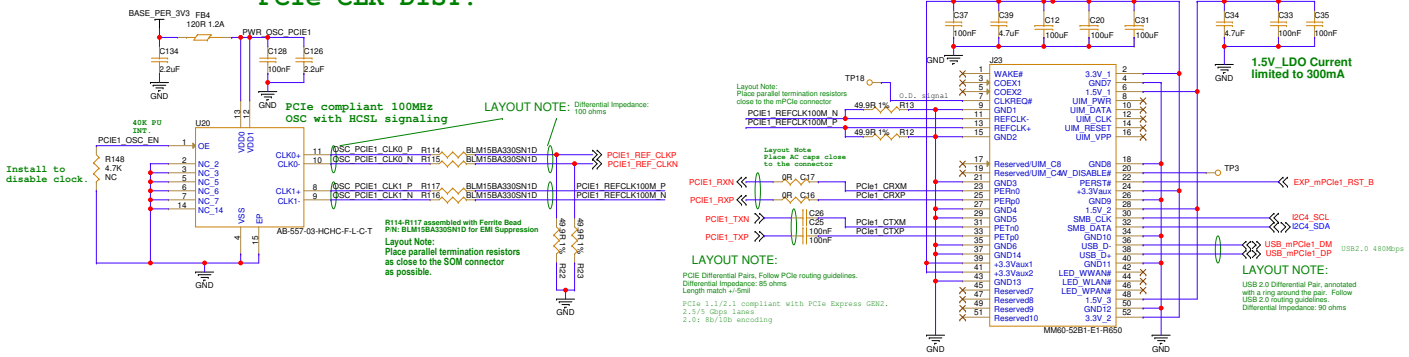
Title	06. HDMI , eDP		
Size A2	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R.1.5
Designer: Leonid S.		Approved By: <Approved By>	
Date: Wednesday, January 08, 2025		Sheet 10 of 17	

07. PCIe, QSPI, MIPI-DSI, USB DEBUG

Customboard 5V power supply is limited to 3A, shared with Board's USB devices. Do not connect devices which exceed current limitation.

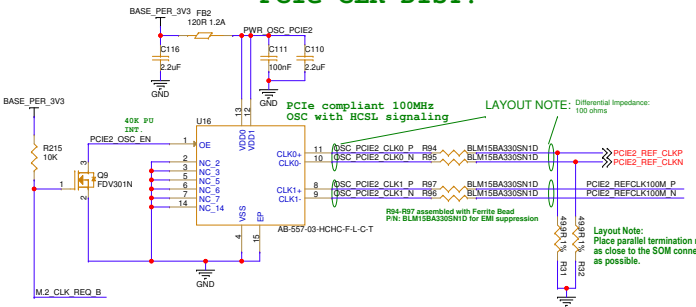
mPCIexp CS

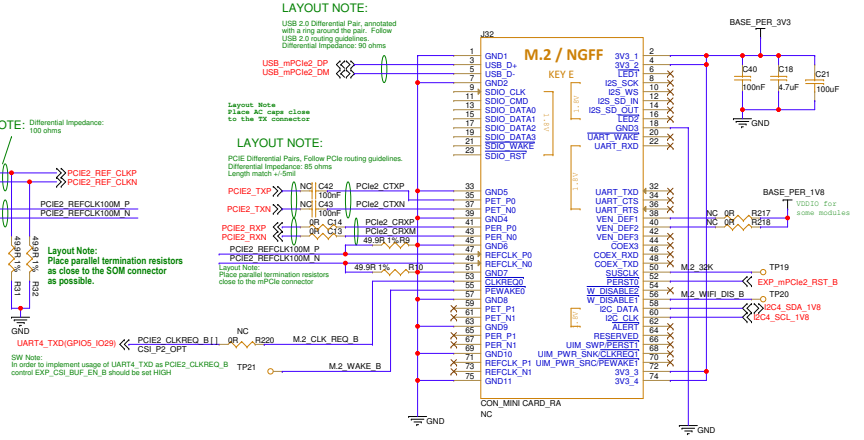
PCIe CLK DIST.



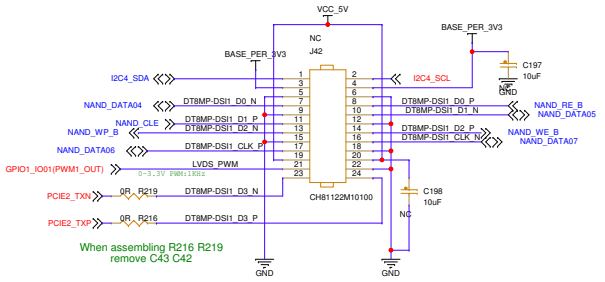
M.2. ON PS - [Reference Design]

PCIe CLK DIST.

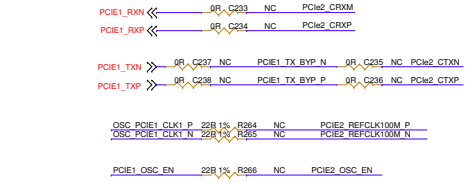




DART-MX8MP MIPI-DSI ON PS Compatible to Symphony J7+J8



PCIe1 TO M.2 PATH



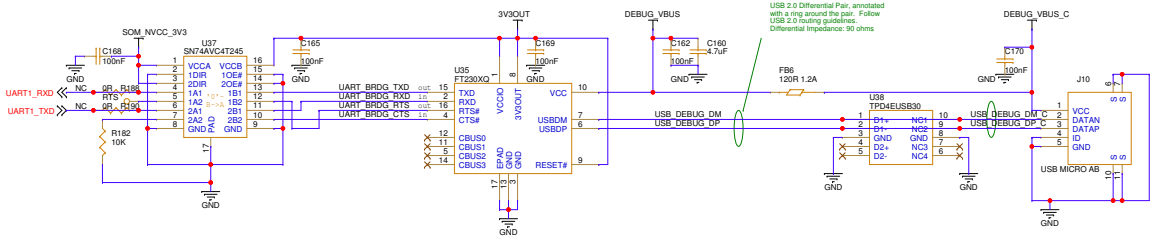
ASSY NOTE:
Customers requiring PCIe on DT8MP and DT8MM routed to M.2. connector (located on PS) should follow:

Remove
C16 C17 C26 C25 R116 R117 C13 C14 R96 R97

Assemble
C237 C238 (100nF)
C235 C236 (0 Ohm)
C233 C234 (0 Ohm)
R264 R265 (22 Ohm)

CLK_REQ_B path and enable not connected

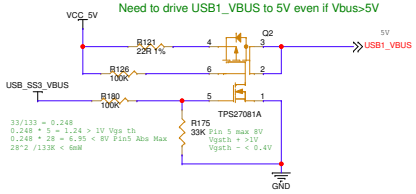
USB UART DEBUG



08. USB TYPE C, USB 3 HUB

USB#1 – DRP
USB TYPE C

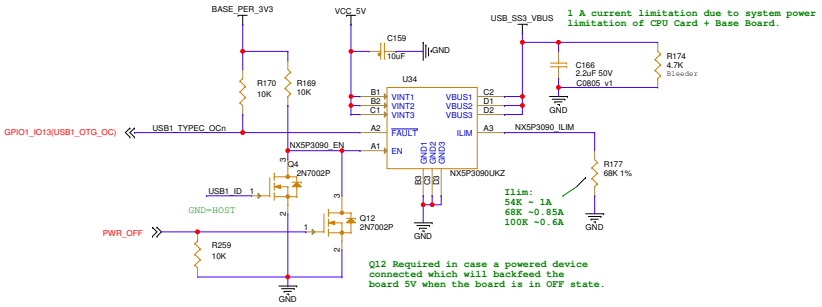
Need to drive USB1_VBUS to 5V even if Vbus>5V



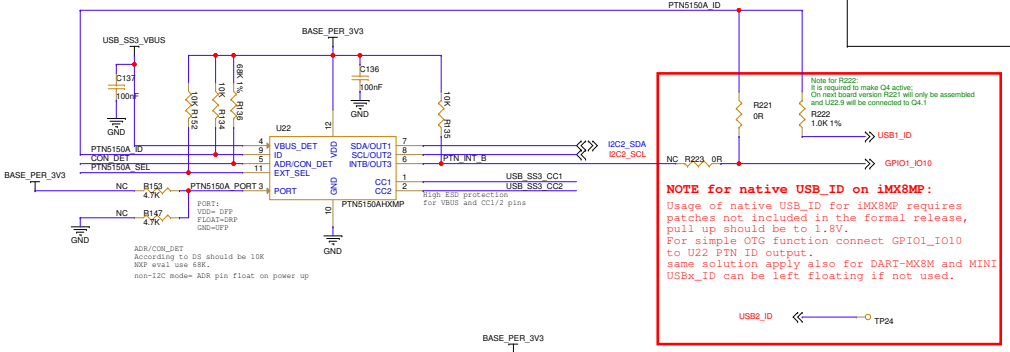
5V Source Load Switch

USB Profile 1 = 5 V @ 2 A

1 A current limitation due to system power limitation of CPU Card + Base Board.



Config Channel Logic Detection & Indication of Plug Orientation

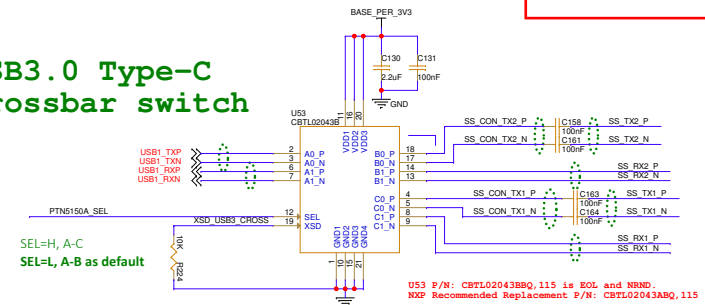


NOTE for native USB_ID on iMX8MP:

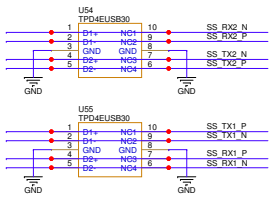
Usage of native USB_ID for iMX8MP requires patches not included in the formal release, pull up should be to 1.8V.
For simple OTG function connect GPIO1_IO10 to U22 PTN ID output.
same solution apply also for DART-MX8M and MINI USBx_ID can be left floating if not used.

USB2_ID — TP24

USB3.0 Type-C crossbar switch

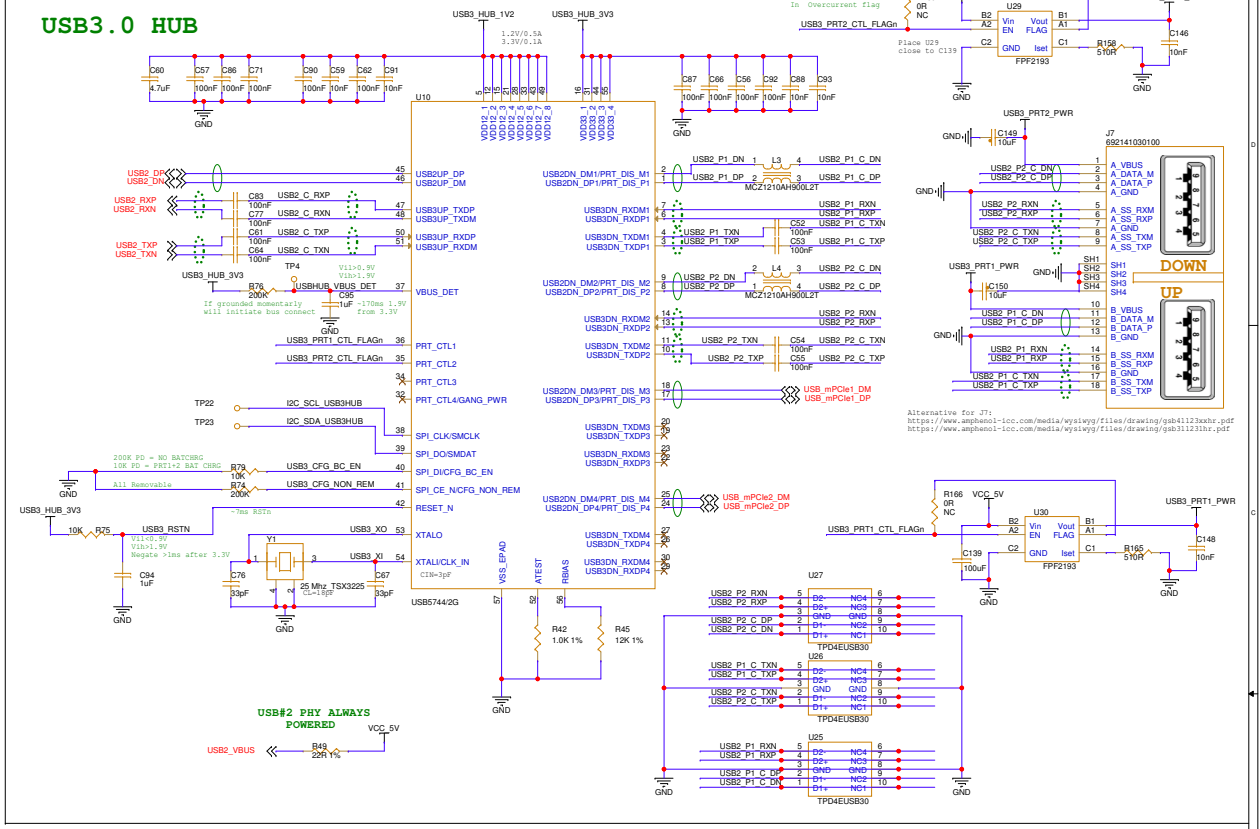


U53 P/N: CBTL02043BBQ,115 is EOL and NRND.
NXP Recommended Replacement P/N: CBTL02043ABQ,115



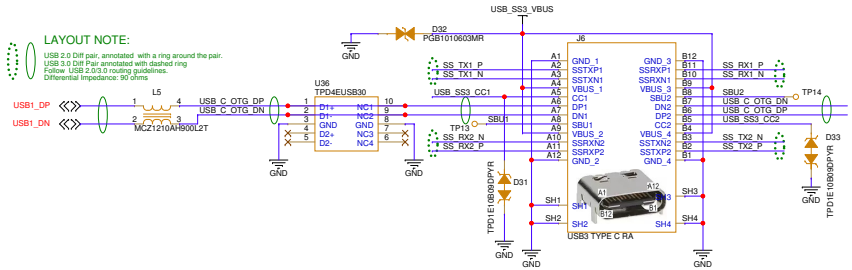
USB#2 – HOST
USB3.0 HUB

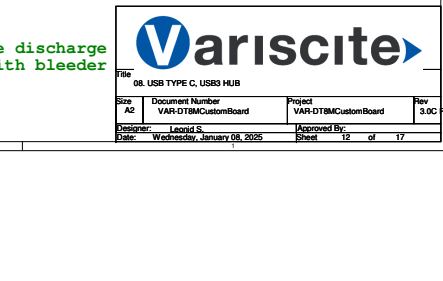
Note:
1.2V should rise before or at the same time as 3.3V
Straps should be valid >1ms after RST_N negate



Note:
VBUS active discharge replaced with bleeder

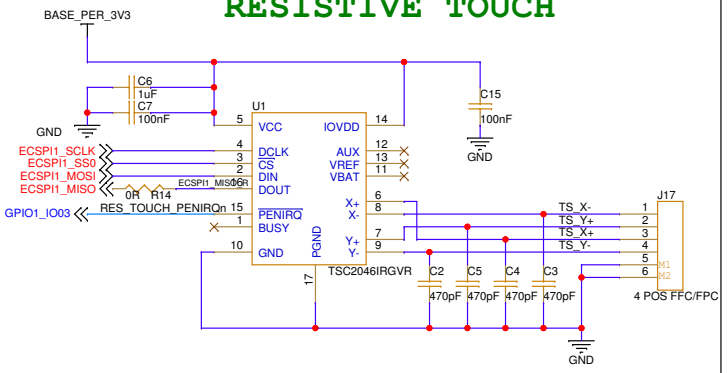
LAYOUT NOTE:
USB 2.0 Diff pair, annotated with a ring around the pair.
USB 3.0 Diff Pair annotated with dashed ring
Follow USB 2.0/3.0 routing guidelines.
Differential Impedance: 90 ohms





09. LVDS, TOUCH, JTAG, I2C EXP

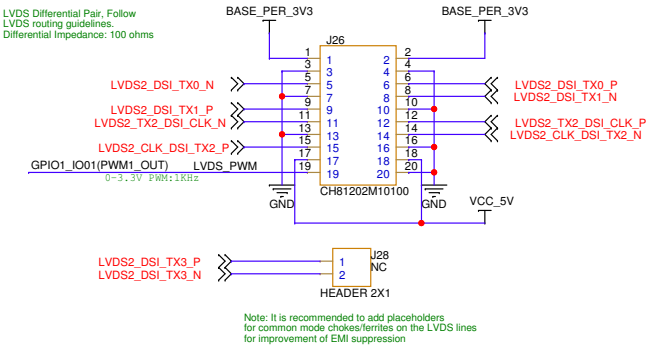
RESISTIVE TOUCH



LVDS CH1 DISPLAY

LAYOUT NOTE:

LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

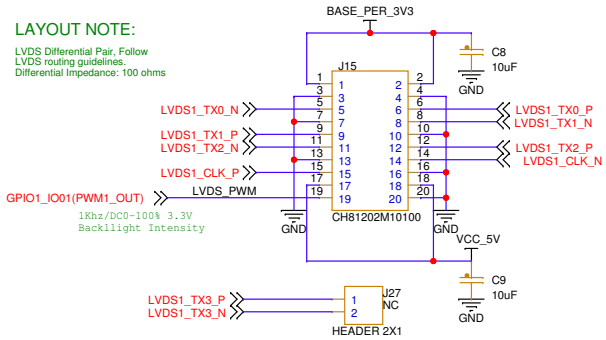


Note: It is recommended to add placeholders for common mode chokes/ferrites on the LVDS lines for improvement of EMI suppression

LVDS DISPLAY CH0

LAYOUT NOTE:

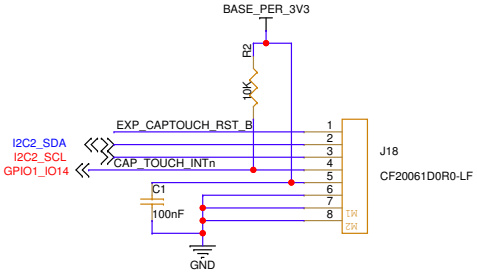
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms



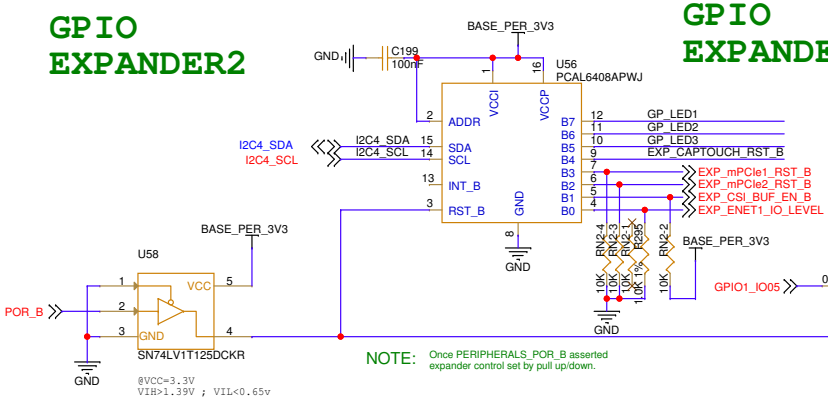
Note: It is recommended to add placeholders for common mode chokes/ferrites on the LVDS lines for improvement of EMI suppression

LCD: GKTW70SDAE4SE
5V/0.45A
3.3V/0.17A

CAPACITIVE TOUCH

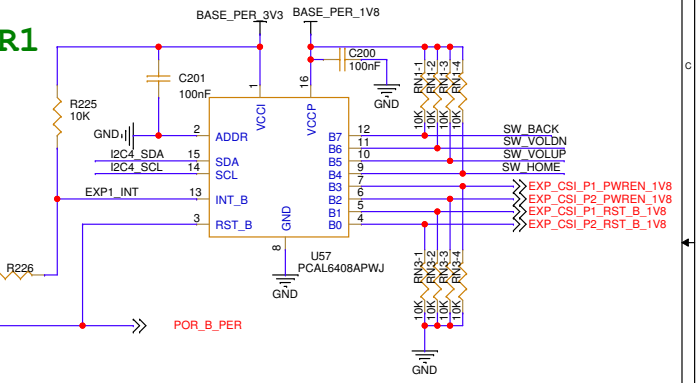


GPIO EXPANDER2

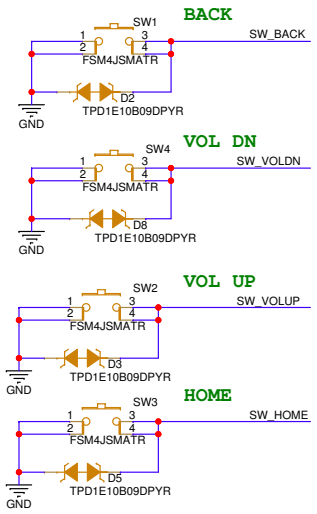


NOTE: Once PERIPHERALS_POR_B asserted expander control set by pull up/down.

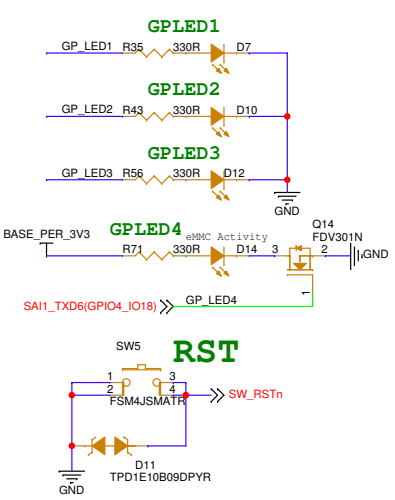
GPIO EXPANDER1



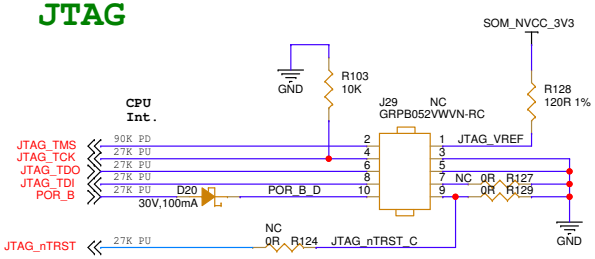
GP BUTTONS



GP LEDS



JTAG



NOTE: DT8MP JTAG_nTRST net connected to JTAG_MODE having 8.2K PD on SOM. Exposed for boundry scan.

The new 10 pin smaller connector is now becoming an industry standard.

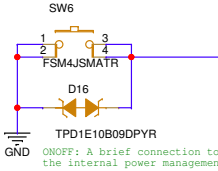
The ARM DStream comes with a 10-pin connector. If you need a ribbon, they can be purhased at Digikey:
Samtec Inc MPN: FFSD-05-D-04.00-01-N

If you need to expand to a 20-pin connector for a different JTAG device, the expander board can also be purchased at Digikey:
Olimex LTD MPN: ARM-JTAG-20-10

https://www.digikey.com/products/en/development-boards-kits-programmers/accessories/783?k=JTAG%20adapter

ON/OFF

PU Included on SOM



ONOFF: A brief connection to GND in OFF mode causes the internal power management state machine to change state to ON. In ON mode, a brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). An approximate 5 second or more connection to GND causes a forced OFF.

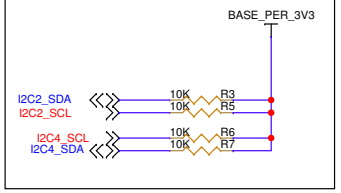
Not used leave NC

Variscite

Title	09. LVDS, TOUCH, JTAG, I2C EXP		
Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 13 of 17	

10. HEADERS, Mechanics, Pull Ups

I2C PULL UP



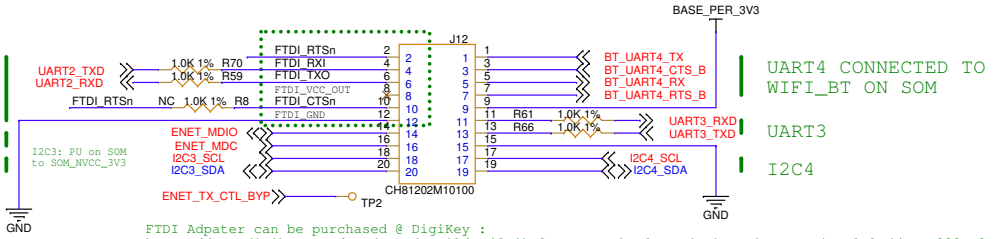
UART2 FTDI PINOUT

ENET0 I2C3

UART4 CONNECTED TO WIFI_BT ON SOM

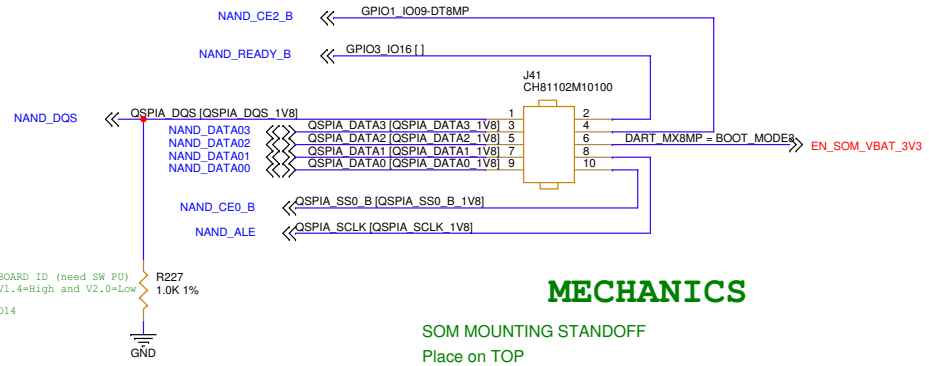
UART3

I2C4



FTDI Adpater can be purchased @ DigiKey :
https://www.digikey.com/product-detail/en/ftdi-future-technology-devices-international-ltd/TTL-232R-3V3/768-1015-ND/1836393
See pinout: http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_TTL-232R_CABLES.pdf

QSPI HEADER



HW NOTE:
Remove R229 R31 (see CAN-FD page) to use different ALT Func. on J13

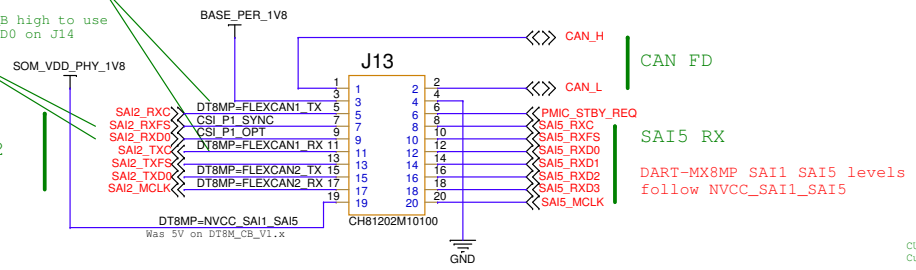
SW NOTE:
Set EXP_CSI_BUF_EN_B high to use SAI2_RXFS & SAI2_RXD0 on J14

SAI2

CAN FD

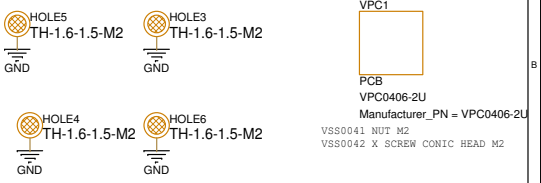
SAI5 RX

DART-MX8MP SAI1 SAI5 levels follow NVCC_SAI1_SAI5

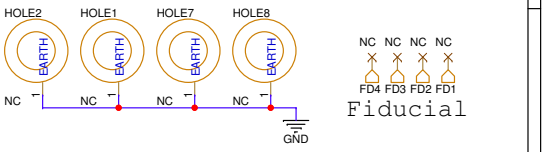


MECHANICS

SOM MOUNTING STANDOFF
Place on TOP

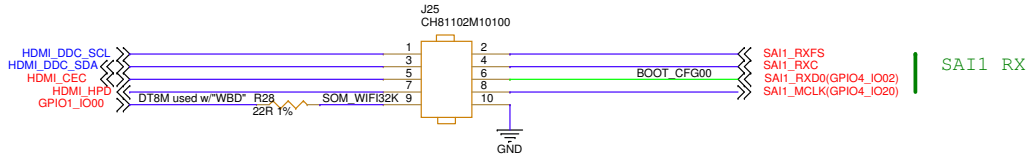


CHASSIS HOLES



HDMI DDC
HPD CEC

SAI1 RX

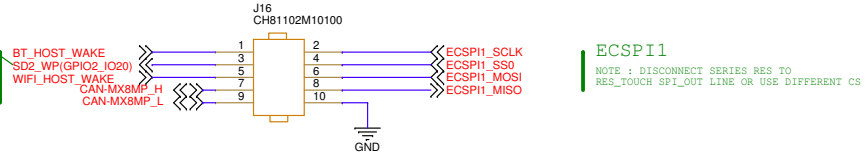


SW NOTE:
Requires GPIO on J1.29 configured as interrupt input

BT/WIFI
HOST WAKE
DT8MP CAN

ECSPI1

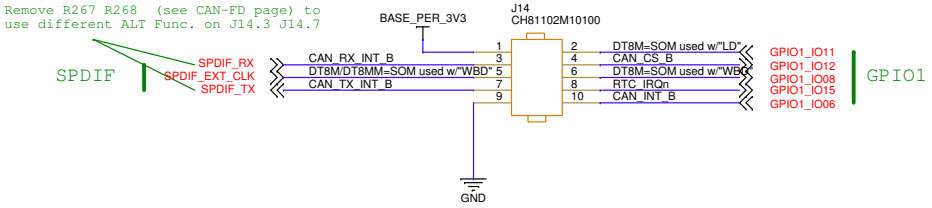
NOTE : DISCONNECT SERIES RES TO RES_TOUCH SPI_OUT LINE OR USE DIFFERENT CS



HW NOTE:
Remove R267 R268 (see CAN-FD page) to use different ALT Func. on J14.3 J14.7

SPDIF

GPIO1



Variscite

Title: 10. HEADERS, Mechanics, Pull Ups			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 14 of 17	

11. BOOT CONFIG & MODE

			INT. BOOT	EXT. BOOT	
SAI1_RXD0(GPIO4_IO02)		BOOT_CFG00	0	0	Need to Enable PU in DTS; See pp. 5
SAI1_RXD1(GPIO4_IO03)	CSI_P2_TRIG	BOOT_CFG01	0	0	
SAI1_RXD2(GPIO4_IO04)	ENET1_MDC	BOOT_CFG02	0	0	
SAI1_RXD3(GPIO4_IO05)	ENET1_MDIO	BOOT_CFG03	0	0	
SAI1_RXD4(GPIO4_IO06)	ENET1_RGMII_RD0	BOOT_CFG04	0	0	
SAI1_RXD5(GPIO4_IO07)	ENET1_RGMII_RD1	BOOT_CFG05	0	0	
SAI1_RXD6(GPIO4_IO08)	ENET1_RGMII_RD2	BOOT_CFG06	0	0	
SAI1_RXD7(GPIO4_IO09)	ENET1_RGMII_RD3	BOOT_CFG07	0	0	
SAI1_TXD0(GPIO4_IO12)	ENET1_RGMII_TD0	BOOT_CFG08	0	0	
SAI1_TXD1(GPIO4_IO13)	ENET1_RGMII_TD1	BOOT_CFG09	0	0	
SAI1_TXD2(GPIO4_IO14)	ENET1_RGMII_TD2	BOOT_CFG10	0	1	
SAI1_TXD3(GPIO4_IO15)	ENET1_RGMII_TD3	BOOT_CFG11	0	0	
SAI1_TXD4(GPIO4_IO16)	ENET1_RGMII_TX_CTL	BOOT_CFG12	0	1	
SAI1_TXD5(GPIO4_IO17)	ENET1_RGMII_TXC	BOOT_CFG13	1	0	
SAI1_TXD6(GPIO4_IO18)	GP_LED4	BOOT_CFG14	0	0	
SAI1_TXD7(GPIO4_IO19)	CSI_P1_TRIG	BOOT_CFG15	0	0	

10K R52 NC BOOT_CFG00 — SAI1_RXD0(GPIO4_IO02)
10K R228 NC BOOT_CFG01 CSI_P2_TRIG — SAI1_RXD1(GPIO4_IO03)
10K R53 NC BOOT_CFG02 ENET1_MDC — SAI1_RXD2(GPIO4_IO04)
10K R93 NC BOOT_CFG03 ENET1_MDIO — SAI1_RXD3(GPIO4_IO05)
10K R58 NC BOOT_CFG04 ENET1_RGMII_RD0 — SAI1_RXD4(GPIO4_IO06)
10K R55 NC BOOT_CFG05 ENET1_RGMII_RD1 — SAI1_RXD5(GPIO4_IO07)
10K R92 NC BOOT_CFG06 ENET1_RGMII_RD2 — SAI1_RXD6(GPIO4_IO08)
10K R54 NC BOOT_CFG07 ENET1_RGMII_RD3 — SAI1_RXD7(GPIO4_IO09)

GND

POR_B_PER
R254 10K
C230 4.7uF
GND
POR_B_PER_DELAY

SOM_NVCC_3V3
C103 100nF GND

Vih >1.39V
Vil <0.65V

BOOT_CFG

U19 SN74LV1T125DCKR
U18 SN74LV1T125DCKR
U17 SN74AUP1G240DCK
VCC GND

10K R91 NC BOOT_CFG08 ENET1_RGMII_TD0 — SAI1_TXD0(GPIO4_IO12)
10K R64 NC BOOT_CFG09 ENET1_RGMII_TD1 — SAI1_TXD1(GPIO4_IO13)
10K R89 BOOT_CFG10 ENET1_RGMII_TD2 — SAI1_TXD2(GPIO4_IO14)
10K R112 NC BOOT_CFG11 ENET1_RGMII_TD3 — SAI1_TXD3(GPIO4_IO15)
10K R90 BOOT_CFG12 ENET1_RGMII_TX_CTL — SAI1_TXD4(GPIO4_IO16)
10K R107 BOOT_CFG13 ENET1_RGMII_TXC — SAI1_TXD5(GPIO4_IO17)
10K R113 NC BOOT_CFG14 GP_LED4 — SAI1_TXD6(GPIO4_IO18)
10K R111 NC BOOT_CFG15 CSI_P1_TRIG — SAI1_TXD7(GPIO4_IO19)

C104 100nF GND

U17 U18 U19 Note:
* Tristate buffers required not to pull ENET1 to 3.3V while running @ lower voltage.
* Buffers required for DART-MX8M & DART-MX8M-MINI
* For DART-MX8M-PLUS only U19 required

SOM_NVCC_3V3
R106 10K
BOOT_CFG
D21
SW7 TDA01H0SB1R
BOOT CFG PRIORITY:
H Ext. SD Card
L Int. eMMC

SOM_NVCC_3V3
R87 4.7K
R100 4.7K NC
R88 10K NC
R99 4.7K
BOOT_MODE0
BOOT_MODE1
GND

Notes:
a. Sampled on rising edge of POR_B
b. SOC PD during POR_B and after on BOOT CFG[15:0] and BOOTMODE[1:0]
c. BOOT_MODE[1:0] ="10" is Internal Boot - Always used.
d. Active boot cfg for one dip sw sel EXTERNAL/INTERNAL

DART-MX8M-MINI Notes:
b. Boot config lines do not follow the Mini datasheet in full DART-MX8M-MINI have added logic to be compatible to DART-MX8M

DART-MX8M-PLUS Notes:
a. Boot configuration set only by SAI1_TXD2 connected on DART via buffer to BOOT_MODE0

i.MX8M Plus Boot Mode

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit) Default
0	0	1	1	USDHC2 (SD boot only, SD2)

CustomBoard Net: BOOT_MODE0 SAI1_TXD2
EN_SOM_VBAT_3V3 BOOT_MODE1

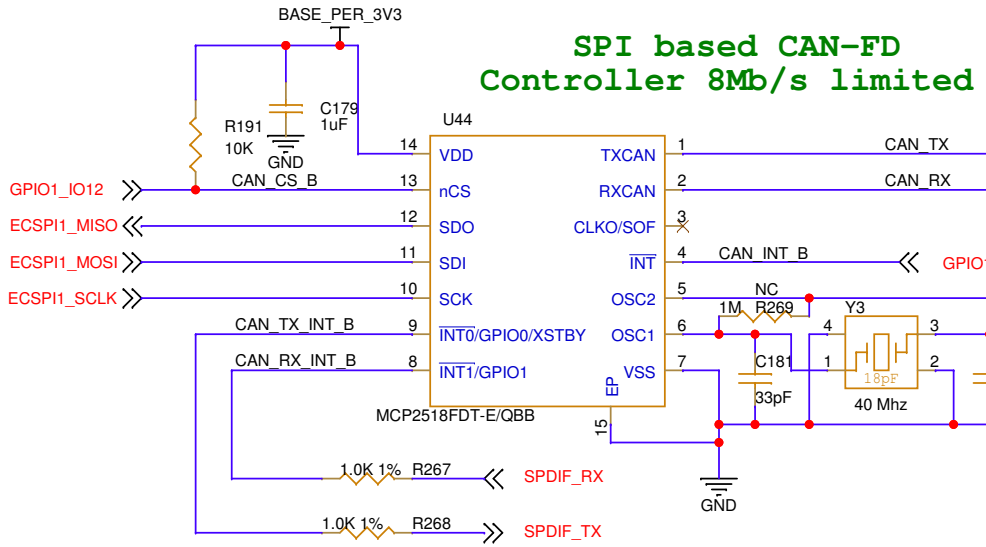
DART-MX8MP BOOT MODE

Variscite

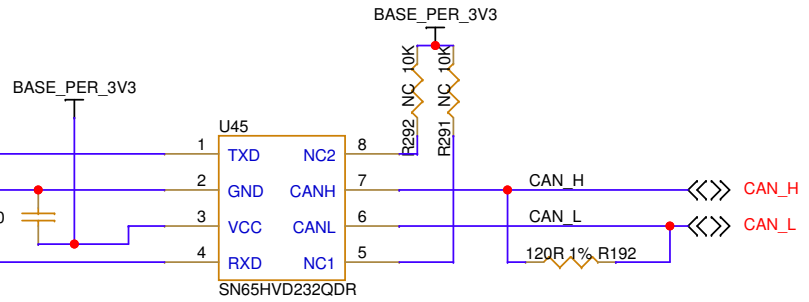
Title: 11. BOOT CONFIG & MODE			
Size: B	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 15 of 17	

13. CAN FD Interface

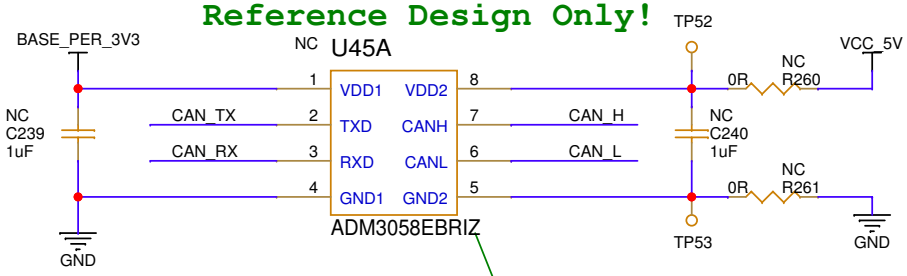
SPI based CAN-FD Controller 8Mb/s limited



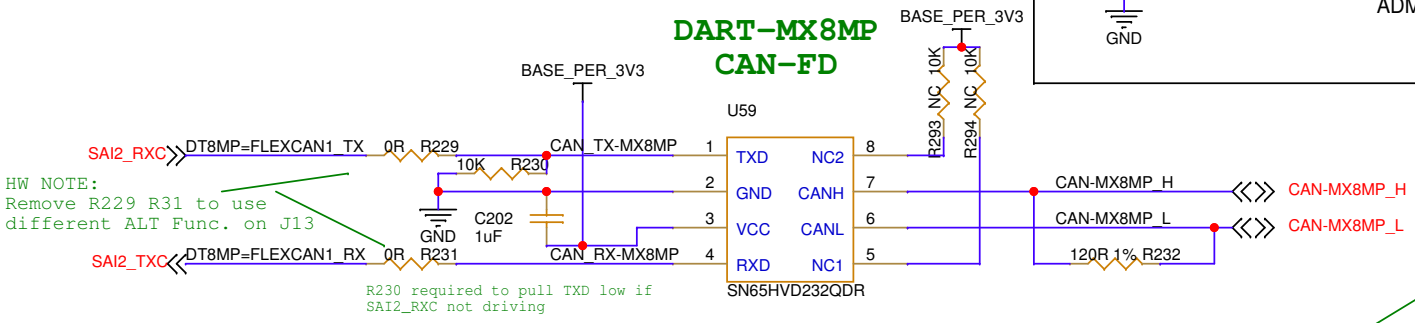
CAN PHY 5Mb/s Limited



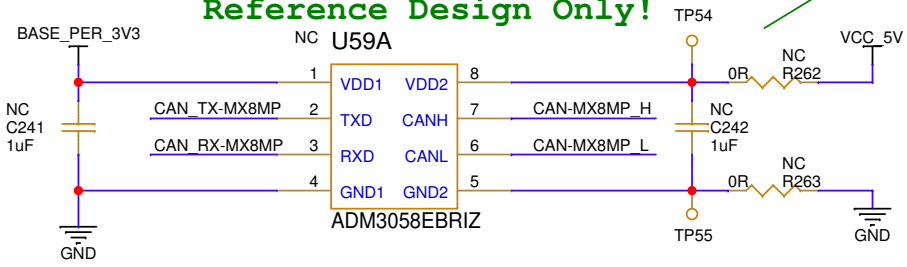
CAN PHY 12Mb/s Reference Design Only!



DART-MX8MP CAN-FD



CAN PHY 12Mb/s Reference Design Only!



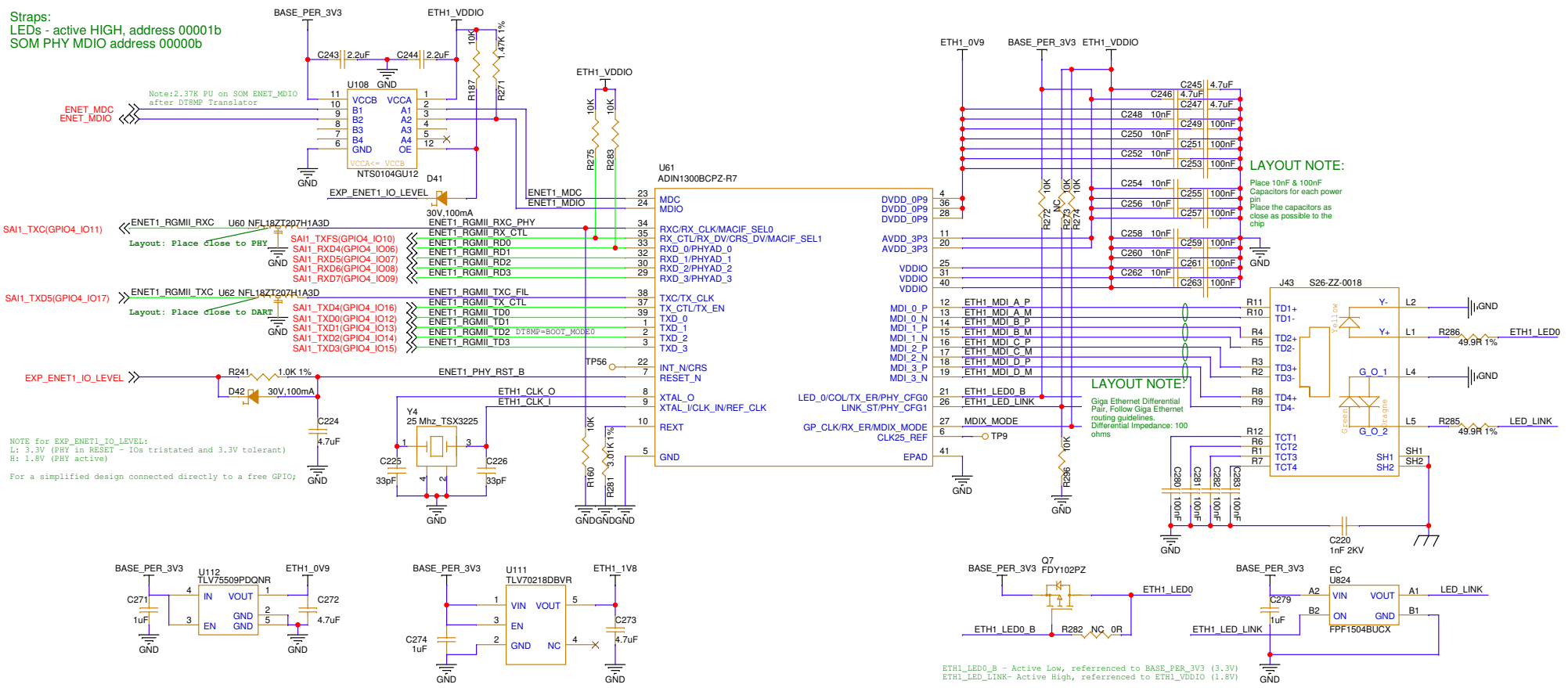
NOTE FOR U59A U45A

- Located on bottom side
- When assembling the ADM3058E IC removal of TCAN332 is a must!

Variscite

Title: 12. CAN FD Interface			
Size: A4	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 16 of 17	

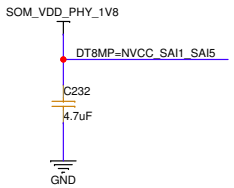
13. DART-MX8MP- ENET1 Gigabit Ethernet



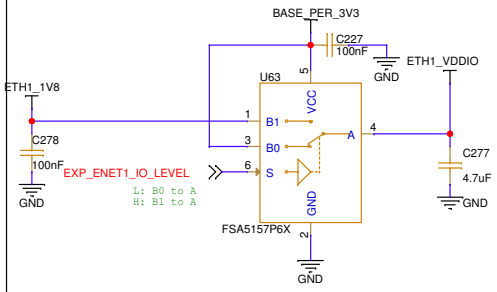
NOTE:
For DT8MP net SOM_VDD_PHY_1V8 connected to NVCC_SAI1_SAI5 which is an output from the DT8MP programmable PMIC LDO.

This output voltage will set SAI1 and SAI5 pads voltage level;
With DT8MCustomBoard-V1.x and earlier it is set to 3.3V.
On DT8MCustomBoard-V2.x it is set to 1.8V for RGMII.

Bypass with 4.7uF min. 6.3V capacitor.



NOTE for U63:
Required for compatibility to DT8M & DT8MM where SAI1 levels are fixed to 3.3V;



NOTE:
Test points below used to access DT8M & DT8MM SAI1 signals;

Levels are fixed to 3.3V by modules;

SAI1_RXD2(GPIO4_IO04)	DT8MP-ENET1_MDC	TP50
SAI1_RXD3(GPIO4_IO05)	DT8MP-ENET1_MDIO	TP51
SAI1_RXD4(GPIO4_IO06)	ENET1_RGMII_RD0	TP31
SAI1_RXD5(GPIO4_IO07)	ENET1_RGMII_RD1	TP33
SAI1_RXD6(GPIO4_IO08)	ENET1_RGMII_RD2	TP37
SAI1_RXD7(GPIO4_IO09)	ENET1_RGMII_RD3	TP35
SAI1_TXC(GPIO4_IO11)	ENET1_RGMII_RXC	TP40
SAI1_TXFS(GPIO4_IO10)	ENET1_RGMII_RX_CTL	TP41
SAI1_TXD0(GPIO4_IO12)	ENET1_RGMII_TD0	TP32
SAI1_TXD1(GPIO4_IO13)	ENET1_RGMII_TD1	TP34
SAI1_TXD2(GPIO4_IO14)	ENET1_RGMII_TD2	TP38
SAI1_TXD3(GPIO4_IO15)	ENET1_RGMII_TD3	TP39
SAI1_TXD5(GPIO4_IO17)	ENET1_RGMII_TXC	TP36
SAI1_TXD4(GPIO4_IO16)	ENET1_RGMII_TX_CTL	TP42

Variscite

Title: 13. Ethernet2			
Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.5
Designer: Leonid S.		Approved By:	
Date: Wednesday, January 08, 2025		Sheet 17 of 17	