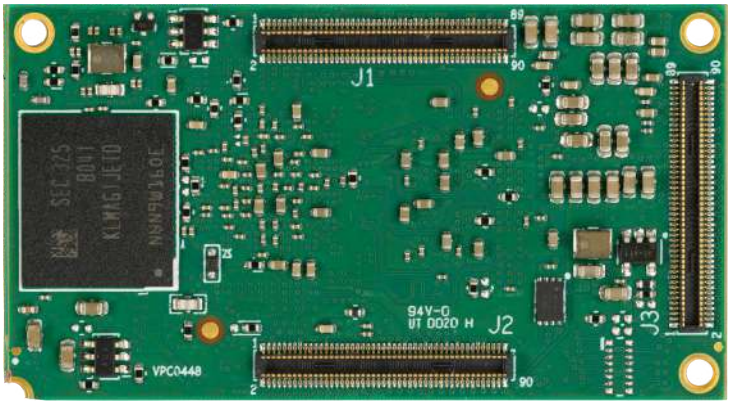
VARISCITE LTD.

DART-MX8M-MINI V1.x Datasheet

NXP i.MX 8M Mini™ - based System-on-Module



VARISCITE LTD.

DART-MX8M-MINI Datasheet

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1. Document Revision History

Revision	Date	Notes
1.00	Feb 25, 2019	Initial Release
1.01	May 20, 2019	Correct SOM height Correct LVDS bridge options description section 8.1 Updated: Table 4 (J2.16 AC Assy), Table 27 added J2.14 J2.16 and section 9.4. Add special note for DMIC_DATA (applicable only for "AC" SOM subset only) voltage level should be 1.8V.
1.02	May 20, 2019	Section 5.4 removed "SIG certified Bluetooth driver" from LWB5 key features.
1.03	Aug 09, 2019	Correct pins J2.2 and J2.14 Audio Codec bypass SOC functions; See Tables 4,7,31,32,38,49,51
1.04	Feb 10, 2020	Remove "Not Recommended" note from Table 3. J1.24 on POR_B Correct block diagram section 4.3 (I2C3 connected to Audio Codec) Added note on I2C3 "Shared with "AC" "
1.05	Jul 07, 2020	Updated power consumption Table: 61 for Suspend mode
1.06	Jan 03, 2021	Update Block Diagram for missing QSPI interface
1.07	Feb 23, 2021	NVCC_3V3 output power supply capabilities section added
1.08	Apr 28, 2021	Updated Reliability data section 10
1.09	Jul 22, 2021	Added note on BOOT_CFG11 Section 8.19
1.10	Nov 04, 2021	Updated block diagram Added EEPROM section 5.8 Updated Table 53 – Added signals BOOT_MODE0/1
1.11	Dec 27, 2021	Added Section 5.1.21 – Degradation of internal IO pullup/pulldown current capability
1.12	Feb 06, 2022	Update the table in section 6
1.13	Mar 16, 2022	Added Ethernet PHY ADIN1300 – Updated sections 4.3, 5.6, 7.3, 8.3, 9.5 Updated section 5.3
1.14	May 1, 2022	Updated sections: 4.2, 5.4, 8.4
1.15	Feb 26, 2023	Updated the eMMC on sections- 4.2 ,5.2 ,6 Updated section 10

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4. Overview

4.1. General Information

The DART-MX 8M MINI offers latest video and audio experience combining state-of-the-art media-specific features with high-performance processing while optimized for lowest power consumption. It perfectly fits various embedded products, the growing market of connected and portable devices and segment for connected streaming audio/video devices, scanning/imaging devices and various devices requiring high-performance, low-power processors.
The product is based on the NXP i.MX 8M MINI family of multi-purpose processors, featuring a quad Arm® Cortex®-A53 core up to 2GHz with a general-purpose Cortex®-M4 400 MHz core processor for low-power processing.

This heterogeneous multicore processing architecture enables the device to run an open operating system like Linux on the Cortex-A53 core and an RTOS like FreeRTOS™ on the Cortex-M4 core for time and security critical tasks.

The DART-MX8M-MINI MINI provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

- VAR-DT8MCustomBoard – evaluation board
  - ✓ Carrier Board, compatible with DART-MX8M, DART-MX8M-MINI
  - ✓ Schematics
- VAR-DVK-MX8M-MINI full development kit, including:
  - ✓ VAR-DT8MCustomBoard
  - ✓ DART-MX8M-MINI
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

Contact Variscite support services for further information: support@variscite.com.

4.2. Feature Summary

- NXP i.MX 8M-MINI series SOC
  - i.MX 8M-MINI family ARM® Cortex™-A53 Core up to 2GHz
  - 400MHz ARM® Cortex™-M4
  - Up to 4GB LPDDR4 RAM
  - 8-bit up to 128GB eMMC boot and storage
- Display Support
  - Dual channel LVDS display interface
  - MIPI DSI
- Networking
  - 10/100/1000 Mbit/s Ethernet Interface
  - Certified Wi-Fi 802.11 ac/a/b/g/n
  - Bluetooth: 5.2/BLE
- Camera
  - MIPI-CSI – CMOS Serial camera Interface 4 lanes
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - 6x Digital audio (SAI, SPDIF, PDM)
- USB
  - 2 x USB 2.0 OTG
- Other Interfaces
  - SDIO/MMC
  - PCIe v2.0
  - Serial interfaces (ECSPI, QSPI, I2C, UART, JTAG)
  - GPIOs
- Single power supply: 3.5V – 5V
- Dimensions (W X L X H): 30 x 55 x 5.13 [mm]
- Industrial temperature range: -40 to 85 °C

4.3. Block Diagram

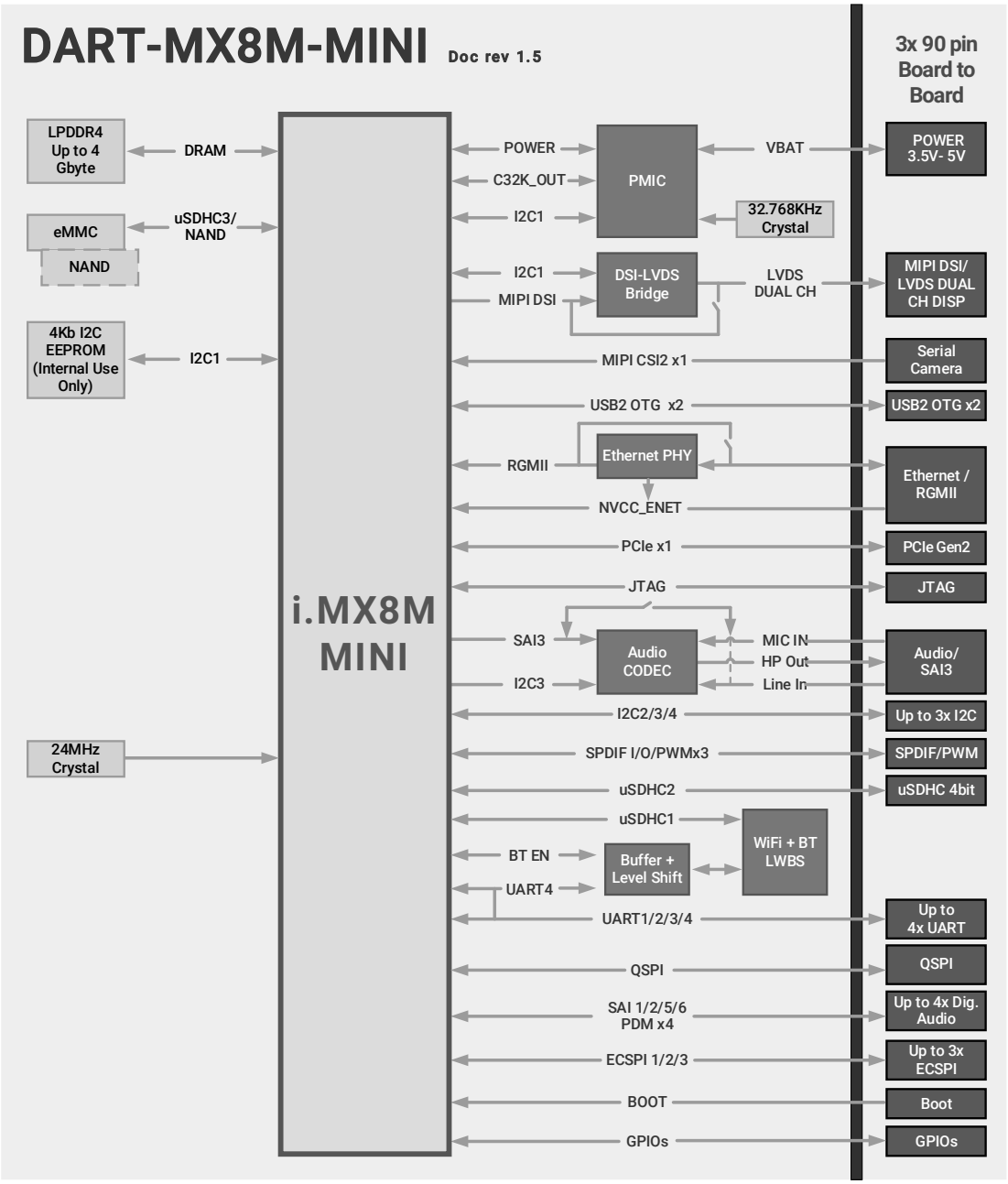


Figure 1 : DART-MX8M-MINI Block Diagram

5. Main Hardware Components

This section summarizes the main hardware building blocks of the DART-MX8M-MINI.

5.1. NXP i.MX 8M-MINI

5.1.1. Overview

The i.MX 8M MINI is a family of products focused on delivering an excellent video and audio experience, combining media-specific features with high-performance processing optimized for low-power consumption.
The i.MX 8M MINI Media Applications Processor is built to achieve both high performance and low power consumption and rely on a powerful fully coherent core complex based on a quad Cortex-A53 cluster with video and graphics accelerators.
The i.MX 8M Family provides additional computing resources and peripherals:

- Advanced security modules for secure boot, cipher acceleration and DRM support
- General purpose Cortex-M4 processor for low power processing
- A wide range of audio interfaces including I2S, AC97, TDM and S/PDIF
- Large set of peripherals that are commonly used in consumer/industrial markets including USB 2.0, PCIe and Ethernet

5.1.2. i.MX8M Block Diagram

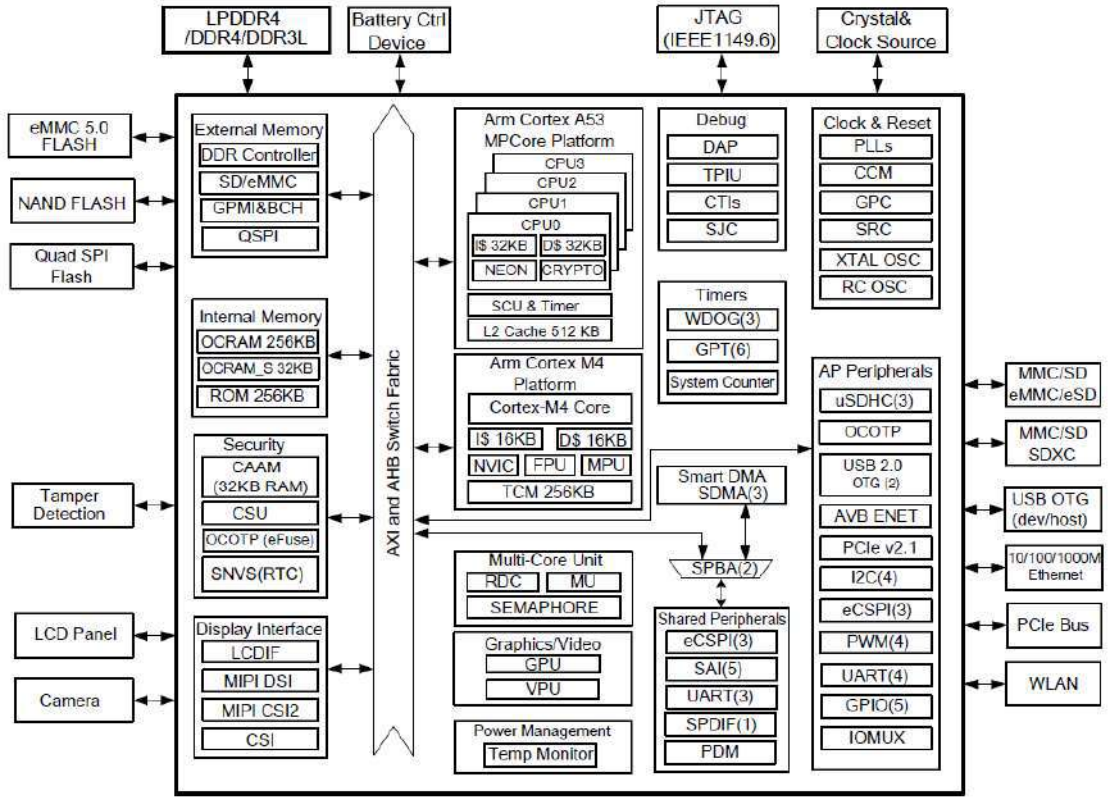


Figure 2 : iMX 8M-MINI Block Diagram

5.1.3. ARM Cortex-A53 MPCore™ Platform

- The i.MX 8M Family Applications Processors are based on the Arm Cortex-A53
- MPCore™ Platform, which has the following features:
    - Quad symmetric Cortex-A53 processors, including:
    - 32 KB L1 Instruction Cache
    - 32 KB L1 Data Cache
    - Media Processing Engine (MPE) with NEON technology supporting the
- Advanced Single Instruction Multiple Data architecture
    - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
    - Support of 64-bit Armv8-A architecture
- 512 KB unified L2 cache
- Target frequency of 2GHz

5.1.4. Arm Cortex-M4 Platform

Cortex-M4 Core Platform include the following:
• Low power microcontroller available for customer application:
    - Low power standby mode
    - IoT features including Weave
    - Manage IR or wireless remote

• Arm Cortex M4 CPU Processor, including:
    - 16 KB L1 Instruction Cache
    - 16 KB L1 Data Cache
    - 256 KB TCM
    - Target frequency of 400MHz

5.1.5. System Bus and Interconnect

System bus and interconnect include the following:

- Network interconnect (NoC) AXI arbiter
- Quality of service controller (QoSC) to configure priorities and limits of AXI transactions
- Performance monitor (PERFMON) to monitor AXI bus activity
- Debug monitor (DBGMON) to record AXI transactions preceding a system reset

5.1.6. Clocking and Resets

Clocking and resets include:

- Clock control module (CCM) provides centralized clock generation and control
- Simplified clock tree structure
- Unified clock programming model for each clock root
- Multicore awareness for resource domains
- System reset controller (SRC) provides reset generation and distribution

5.1.7. Interrupts and DMA

Interrupts and DMA include:

- 128 shared peripheral interrupts routed to Cortex-A53 Global Interrupt Controller (GIC) and Cortex-M4 nested vector interrupt controller (NVIC) for flexible interrupt handling
- Three Smart direct memory access (SDMA) engines. Although these three engines are identical to each other, they are integrated into the processor to serve different peripherals.
    - SDMA-1 is a general-purpose DMA engine which can be used by low speed peripherals including UART, SPI and also others peripherals.
    - SDMA-2 and SMDA-3 is used for audio interface, including SAI-1/2/3/5/6, SPDIF and PDM audio input.

5.1.8. On-Chip Memory

The on-chip memory system consists of the following:

- Boot ROM (256KB)
- On-chip RAM (256KB + 32KB)

5.1.9. External Memory Interface

The external memory interfaces supported on this chip include:

- 16/32-bit DRAM Interface:
    - LPDDR4-3000
- 8-bit NAND FLASH, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)
- eMMC 5.0 FLASH (2 interfaces)
- SPI NOR FLASH (3 interfaces)
- FlexSPI FLASH with support for XIP (for M4 in low-power mode) and parallel read mode of two identical FLASH devices

5.1.10. Timers

The timers on this chip include:

- One local generic timer integrated into each Cortex-A53 CPU
- Global system counter with timer bus interface to Cortex-A53 MPCore generic timers
- One local system timer (SysTick) integrated into the Cortex-M4 CPU
- Six general purpose timer (GPT) modules
- Three watchdog timer (WDOG) modules
- Four pulse width modulation (PWM) modules

5.1.11. Graphics Processing Unit (GPU)

The chip incorporates the following Graphics Processing Unit (GPU) features:

- 2D/3D acceleration
- Target frequency of 800 MHz
- Support OpenGL ES 1.1, 2.0, OpenVG 1.1
- TrustZone support using a local MMU to manage secure regions
- Support multi-source composition
- Support one-pass filter
- Support tile format

5.1.12. Video Processing Unit (VPU)

The chip incorporates the following Video Processing Unit (VPU) features:

- 1080p60 VP9 Profile 0, 2 (10 bit) Decoder (Hantro G2)
- 1080p60 HEVC/H.265 Decoder (Hantro G2)
- 1080p60 AVC/H.264 Baseline, Main, High Decoder (Hantro G1)
- 1080p60 VP8 Decoder (Hantro G1)
- 1080p60 AVC/H.264 Encoder (Hantro H1)
- 1080p60 VP8 Encoder (Hantro H1)
- TrustZone support

5.1.13. Display/Camera Interfaces

The chip has the following display/camera support:

- LCDIF Display Controller:
  - Supports up to 2 layers of overlay
  - Support up to 1080p60 display through MIPI DSI
- MIPI Interface:
  - 4-lane MIPI CSI interface
  - 4-lane MIPI DSI interface
- CSI Interface:
  - CSI is a simple camera interface which is used to capture the MIPI CSI input and save the pixels into memory

5.1.14. Audio

Audio include the following:

- S/PDIF Input and Output, including a new Raw Capture input mode
- Five external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces, including one SAI with 8 TX and 8 RX lanes, one SAI with 4 TX and 4 RX lanes, two SAI with 2 TX and 2 RX lanes, and one SAI with 1 TX and 1 RX lanes. Supports over 20 channels of audio subject to I/O limitations.
- Four channels of PDM (Digital Microphone Interfaces)

5.1.15. General Connectivity Interfaces

The chip contains a rich set of general connectivity interfaces, including:

- One PCI Express (PCIe):
  - Single lane supporting PCIe Gen 2
  - Dual mode operation to function as root complex or endpoint
  - Integrated PHY interface
  - Supports L1 low power substate
- Two USB 2.0 OTG controllers with integrated PHY interface
  - Spread spectrum clock support
- Three Ultra Secure Digital Host Controller (uSDHC) interfaces
  - MMC 5.0 compliance with HS400 DDR signaling to support up to 400 MB/sec
  - SD/SDIO 3.01 compliance with 200 MHZ SDR signaling to support up to 100 MB/sec
  - Support for SDXC (extended capacity)
- One Gigabit Ethernet controller with support for EEE, Ethernet AVB and IEEE1588
- Four universal asynchronous receiver/transmitter (UART) modules
- Four I2C modules
- Three SPI modules

5.1.16. Security

Security functions are enabled and accelerated by the following hardware:

- RDC – Resource Domain Controller:
  - Supports 4 domains and up to 8 regions
- Arm TrustZone including the TZ architecture:
  - ARM Cortex-A53 MPCore TrustZone support
- On-chip RAM (OCRAM) secure region protection using OCRAM controller
- High Assurance Boot (HAB)
- Cryptographic Acceleration and Assurance Module (CAAM)
  - Support Widevine and PlayReady content protection
  - Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC)
  - algorithms
  - Real-time integrity checker (RTIC)
  - DRM support for RSA, AES, 3DES, DES
  - Side channel attack resistance
  - True random number generation (RNG)
  - Manufacturing protection support
- Secure Non-Volatile Storage (SNVS), including
  - Secure Real Time Clock (RTC)
- Secure JTAG Controller (SJC)

5.1.17. Multicore Support

Multicore support contains:

- Resource domain controller (RDC) to support isolation and safe sharing of system resources
- Messaging unit (MU)
- Hardware Semaphore (SEMA42)
- Shared bus topology

5.1.18. GPIO and Pin Multiplexing

- General-purpose input/output (GPIO) modules with interrupt capability
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control

5.1.19. Power Management

The power management unit consists of:

- Temperature sensor with programmable trip points
- Flexible power domain partitioning with internal power switches to support efficient power management

5.1.20. System Debug

The system debug features are:

- ARM CoreSight debug and trace architecture
- Trace Port Interface Unit (TPIU) to support off-chip real-time trace
- Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
- Unified trace capability for Quad Cortex-A53 and Cortex-M4 CPUs
- Cross-Triggering Interface (CTI)
- Support for 5-pin (JTAG) debug interfaces

5.1.21. Degradation of internal IO pullup/pulldown current capability

According to latest NXP Errata ERR050080 there is a degradation of the internal IO pullup/pulldown capability when the IO pads are continuously driven in the opposite logic level.

For example, when internal pullup is enabled with external logic driving the pin low, and a 3.3V operating condition which limits the pads pullup/pulldown ability.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB, and MIPI PHY IO's.

The suggested workaround is to use external resistors for the pullup/pulldown and disable the internal pullup/pulldown via software on pins that operate at 3.3V and the circuit requires pullup or pulldown

5.2. Memory

5.2.1. RAM

The DART-MX8M-MINI is available with up to 4 GB of LPDDR4 memory capable of running up to 3000MTS.

5.2.2. Non-volatile Storage Memory

The DART-MX8M-MINI is available with a non-volatile storage memory with optional densities. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.
The DART-MX8M-MINI can arrive with up to 128GB MLC eMMC or NAND with density up to 512MB.

5.3. Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- 1 fully differential mic / line input per stereo channel

- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4. Wi-Fi + BT (LWB5™)

The DART-MX8M-MINI contains LSR's pre-certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 5.2 wireless connectivity.

The DART-MX8M-MINI module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

Key Features:

- IEEE 802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, and BLE 5.2
- U.F.L connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)

5.5. PMIC

The DART-MX8M-MINI features ROHM PN:BD71847MWV as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX8M-MINI series of application processors. The PMIC regulates all power rails required on SOM from a single power supply with 3.5V – 5V range.
The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

5.6. 10/100/1000 Mbps Ethernet Transceiver

The SOM can be ordered with an Integrated Ethernet Transceiver,
Qualcomm Atheros AR8033 or Analog Devices ADIN1300.
Please contact sales@variscite.com for inquiries about P/N assembled on your SOM.

5.6.1. Qualcomm Atheros AR8033 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- 1000BASE-T PCS and auto-negotiation with next page support
- Green ETHOS power saving modes with internal automatic DSP power saving scheme
- IEEE 802.3az EEE
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Robust operation over up to 140 meters of CAT5 cable
- Automatic Channel Swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction ν IEEE 802.3u compliant auto-negotiation
- Jumbo frame supports up to 10 KB (full-duplex)
- Integrated termination circuitry at the line side

5.6.2. Analog Devices ADIN1300 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.
- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover
- Autonegotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

5.7. MIPI-DSI to Dual Channel LVDS Bridge (SN65DSI84)

The DART-MX8M-MINI features TI SN65DIS84 MIPI-DSI Bridge to FLATLINK LVDS display.

The SN65DSI84 DSI to FlatLink™ bridge features a single-channel MIPI® D-PHY receiver front-end configuration with 4 lanes per channel operating at 1 Gbps per lane. The bridge decodes MIPI® DSI 18bpp RGB666 and 24 bpp RGB888 packets and converts the formatted video data stream to a FlatLink™ compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Dual-Link LVDS, Single-Link LVDS interface with four data lanes per link.
The SN65DSI84 is well suited for WUXGA 1920 x1200 at 60 frames per second, with up to 24 bits-per- pixel. Partial line buffering is implemented to accommodate the data stream mismatch between the DSI and LVDS interfaces.
Designed with industry compliant interface technology, the SN65DSI84 is compatible with a wide range of micro-processors and is designed with a range of power management features including low running swing LVDS outputs, and the MIPI® defined ultra-low power state (ULPS) support.

5.8. EEPROM

The SOM uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters. This EEPROM is connected to I2C1 bus and intended only for holding the above information. The SOM may not boot if the contents of EEPROM device are corrupted.

6. DART-MX8M-MINI Hardware Configuration

DART-MX8M-MINI hardware interfaces, explained on sections 5.3, 5.4, Error! Reference source not found. and 5.7, configured using the orderable part number of the module.

For every hardware configuration option, the SOM pinout will be affected, see section 7.3 for complete list.

Table 1 details part of the hardware configuration orderable options.

Table 1: Partial Hardware Configuration Options

OPTION	DESCRIPTION
EC	**E**thernet **C**ontroller PHY assembled on SOM
AC	**A**udio **C**odec assembled on SOM
WBD	**W**i-Fi **B**luetooth (BT/BLE) **D**ual band - combo assembled on SOM
LD	**L**VDS **D**isplay bridge assembled on SOM
0xG	**NAND** Configuration size: Currently 05G (512MB)– **Not released Yet!**
xG	**eMMC** Configuration size: 8G/16G/32G/64G/128G (8/16/32/64/128 GB)
CT **IT**	Temperature grade: **CT** - Commercial Grade **IT** – Industrial Grade

NOTE

Other orderable options are available and are not part of this datasheet.
Please *Contact Information* for complete list of configuration options.

7. External Connectors

7.1. Board to Board Connector

- The DART-MX8M-MINI exposes three 90-pin board-to-board connectors.
- The recommended mating connector is: **Hirose Electric Co Ltd PN: DF40C-90DS-0.4V(51)**

7.2. Wi-Fi & BT Connector

- Modules with Wi-Fi ***"WBD" Configuration*** **-** a combined Wi-Fi + BT antenna connector is assembled
- Connector type: **U.FL JACK connector**
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3. DART-MX8M-MINI Connector Pin-out

Tables under this section lists the SOM connectors pinout with each pin listed for all the available ball names related to the assembly hardware configuration options.

Table 2: PIN-OUT Tables Mnemonics

Column Heading		Meaning
PIN#	**Jx.YY**	Pin number on a connector: Jx : Can be J1 J2 or J3 YY : Can be 1 to 90
ASSY		Can be any of the **options listed in Table 1**. **"NO"** - will be added to above option - means the option is not part of the SOM part number. **Blank** - pin listed have no hardware configuration option **NC** - Pin is Not Connected
BALL NAME		Name of the ball for the specific ASSY option
GPIO	**GPIOx_y**	SOC pin GPIO Alternate function number including: **x- GPIO bank** **y-Bit number in the bank**
NOTES		This column displays any special note related to the specific pin with the specific ASSY The notes will repeat also in the function tables.
BALL		Source device and it's pin number.
	XX.YY	XX: Source Chip can be: SOC.yy – pins connected to the iMX8M SoC AR8033.yy / ADIN1300.yy – pins connected the Ethernet Controller (***"EC" Configuration***) WM8904.yy - pins connected the Audio Codec (***"AC" Configuration***) SN65DSI84.yy - pins connected the LVDS Display bridge (***"LD" Configuration***) YY : Pin/Ball number of source chip.

NOTE

A. Some pins may appear in several consecutive lines if additional chip function used on SOM; Relates to the DART-MX8M-MINI orderable hardware configuration.

B. In case a chip is added due to an orderable configuration the chip function must be used.

7.3.1. DART-MX8M-MINI J1 Pin-out

Table 3: J1 PIN-OUT

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J1.1		GPIO1_IO00	GPIO1_IO00		SOC.AG14
J1.2	NO EC	ENET_TD1	GPIO1_IO20	Powered by NVCC_ENET pin	SOC.AF26
J1.2	EC	ETH_TRX1_P		Signal source is Ethernet PHY.	AR8033.14/ ADIN1300.14
J1.3	NO EC	ENET_TX_CTL	GPIO1_IO22	Powered by NVCC_ENET pin	SOC.AF24
J1.3	EC	ETH_NC		With EC configuration this pin in Not Connected.	NC
J1.4	NO EC	ENET_TD0	GPIO1_IO21	Powered by NVCC_ENET pin	SOC.AG26
J1.4	EC	ETH_TRX1_N		Signal source is Ethernet PHY.	AR8033.15/ ADIN1300.15
J1.5	NO EC	ENET_TXC	GPIO1_IO23	Powered by NVCC_ENET pin	SOC.AG24
J1.5	EC	ETH_LED_LINK10_100		Signal source is Ethernet PHY.	AR8033.26/ ADIN1300 - GND
J1.6	NO EC	ENET_TD2	GPIO1_IO19	Powered by NVCC_ENET pin	SOC.AG25
J1.6	EC	ETH_TRX0_N		Signal source is Ethernet PHY.	AR8033.12/ ADIN1300.13
J1.7	NO EC	ENET_RXC	GPIO1_IO25	Powered by NVCC_ENET pin	SOC.AE26
J1.7	EC	ETH_LED_LINK1000		Signal source is Ethernet PHY.	AR8033.24/ ADIN1300.26 (via level shifter)
J1.8	NO EC	ENET_TD3	GPIO1_IO18	Powered by NVCC_ENET pin	SOC.AF25
J1.8	EC	ETH_TRX0_P		Signal source is Ethernet PHY.	AR8033.11/ ADIN1300.12
J1.9	NO EC	ENET_RX_CTL	GPIO1_IO24	Powered by NVCC_ENET pin	SOC.AF27
J1.9	EC	ETH_LED_ACT		Signal source is Ethernet PHY.	AR8033.23/ ADIN1300.21 via inv. FET
J1.10	NO EC	ENET_RD0	GPIO1_IO26	Powered by NVCC_ENET pin	SOC.AE27
J1.10	EC	ETH_TRX2_P		Signal source is Ethernet PHY.	AR8033.17/ ADIN1300.16
J1.11		ENET_MDIO	GPIO1_IO17	Shared on SOM with "EC"; Includes PU to NVCC_ENET with "EC" Only;	SOC.AB27
J1.12	NO EC	ENET_RD1	GPIO1_IO27	Powered by NVCC_ENET pin	SOC.AD27
J1.12	EC	ETH_TRX2_N		Signal source is Ethernet PHY.	AR8033.18/ ADIN1300.17
J1.13		ENET_MDC	GPIO1_IO16	Shared on SOM with "EC"; powered by NVCC_ENET.	SOC.AC27
J1.14	NO EC	ENET_RD2	GPIO1_IO28	Powered by NVCC_ENET pin	SOC.AD26
J1.14	EC	ETH_TRX3_P		Signal source is Ethernet PHY.	AR8033.20/ ADIN1300.18
J1.15		NVCC_SNVS_1V8			NVCC_SNVS_1V8
J1.16	NO EC	ENET_RD3	GPIO1_IO29	Powered by NVCC_ENET pin	SOC.AC26
J1.16	EC	ETH_TRX3_N		Signal source is Ethernet PHY.	AR8033.21/ ADIN1300.19
J1.17		I2C4_SCL	GPIO5_IO20		SOC.D13
J1.18		GND		Digital Ground	GND
J1.19		I2C4_SDA	GPIO5_IO21		SOC.E13
J1.20		ONOFF		SOC input with internal PU	SOC.A25

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J1.21		GND		Digital Ground	GND
J1.22		PMIC_ON_REQ		SOC output (OD with PU) controls the PMIC state; Can be pulled externally to cause cold reset.	SOC.A24
J1.23	WBD	BT_HOST_WAKE		Output from the LWB5 module;	LWB5.46
J1.23	No WBD			With "No WBD" configuration this pin in Not Connected.	NC_NO_WBD
J1.24		POR_B		PMIC output (OD with PU) connected to SOC; Can be pulled low externally to cause hot reset	SOC.B24
J1.25	WBD	WIFI_HOST_WAKE		Output from the LWB5 module;	LWB5.17
J1.25	No WBD	NC		With "No WBD" configuration this pin in Not Connected.	NC
J1.26		PMIC_STBY_REQ		SOC output controls the PMIC state; Can be used externally to control carrier board power	SOC.E24
J1.27		NVCC_3V3		Power output from SOM; Rises after last power rail; Can be used to control base board power.	NVCC_3V3
J1.28		CONN_SD2_NRST	GPIO2_IO19	Can be used to control the SD card power in order to perform SD RESET function.	SOC.AB26
J1.29		SD1_DATA7	GPIO2_IO09_1V8	SD1_DATA7 can be used as GPIO2_IO09_1V8 connected to: BT or HOST wake signals of LWB5	SOC.W26
J1.30		GND		Digital Ground	GND
J1.31	EC	NVCC_ENET		ENET pins power: AR8033 PHY - 2.5V; ADIN1300 - 1.8V **Do not connect!**	SOC.W22
J1.31	No EC	NVCC_ENET		ENET pins power: **Must supply** - * RMII uses 1.8 or 3.3V. * RGMII uses 1.8 or 2.5V. * GPIO 1.8V/2.5V/3.3V	SOC.W22
J1.32	eMMC	NAND_DATA01	GPIO3_IO07_1V8	Run at 1.8V level!	SOC.K24
J1.32	NAND			DO NOT connect!	SOC.K24
J1.33		GND		Digital Ground	GND
J1.34	eMMC	NAND_CE0_B	GPIO3_IO01_1V8	Run at 1.8V level!	SOC.N24
J1.34	NAND			DO NOT connect!	SOC.N24
J1.35		CLKIN1_1V8			SOC.H27
J1.36		NC		Not Connected	NC
J1.37		CLKIN2_1V8			SOC.J27
J1.38	eMMC	NAND_DQS	GPIO3_IO14_1V8	Run at 1.8V level!	SOC.R22
J1.38	NAND			DO NOT connect!	SOC.R22
J1.39		NC		Not Connected	NC
J1.40	eMMC	NAND_ALE	GPIO3_IO00_1V8	Run at 1.8V level!	SOC.N22
J1.40	NAND			DO NOT connect!	SOC.N22
J1.41	No EC	GPIO1_IO07	GPIO1_IO07	DO NOT connect!	SOC.AF11
J1.41	EC			Used internally with "EC" (ETH_PHY_3V3_EN_B).	SOC.AF11

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J1.42		NC		Not Connected	NC
J1.43		NC		Not Connected	NC
J1.44		NC		Not Connected	NC
J1.45		CLKOUT1_1v8			SOC.H26
J1.46	eMMC	NAND_DATA03	GPIO3_IO09_1V8	Run at 1.8V level!	SOC.N23
J1.46	NAND			DO NOT connect!	SOC.N23
J1.47		CLKOUT2_1v8			SOC.J26
J1.48	eMMC	NAND_DATA00	GPIO3_IO06_1V8	Run at 1.8V level!	SOC.P23
J1.48	NAND			DO NOT connect!	SOC.P23
J1.49		GND		Digital Ground	GND
J1.50	eMMC	NAND_DATA02	GPIO3_IO08_1V8	Run at 1.8V level!	SOC.K23
J1.50	NAND			DO NOT connect!	SOC.K23
J1.51		PCIE1_REF_CLK_N			SOC.A21
J1.52		GND		Digital Ground	GND
J1.53		PCIE1_REF_CLK_P			SOC.B21
J1.54		NC		Not Connected	NC
J1.55		GND		Digital Ground	GND
J1.56		NC		Not Connected	NC
J1.57		PCIE1_TX_N			SOC.A20
J1.58		GND		Digital Ground	GND
J1.59		PCIE1_TX_P			SOC.B20
J1.60		PCIE1_RX_N			SOC.A19
J1.61		GND		Digital Ground	GND
J1.62		PCIE1_RX_P			SOC.B19
J1.63		NC		Not Connected	NC
J1.64		GND		Digital Ground	GND
J1.65		NC		Not Connected	NC
J1.66		NC		Not Connected	NC
J1.67		GND		Digital Ground	GND
J1.68		NC		Not Connected	NC
J1.69		MIPI_CSI1_D3_P			SOC.B18
J1.70		GND		Digital Ground	GND
J1.71		MIPI_CSI1_D3_N			SOC.A18
J1.72		NC		Not Connected	NC
J1.73		MIPI_CSI1_D1_P			SOC.B15
J1.74		SD2_CD_B	GPIO2_IO012		SOC.AA26
J1.75		MIPI_CSI1_D1_N			SOC.A15
J1.76		GND		Digital Ground	GND
J1.77		MIPI_CSI1_D2_N			SOC.A17
J1.78		SD2_DATA2	GPIO2_IO17		SOC.V24
J1.79		MIPI_CSI1_D2_P			SOC.B17
J1.80		SD2_DATA1	GPIO2_IO16		SOC.AB24
J1.81		MIPI_CSI1_D0_P			SOC.B14

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J1.82		SD2_CLK	GPIO2_IO13		SOC.W23
J1.83		MIPI_CSI1_D0_N			SOC.A14
J1.84		SD2_DATA3	GPIO2_IO18		SOC.V23
J1.85		GND		Digital Ground	GND
J1.86		SD2_DATA0	GPIO2_IO15		SOC.AB23
J1.87		MIPI_CSI1_CLK_P			SOC.B16
J1.88		SD2_CMD	GPIO2_IO14	Includes 2.4K PU on SOM	SOC.W24
J1.89		MIPI_CSI1_CLK_N			SOC.A16
J1.90		NVCC_SD2_1V8_3V3		Power output from SOM; Power the SD2 interface pins; Will change 1.8V/3.3V according to SD capabilities.	NVCC_SD2_1V8_3V3

7.3.2. DART-MX8M-MINI J2 Pin-out

Table 4: J2 PIN-OUT

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J2.1		JTAG_TCK		Need to include an external PD of 4.7K Ohm	SOC.F26
J2.2	NO AC	SAI3_RXD	GPIO4_IO30		SOC.AF7
J2.2	AC	HPLOUT		Signal source is Audio Codec.	WM8904.13
J2.3		JTAG_TMS			SOC.F27
J2.4	NO AC	SAI3_TXC	GPIO5_IO00		SOC.AG6
J2.4	AC	HPROUT		Signal source is Audio Codec.	WM8904.15
J2.5		JTAG_TRST_B			SOC.C27
J2.6	NO AC	SAI3_RXFS	GPIO4_IO28		SOC.AG8
J2.6	AC	HPOUTFB		Signal source is Audio Codec.	WM8904.14
J2.7		JTAG_TDI			SOC.E27
J2.8	NO AC	SAI3_RXC	GPIO4_IO29		SOC.AG7
J2.8	AC	LINEIN1_LP		Signal source is Audio Codec.	WM8904.26
J2.9		JTAG_TDO			SOC.E26
J2.10	NO AC	SAI3_TXFS	GPIO4_IO31		SOC.AC6
J2.10	AC	LINEIN1_RP		Signal source is Audio Codec.	WM8904.24
J2.11		BOOT_MODE1			SOC.G27
J2.12		AGND		Audio Ground	AGND
J2.13		BOOT_MODE0			SOC.G26
J2.14	NO AC	SAI3_TXD	GPIO5_IO01		SOC.AF6
J2.14	AC	DMIC_CLK		Signal source is external Digital Microphone.	WM8904.1
J2.15		NC		Not Connected	NC
J2.16	NO AC	SAI3_MCLK	GPIO5_IO02		SOC.AD6
J2.16	AC	DMIC_DATA_1V8		Signal source is external Digital Microphone. Signal level is 1.8V	WM8904.27
J2.17		NC		Not Connected	NC
J2.18		GND		Digital Ground	GND
J2.19		NC		Not Connected	NC
J2.20	WBD	ECSPI2_MOSI	GPIO5_IO11	Used internally with "WBD"; Function can be released if BT Buffer disabled.	SOC.B8
J2.20	No WBD	ECSPI2_MOSI	GPIO5_IO11		SOC.B8
J2.21		NC		Not Connected	NC
J2.22	WBD	ECSPI2_MISO	GPIO5_IO12	Used internally with "WBD"; Function can be released if BT Buffer disabled.	SOC.A8
J2.22	No WBD	ECSPI2_MISO	GPIO5_IO12		SOC.A8
J2.23		GND		Digital Ground	GND
J2.24	WBD	ECSPI2_SCLK	GPIO5_IO10	Used internally with "WBD"; Function can be released if BT Buffer disabled.	SOC.E6
J2.24	No WBD	ECSPI2_SCLK	GPIO5_IO10		SOC.E6
J2.25		NC		Not Connected	NC
J2.26	WBD	ECSPI2_SS0	GPIO5_IO13	Used internally with "WBD"; Function can be released if BT Buffer disabled.	SOC.A6
J2.26	No WBD	ECSPI2_SS0	GPIO5_IO13		SOC.A6

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J2.27		NC		Not Connected	NC
J2.28		GPIO1_IO02	GPIO1_IO02		SOC.AG13
J2.29		NC		Not Connected	NC
J2.30		I2C2_SDA	GPIO5_IO17		SOC.D9
J2.31		NC		Not Connected	NC
J2.32		I2C2_SCL	GPIO5_IO16		SOC.D10
J2.33		NC		Not Connected	NC
J2.34		SAI5_RXFS	GPIO3_IO19		SOC.AB15
J2.35		NC		Not Connected	NC
J2.36		SAI5_RXD0	GPIO3_IO21		SOC.AD18
J2.37		NC		Not Connected	NC
J2.38		SAI5_RXD2	GPIO3_IO23		SOC.AD13
J2.39		NC		Not Connected	NC
J2.40		SAI5_RXC	GPIO3_IO20		SOC.AC15
J2.41		NC		Not Connected	NC
J2.42		SAI5_RXD1	GPIO3_IO22		SOC.AC14
J2.43		NC		Not Connected	NC
J2.44		SAI5_RXD3	GPIO3_IO24		SOC.AC13
J2.45		NC		Not Connected	NC
J2.46		SAI5_MCLK	GPIO3_IO25		SOC.AD15
J2.47		GND		Digital Ground	GND
J2.48		SAI2_RXFS	GPIO4_IO21		SOC.AC19
J2.49		NC		Not Connected	NC
J2.50		SAI2_RXC	GPIO4_IO22		SOC.AB22
J2.51		NC		Not Connected	NC
J2.52		SAI2_TXFS	GPIO4_IO24		SOC.AD23
J2.53		GND		Digital Ground	GND
J2.54		SAI2_MCLK	GPIO4_IO27		SOC.AD19
J2.55		SAI1_RXFS	GPIO4_IO00		SOC.AG16
J2.56		SAI2_TXC	GPIO4_IO25		SOC.AD22
J2.57		SAI1_RXC	GPIO4_IO01		SOC.AF16
J2.58		SAI2_RXD0	GPIO4_IO23		SOC.AC24
J2.59		SAI1_RXD1	GPIO4_IO03	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF15
J2.60		SAI2_TXD0	GPIO4_IO26		SOC.AC22
J2.61		SAI1_RXD0	GPIO4_IO02	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG15
J2.62		SAI1_RXD3	GPIO4_IO05	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF17
J2.63		SAI1_RXD2	GPIO4_IO04	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG17
J2.64		SAI1_TXFS	GPIO4_IO10		SOC.AB19
J2.65		SAI1_RXD4	GPIO4_IO06	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG18

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J2.66		SAI1_RXD6	GPIO4_IO08	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG19
J2.67		SAI1_TXD1	GPIO4_IO13	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF20
J2.68		SAI1_RXD7	GPIO4_IO09	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF19
J2.69		SAI1_RXD5	GPIO4_IO07	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF18
J2.70		SAI1_TXD0	GPIO4_IO12	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG20
J2.71		SAI1_TXD5	GPIO4_IO17	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF22
J2.72		SAI1_TXC	GPIO4_IO11		SOC.AC18
J2.73		SAI1_TXD3	GPIO4_IO15	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF21
J2.74		SAI1_TXD4	GPIO4_IO16	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG22
J2.75		GND		Digital Ground	GND
J2.76		SAI1_TXD7	GPIO4_IO19	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF23
J2.77		ECSPI1_SCLK	GPIO5_IO06		SOC.D6
J2.78		SAI1_TXD2	GPIO4_IO14	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG21
J2.79		ECSPI1_SS0	GPIO5_IO09		SOC.B6
J2.80		SAI1_TXD6	GPIO4_IO18	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG23
J2.81		ECSPI1_MISO	GPIO5_IO08		SOC.A7
J2.82		SAI1_MCLK	GPIO4_IO20		SOC.AB18
J2.83		ECSPI1_MOSI	GPIO5_IO07		SOC.B7
J2.84		GND		Digital Ground	GND
J2.85		UART2_RXD	GPIO5_IO24		SOC.F15
J2.86		UART2_TXD	GPIO5_IO25		SOC.E15
J2.87		UART3_RXD	GPIO5_IO26		SOC.E18
J2.88		UART1_RXD	GPIO5_IO22		SOC.E14
J2.89		UART3_TXD	GPIO5_IO27		SOC.D18
J2.90		UART1_TXD	GPIO5_IO23		SOC.F13

[1] For boot configuration refer to section 76

7.3.3. DART-MX8M-MINI J3 Pin-out

Table 5: J3 PIN-OUT

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J3.1		UART4_TXD	GPIO5_IO29		SOC.F18
J3.2	LD	LVDS1_TX0_P		Signal source is LVDS Bridge.	SN65DSI84.C8
J3.2	No LD	NC		This pin is not connected with No "LD" configuration!	NC
J3.3		UART4_RXD	GPIO5_IO28		SOC.F19
J3.4	LD	LVDS1_TX0_N		Signal source is LVDS Bridge.	SN65DSI84.C9
J3.4	No LD	NC		This pin is not connected with No "LD" configuration!	NC
J3.5	LD	LVDS1_TX2_P		Signal source is LVDS Bridge.	SN65DSI84.E8
J3.5	No LD	NC		This pin is not connected with No "LD" configuration!	NC
J3.6	LD	LVDS1_TX1_P		Signal source is LVDS Bridge.	SN65DSI84.D8
J3.6	No LD	NC		This pin is not connected with No "LD" configuration!	NC
J3.7	LD	LVDS1_TX2_N		Signal source is LVDS Bridge.	SN65DSI84.E9
J3.7	No LD	NC		This pin is not connected with No "LD" configuration!	NC
J3.8	LD	LVDS1_TX1_N		Signal source is LVDS Bridge.	SN65DSI84.D9
J3.8	No LD	NC		This pin is not connected with No "LD" configuration!	NC
J3.9		GND		Digital Ground	GND
J3.10		GND		Digital Ground	GND
J3.11	LD	LVDS1_CLK_P		Signal source is LVDS Bridge.	SN65DSI84.F8
J3.11	No LD	NC		This pin is not connected with No "LD" configuration!	NC
J3.12	No LD	MIPI_DSI_TX0_P			SOC.B9
J3.12	LD	LVDS2_TX0_P		Signal source is LVDS Bridge.	SN65DSI84.B3
J3.13	LD	LVDS1_CLK_N		Signal source is LVDS Bridge.	SN65DSI84.F9
J3.13	No LD	NC		This pin is not connected with No "LD" configuration!	NC
J3.14	No LD	MIPI_DSI_TX0_N			SOC.A9
J3.14	LD	LVDS2_TX0_N		Signal source is LVDS Bridge.	SN65DSI84.A3
J3.15		GND		Digital Ground	GND
J3.16	No LD	MIPI_DSI_TX1_P			SOC.B10
J3.16	LD	LVDS2_TX1_P		Signal source is LVDS Bridge.	SN65DSI84.B4
J3.17	LD	LVDS1_TX3_P		Signal source is LVDS Bridge.	SN65DSI84.G8
J3.18	No LD	MIPI_DSI_TX1_N			SOC.A10
J3.18	LD	LVDS2_TX1_N		Signal source is LVDS Bridge.	SN65DSI84.A4
J3.19	LD	LVDS1_TX3_N		Signal source is LVDS Bridge.	SN65DSI84.G9
J3.19	No LD	NC		This pin is not connected with No "LD" configuration!	NC
J3.20	No LD	MIPI_DSI_TX3_P			SOC.B13
J3.20	LD	LVDS2_TX3_P		Signal source is LVDS Bridge.	SN65DSI84.B7
J3.21		GND		Digital Ground	GND
J3.22	No LD	MIPI_DSI_TX3_N			SOC.A13
J3.22	LD	LVDS2_TX3_N		Signal source is LVDS Bridge.	SN65DSI84.A7
J3.23	No LD	MIPI_DSI_TX2_P			SOC.B12
J3.23	LD	LVDS2_CLK_P		Signal source is LVDS Bridge.	SN65DSI84.B6
J3.24		GND		Digital Ground	GND
J3.25	No LD	MIPI_DSI_TX2_N			SOC.A12
J3.25	LD	LVDS2_CLK_N		Signal source is LVDS Bridge.	SN65DSI84.A6

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J3.26		USB2_VBUS		USB PHY power pin; 5V tolerant	SOC.F23
J3.27		GND		Digital Ground	GND
J3.28		SPDIF_RX	GPIO5_IO04		SOC.AG9
J3.29	No LD	MIPI_DSI_CLK_N			SOC.A11
J3.29	LD	LVDS2_TX2_N		Signal source is LVDS Bridge.	SN65DSI84.A5
J3.30		GPIO1_IO11	GPIO1_IO11		SOC.AC10
J3.31	No LD	MIPI_DSI_CLK_P			SOC.B11
J3.31	LD	LVDS2_TX2_P		Signal source is LVDS Bridge.	SN65DSI84.B5
J3.32	WBD	SPDIF_EXT_CLK	GPIO5_IO05	Used internally with "WBD" as (GPIO5_IO05) BT_BUF_EN_B; Set this pin HIGH to disable BT buffer in order to release BT UART pins.	SOC.AF8
J3.32	No WBD	SPDIF_EXT_CLK	GPIO5_IO05		SOC.AF8
J3.33		GND		Digital Ground	GND
J3.34		GND		Digital Ground	GND
J3.35		NC		Not Connected	NC
J3.36		SPDIF_TX	GPIO5_IO03		SOC.AF9
J3.37		NC		Not Connected	NC
J3.38		GPIO1_IO15	GPIO1_IO15		SOC.AB9
J3.39		GND		Digital Ground	GND
J3.40		GPIO1_IO13	GPIO1_IO13		SOC.AD9
J3.41		NC		Not Connected	NC
J3.42		I2C3_SDA	GPIO5_IO19	10K internal PU included; Shared with “AC”	SOC.F10
J3.43		NC		Not Connected	NC
J3.44		USB2_ID		USB PHY ID pin	SOC.D23
J3.45		GND		Digital Ground	GND
J3.46		I2C3_SCL	GPIO5_IO18	10K internal PU included; Shared with “AC”	SOC.E10
J3.47		USB2_D_P			SOC.B23
J3.48		GPIO1_IO14	GPIO1_IO14		SOC.AC9
J3.49		USB2_D_N			SOC.A23
J3.50		GPIO1_IO12	GPIO1_IO12		SOC.AB10
J3.51		GND		Digital Ground	GND
J3.52		GPIO1_IO10	GPIO1_IO10		SOC.AD10
J3.53		NC		Not Connected	NC
J3.54		GPIO1_IO03	GPIO1_IO03		SOC.AF13
J3.55		NC		Not Connected	NC
J3.56		USB1_ID		USB PHY ID pin	SOC.D22
J3.57		GND		Digital Ground	GND
J3.58		GPIO1_IO06	GPIO1_IO06		SOC.AG11
J3.59		NC		Not Connected	NC
J3.60		GPIO1_IO08	GPIO1_IO08		SOC.AG10
J3.61		NC		Not Connected	NC
J3.62		GPIO1_IO05	GPIO1_IO05		SOC.AF12
J3.63		GND		Digital Ground	GND

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J3.64		GPIO1_IO01	GPIO1_IO01		SOC.AF14
J3.65		USB1_D_P			SOC.B22
J3.66		USB1_VBUS		USB PHY power pin; 5V tolerant	SOC.F22
J3.67		USB1_D_N			SOC.A22
J3.68		GND		Digital Ground	GND
J3.69		NC		Not Connected	NC
J3.70		NC		Not Connected	NC
J3.71		VBAT		SOM Power	VBAT
J3.72		NC		Not Connected	NC
J3.73		VBAT		SOM Power	VBAT
J3.74		GND		Digital Ground	GND
J3.75		VBAT		SOM Power	VBAT
J3.76		NC		Not Connected	NC
J3.77		VBAT		SOM Power	VBAT
J3.78		NC		Not Connected	NC
J3.79		VBAT		SOM Power	VBAT
J3.80		NC		Not Connected	NC
J3.81		VBAT		SOM Power	VBAT
J3.82		NC		Not Connected	NC
J3.83		VBAT		SOM Power	VBAT
J3.84		NC		Not Connected	NC
J3.85		VBAT		SOM Power	VBAT
J3.86		NC		Not Connected	NC
J3.87		VBAT		SOM Power	VBAT
J3.88		NC		Not Connected	NC
J3.89		VBAT		SOM Power	VBAT
J3.90		NC		Not Connected	NC

7.4. DART-MX8M-MINI Pin-Mux

This section tables lists the SOM connectors with the available functions on each pin.

Table 6: DART-MX8M-MINI_J1 PINMUX

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J1.1		SOC.AG14	GPIO1_IO00	ENET_PHY_REF_ CLK_ROOT_OUT				REF_CLK_32K	EXT_CLK1
J1.2	No EC	SOC.AF26	ENET_TD1					GPIO1_IO20	
J1.3	No EC	SOC.AF24	ENET_TX_CTL					GPIO1_IO22	
J1.4	No EC	SOC.AG26	ENET_TD0					GPIO1_IO21	
J1.5	No EC	SOC.AG24	ENET_TXC	ENET_TX_ER				GPIO1_IO23	
J1.6	No EC	SOC.AG25	ENET_TD2	IN=ENET_TX_CLK OUT=ENET_REF_CLK_ROOT				GPIO1_IO19	
J1.7	No EC	SOC.AE26	ENET_RXC	ENET_RX_ER				GPIO1_IO25	
J1.8	No EC	SOC.AF25	ENET_TD3					GPIO1_IO18	
J1.9	No EC	SOC.AF27	ENET_RX_CTL					GPIO1_IO24	
J1.10	No EC	SOC.AE27	ENET_RD0					GPIO1_IO26	
J1.11		SOC.AB27	ENET_MDIO					GPIO1_IO17	
J1.12	No EC	SOC.AD27	ENET_RD1					GPIO1_IO27	
J1.13		SOC.AC27	ENET_MDC					GPIO1_IO16	
J1.14	No EC	SOC.AD26	ENET_RD2					GPIO1_IO28	
J1.16	No EC	SOC.AC26	ENET_RD3					GPIO1_IO29	
J1.17		SOC.D13	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B			GPIO5_IO20	
J1.19		SOC.E13	I2C4_SDA	PWM1_OUT				GPIO5_IO21	
J1.28		SOC.AB26	SD2_RESET_B					GPIO2_IO19	
J1.29		SOC.W26						GPIO2_IO09_1V8	
J1.32	eMMC	SOC.K24		QSPIA_DATA1_1V8				GPIO3_IO07_1V8	
J1.34	eMMC	SOC.N24		QSPIA_SS0_B_1V8				GPIO3_IO01_1V8	
J1.38	eMMC	SOC.R22		QSPIA_DQS_1V8				GPIO3_IO14_1V8	
J1.40	eMMC	SOC.N22		QSPIA_SCLK_1V8				GPIO3_IO00_1V8	
J1.41		SOC.AF11	GPIO1_IO07	ENET_MDIO					EXT_CLK4
J1.46	eMMC	SOC.N23		QSPIA_DATA3_1V8				GPIO3_IO09_1V8	
J1.48	eMMC	SOC.P23		QSPIA_DATA0_1V8				GPIO3_IO06_1V8	

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J1.50	eMMC	SOC.K23		QSPIA_DATA2_1V8				GPIO3_IO08_1V8	
J1.74		SOC.AA26	SD2_CD_B					GPIO2_IO012	
J1.78		SOC.V24	SD2_DATA2					GPIO2_IO17	
J1.80		SOC.AB24	SD2_DATA1					GPIO2_IO16	
J1.82		SOC.W23	SD2_CLK					GPIO2_IO13	
J1.84		SOC.V23	SD2_DATA3					GPIO2_IO18	
J1.86		SOC.AB23	SD2_DATA0					GPIO2_IO15	
J1.88		SOC.W24	SD2_CMD					GPIO2_IO14	

Table 7: DART-MX8M-MINI_J2 PINMUX

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J2.2	No AC	SOC.AF7	SAI3_RXD	GPT1_COMPARE1	SAI5_RXD0		UART2_RTS_B	GPIO4_IO30	
J2.4	No AC	SOC.AG6	SAI3_TXC	GPT1_COMPARE2	SAI5_RXD2		UART2_TXD	GPIO5_IO00	
J2.6	No AC	SOC.AG8	SAI3_RXFS	GPT1_CAPTURE1	SAI5_RXFS	SAI3_RXD1		GPIO4_IO28	
J2.8	No AC	SOC.AG7	SAI3_RXC	GPT1_CLK	SAI5_RXC		UART2_CTS_B	GPIO4_IO29	
J2.10	No AC	SOC.AC6	SAI3_TXFS	GPT1_CAPTURE2	SAI5_RXD1	SAI3_TXD1	UART2_RXD	GPIO4_IO31	
J2.14	No AC	SOC.AF6	SAI3_TXD	GPT1_COMPARE3	SAI5_RXD3			GPIO5_IO01	
J2.16	No AC	SOC.AD6	SAI3_MCLK	PWM4_OUT	SAI5_MCLK			GPIO5_IO02	
J2.20		SOC.B8	ECSPI2_MOSI	UART4_TXD				GPIO5_IO11	
J2.22		SOC.A8	ECSPI2_MISO	UART4_CTS_B				GPIO5_IO12	
J2.24		SOC.E6	ECSPI2_SCLK	UART4_RXD				GPIO5_IO10	
J2.26		SOC.A6	ECSPI2_SS0	UART4_RTS_B				GPIO5_IO13	
J2.28		SOC.AG13	GPIO1_IO02	WDOG_B				WDOG_ANY	
J2.30		SOC.D9	I2C2_SDA	ENET_1588_EVENT1_OUT				GPIO5_IO17	
J2.32		SOC.D10	I2C2_SCL	ENET_1588_EVENT1_IN				GPIO5_IO16	
J2.34		SOC.AB15	SAI5_RXFS	SAI1_TXD0				GPIO3_IO19	
J2.36		SOC.AD18	SAI5_RXD0	SAI1_TXD2			PDM_BIT0	GPIO3_IO21	
J2.38		SOC.AD13	SAI5_RXD2	SAI1_TXD4	SAI1_TXFS	SAI5_TXC	PDM_BIT2	GPIO3_IO23	
J2.40		SOC.AC15	SAI5_RXC	SAI1_TXD1			PDM_CLK	GPIO3_IO20	
J2.42		SOC.AC14	SAI5_RXD1	SAI1_TXD3	SAI1_TXFS	SAI5_TXFS	PDM_BIT1	GPIO3_IO22	
J2.44		SOC.AC13	SAI5_RXD3	SAI1_TXD5	SAI1_TXFS	SAI5_TXD0	PDM_BIT3	GPIO3_IO24	
J2.46		SOC.AD15	SAI5_MCLK	SAI1_TXC				GPIO3_IO25	
J2.48		SOC.AC19	SAI2_RXFS	SAI5_TXFS	SAI5_TXD1	SAI2_RXD1	UART1_TXD	GPIO4_IO21	
J2.50		SOC.AB22	SAI2_RXC	SAI5_TXC			UART1_RXD	GPIO4_IO22	
J2.52		SOC.AD23	SAI2_TXFS	SAI5_TXD1		SAI2_TXD1	UART1_CTS_B	GPIO4_IO24	
J2.54		SOC.AD19	SAI2_MCLK	SAI5_MCLK				GPIO4_IO27	
J2.55		SOC.AG16	SAI1_RXFS	SAI5_RXFS				GPIO4_IO00	
J2.56		SOC.AD22	SAI2_TXC	SAI5_TXD2				GPIO4_IO25	
J2.57		SOC.AF16	SAI1_RXC	SAI5_RXC				GPIO4_IO01	
J2.58		SOC.AC24	SAI2_RXD0	SAI5_TXD0			UART1_RTS_B	GPIO4_IO23	
J2.59		SOC.AF15	SAI1_RXD1	SAI5_RXD1		PDM_BIT1		GPIO4_IO03	BOOT_CFG01
J2.60		SOC.AC22	SAI2_TXD0	SAI5_TXD3				GPIO4_IO26	
J2.61		SOC.AG15	SAI1_RXD0	SAI5_RXD0	SAI1_TXD1	PDM_BIT0		GPIO4_IO02	BOOT_CFG00

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J2.62		SOC.AF17	SAI1_RXD3	SAI5_RXD3		PDM_BIT3		GPIO4_IO05	BOOT_CFG03
J2.63		SOC.AG17	SAI1_RXD2	SAI5_RXD2		PDM_BIT2		GPIO4_IO04	BOOT_CFG02
J2.64		SOC.AB19	SAI1_TXFS	SAI5_TXFS				GPIO4_IO10	
J2.65		SOC.AG18	SAI1_RXD4	SAI6_TXC	SAI6_RXC			GPIO4_IO06	BOOT_CFG04
J2.66		SOC.AG19	SAI1_RXD6	SAI6_TXFS	SAI6_RXFS			GPIO4_IO08	BOOT_CFG06
J2.67		SOC.AF20	SAI1_TXD1	SAI5_TXD1				GPIO4_IO13	BOOT_CFG09
J2.68		SOC.AF19	SAI1_RXD7	SAI6_MCLK	SAI1_TXFS	SAI1_TXD4		GPIO4_IO09	BOOT_CFG07
J2.69		SOC.AF18	SAI1_RXD5	SAI6_TXD0	SAI6_RXD0	SAI1_RXFS		GPIO4_IO07	BOOT_CFG05
J2.70		SOC.AG20	SAI1_TXD0	SAI5_TXD0				GPIO4_IO12	BOOT_CFG08
J2.71		SOC.AF22	SAI1_TXD5	SAI6_RXD0	SAI6_TXD0			GPIO4_IO17	BOOT_CFG13
J2.72		SOC.AC18	SAI1_TXC	SAI5_TXC				GPIO4_IO11	
J2.73		SOC.AF21	SAI1_TXD3	SAI5_TXD3				GPIO4_IO15	BOOT_CFG11
J2.74		SOC.AG22	SAI1_TXD4	SAI6_RXC	SAI6_TXC			GPIO4_IO16	BOOT_CFG12
J2.76		SOC.AF23	SAI1_TXD7	SAI6_MCLK		PDM_CLK		GPIO4_IO19	BOOT_CFG15
J2.77		SOC.D6	ECSPI1_SCLK	UART3_RXD				GPIO5_IO06	
J2.78		SOC.AG21	SAI1_TXD2	SAI5_TXD2				GPIO4_IO14	BOOT_CFG10
J2.79		SOC.B6	ECSPI1_SS0	UART3_RTS_B				GPIO5_IO09	
J2.80		SOC.AG23	SAI1_TXD6	SAI6_RXFS	SAI6_TXFS			GPIO4_IO18	BOOT_CFG14
J2.81		SOC.A7	ECSPI1_MISO	UART3_CTS_B				GPIO5_IO08	
J2.82		SOC.AB18	SAI1_MCLK	SAI5_MCLK	SAI1_TXC	PDM_CLK		GPIO4_IO20	
J2.83		SOC.B7	ECSPI1_MOSI	UART3_TXD				GPIO5_IO07	
J2.85		SOC.F15	UART2_RXD	ECSPI3_MISO				GPIO5_IO24	
J2.86		SOC.E15	UART2_TXD	ECSPI3_SS0				GPIO5_IO25	
J2.87		SOC.E18	UART3_RXD	UART1_CTS_B				GPIO5_IO26	
J2.88		SOC.E14	UART1_RXD	ECSPI3_SCLK				GPIO5_IO22	
J2.89		SOC.D18	UART3_TXD	UART1_RTS_B				GPIO5_IO27	
J2.90		SOC.F13	UART1_TXD	ECSPI3_MOSI				GPIO5_IO23	

Table 8: DART-MX8M-MINI_J3 PINMUX

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J3.1		SOC.F18	UART4_TXD	UART2_RTS_B				GPIO5_IO29	
J3.3		SOC.F19	UART4_RXD	UART2_CTS_B	PCIE1_CLKREQ_B			GPIO5_IO28	
J3.28		SOC.AG9	SPDIF_RX	PWM2_OUT				GPIO5_IO04	
J3.30		SOC.AC10	GPIO1_IO11	USB2_OTG_ID					
J3.32		SOC.AF8	SPDIF_EXT_CLK	PWM1_OUT				GPIO5_IO05	
J3.36		SOC.AF9	SPDIF_TX	PWM3_OUT				GPIO5_IO03	
J3.38		SOC.AB9	GPIO1_IO15	USB2_OTG_OC				PWM4_OUT	CLKO2
J3.40		SOC.AD9	GPIO1_IO13	USB1_OTG_OC				PWM2_OUT	
J3.42		SOC.F10	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO19	
J3.46		SOC.E10	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO18	
J3.48		SOC.AC9	GPIO1_IO14	USB2_OTG_PWR				PWM3_OUT	CLKO1
J3.50		SOC.AB10	GPIO1_IO12	USB1_OTG_PWR					
J3.52		SOC.AD10	GPIO1_IO10	USB1_OTG_ID					
J3.54		SOC.AF13	GPIO1_IO03	USDHC1_VSELECT					
J3.58		SOC.AG11	GPIO1_IO06	ENET_MDC				SD1_CD_B	EXT_CLK3
J3.60		SOC.AG10	GPIO1_IO08	ENET_1588_EVENT0_IN				SD2_RESET_B	
J3.62		SOC.AF12	GPIO1_IO05	M4_NMI				PMIC_READY	
J3.64		SOC.AF14	GPIO1_IO01	PWM1_OUT				REF_CLK_24M	EXT_CLK2

8. SOM's interfaces

Acronym used in the tables listed under this section:

Table 9: Interface Tables Mnemonics

Column Heading		Meaning
PIN#	**Jx.YY**	Pin number on a connector: Jx: Can be J1 J2 or J3 YY: Can be 1 to 90
ALT NAME		Pin type & direction
ALT#		Alternate number for the function. Blank in case the function origin is a PHY pin.
NOTES		This column displays any special note related to the specific pin with the specific ASSY.
BALL	**XX.YY**	Source device and its pin number; See Table 2.

Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 10: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
PCIe TX/RX data pairs	85 Ω Differential
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, PCIe clocks, MIPI (CSI and DSI), LVDS lines	100 Ω Differential

8.1. Display Interfaces

The DART-MX8M-MINI consists of the following display interfaces options:

- MIPI DSI – **No *"LD" Configuration***
  - MIPI-DSI standard v1.1 support resolution up to 1920x1080p60.
  - Up to 4 data lanes support D-PHY
  - 80Mbps - 1.5Gbps data rate in high speed operation
  - 10Mbps data rate in low power operation
  - Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
  - Supports High Speed and Low Power operation
  - Host Version
- LVDS - ***"LD" Configuration***
  - Implemented using SN65DSI84 (see section 5.7)
  - Single channel DSI to Single-Link or Dual-Link LVDS
  - Resolution up to 1920x1200 60 fps at 24 bpp/18 bpp, but limited by the DSI interface to 1920x1080.
  - DSI Channel has 4 DSI data lanes + 1 CLK lane.
  - Each LVDS link has 4 data lanes + 1 CLK lane.

8.1.1. MIPI-DSI Signals

The MIPI-DSI signals share the same pins as the LVDS channel 2 function depending on the orderable configuration option.

Table 11: MIPI-DSI Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J3.29	No LD	MIPI_DSI_CLK_N		Differential Pair Negative side	SOC.A11
J3.31	No LD	MIPI_DSI_CLK_P		Differential Pair Positive side	SOC.B11
J3.14	No LD	MIPI_DSI_TX0_N		Differential Pair Negative side	SOC.A9
J3.12	No LD	MIPI_DSI_TX0_P		Differential Pair Positive side	SOC.B9
J3.18	No LD	MIPI_DSI_TX1_N		Differential Pair Negative side	SOC.A10
J3.16	No LD	MIPI_DSI_TX1_P		Differential Pair Positive side	SOC.B10
J3.25	No LD	MIPI_DSI_TX2_N		Differential Pair Negative side	SOC.A12
J3.23	No LD	MIPI_DSI_TX2_P		Differential Pair Positive side	SOC.B12
J3.22	No LD	MIPI_DSI_TX3_N		Differential Pair Negative side	SOC.A13
J3.20	No LD	MIPI_DSI_TX3_P		Differential Pair Positive side	SOC.B13

8.1.2. LVDS Display Signals

The LVDS display output support includes two channels generated by the driving IC, see section 5.7.

Sections 8.1.2.1 and 0 lists the interface pins and signal description.

8.1.2.1. LVDS Display Signals Channel 1

Table 12: LVDS Display Channel 1 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J3.13	LD	LVDS1_CLK_N		Signal source is LVDS Bridge. Differential Pair Negative side	SN65DSI84.F9
J3.11	LD	LVDS1_CLK_P		Signal source is LVDS Bridge. Differential Pair Positive side	SN65DSI84.F8
J3.4	LD	LVDS1_TX0_N		Signal source is LVDS Bridge. Differential Pair Negative side	SN65DSI84.C9
J3.2	LD	LVDS1_TX0_P		Signal source is LVDS Bridge. Differential Pair Positive side	SN65DSI84.C8
J3.8	LD	LVDS1_TX1_N		Signal source is LVDS Bridge. Differential Pair Negative side	SN65DSI84.D9
J3.6	LD	LVDS1_TX1_P		Signal source is LVDS Bridge. Differential Pair Positive side	SN65DSI84.D8
J3.7	LD	LVDS1_TX2_N		Signal source is LVDS Bridge. Differential Pair Negative side	SN65DSI84.E9
J3.5	LD	LVDS1_TX2_P		Signal source is LVDS Bridge. Differential Pair Positive side	SN65DSI84.E8
J3.19	LD	LVDS1_TX3_N		Signal source is LVDS Bridge. Differential Pair Negative side	SN65DSI84.G9
J3.17	LD	LVDS1_TX3_P		Signal source is LVDS Bridge. Differential Pair Positive side	SN65DSI84.G8

8.1.2.2. LVDS Display Signals Channel 2

Table 13: LVDS Display Channel 2 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J3.25	LD	LVDS2_CLK_N		Signal source is LVDS Bridge. Differential Pair Negative side	SN65DSI84.A6
J3.23	LD	LVDS2_CLK_P		Signal source is LVDS Bridge. Differential Pair Positive side	SN65DSI84.B6
J3.14	LD	LVDS2_TX0_N		Signal source is LVDS Bridge. Differential Pair Negative side	SN65DSI84.A3
J3.12	LD	LVDS2_TX0_P		Signal source is LVDS Bridge. Differential Pair Positive side	SN65DSI84.B3
J3.18	LD	LVDS2_TX1_N		Signal source is LVDS Bridge. Differential Pair Negative side	SN65DSI84.A4
J3.16	LD	LVDS2_TX1_P		Signal source is LVDS Bridge. Differential Pair Positive side	SN65DSI84.B4
J3.29	LD	LVDS2_TX2_N		Signal source is LVDS Bridge. Differential Pair Negative side	SN65DSI84.A5
J3.31	LD	LVDS2_TX2_P		Signal source is LVDS Bridge. Differential Pair Positive side	SN65DSI84.B5
J3.22	LD	LVDS2_TX3_N		Signal source is LVDS Bridge. Differential Pair Negative side	SN65DSI84.A7
J3.20	LD	LVDS2_TX3_P		Signal source is LVDS Bridge. Differential Pair Positive side	SN65DSI84.B7

NOTE

When the ***"LD" configuration*** NOT chosen, the LVDS Channel 2 pins exposes the MIPI-DSI on the DART-MX8M-MINI connector.

8.2. Camera Interface

8.2.1. MIPI Camera Serial Interface

The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

Key features include:

- Module provides one four-lane MIPI camera serial interfaces
- MIPI D-PHY specification V1.2 (Board Approved)
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature (Board Approved)
- Support primary and secondary Image format
    - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
    - RGB565, RGB666, RGB888
    - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
    - All of User defined Byte-based Data packet
- Support up to 4 lanes of D-PHY, which operates up to a maximum bit rate of 1.5 Gbps.
- Interfaces
    - Compatible to PPI (Protocol-to-PHY Interface) in MIPI D-PHY Specification
    - AMBA3.0 APB Slave for Register configuration.
    - Image output data bus width: 32 bits
- Image memory
    - Size of SRAM is 4KB
- Pixel clock can be gated when no PPI data is coming

8.2.2. MIPI-CSI2 Signals

The DART-MX8M-MINI exposes one MIPI-CSI input port of the iMX-8M-MINI SOC.
The following table list the interface pinout for MIPI-CSI port.

1.1.1.1. MIPI-CSI2 Port 1 Signals

Table 14: MIPI-CSI2 P1 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J1.89		MIPI_CSI1_CLK_N		Differential Pair Negative side	SOC.A16
J1.87		MIPI_CSI1_CLK_P		Differential Pair Positive side	SOC.B16
J1.83		MIPI_CSI1_D0_N		Differential Pair Negative side	SOC.A14
J1.81		MIPI_CSI1_D0_P		Differential Pair Positive side	SOC.B14
J1.75		MIPI_CSI1_D1_N		Differential Pair Negative side	SOC.A15
J1.73		MIPI_CSI1_D1_P		Differential Pair Positive side	SOC.B15
J1.77		MIPI_CSI1_D2_N		Differential Pair Negative side	SOC.A17
J1.79		MIPI_CSI1_D2_P		Differential Pair Positive side	SOC.B17
J1.71		MIPI_CSI1_D3_N		Differential Pair Negative side	SOC.A18
J1.69		MIPI_CSI1_D3_P		Differential Pair Positive side	SOC.B18

8.3. Ethernet Interface

The DART-MX8M-MINI exposes two **optional** interfaces on the same pins depending on the configuration:

- MDI lines driven by the AR8033 /ADIN1300 Gigabit PHY – ***"EC" Configuration***
- ENET signal driven by the SOC – **No *"EC" Configuration***

The SOC core implements a triple-speed 10/100/1000-Mbit/s Ethernet MACs compliant with the IEEE802.3-2002 standard.

The i.MX8M processor also consists of HW support for **IEEE1588** standard.

8.3.1. Ethernet PHY

The on SOM Atheros AR8033 / Analog Devices ADIN1300 Gigabit PHY in conjunction with external magnetics on carrier board complete the interface to the media.

8.3.1.1. Gigabit Ethernet Signals

Table 15: Ethernet PHY Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J1.9	EC	ETH_LED_ACT		Signal source is Ethernet PHY. Differential Pair Positive side	AR8033.23/ ADIN1300.21 (via inv. FET)
J1.5	EC	ETH_LED_LINK10_100		Signal source is Ethernet PHY. Differential Pair Negative side	AR8033.26/ ADIN1300-GND
J1.7	EC	ETH_LED_LINK1000		Signal source is Ethernet PHY. Differential Pair Negative side	AR8033.24/ ADIN1300.26 (via level shifter)
J1.3	EC	ETH_NC		With "EC" configuration this pin in Not Connected. Differential Pair Negative side	NC_EC
J1.6	EC	ETH_TRX0_N		Signal source is Ethernet PHY. Differential Pair Negative side	AR8033.12/ ADIN1300.13
J1.8	EC	ETH_TRX0_P		Signal source is Ethernet PHY. Differential Pair Positive side	AR8033.11/ ADIN1300.12
J1.4	EC	ETH_TRX1_N		Signal source is Ethernet PHY. Differential Pair Negative side	AR8033.15/ ADIN1300.15
J1.2	EC	ETH_TRX1_P		Signal source is Ethernet PHY. Differential Pair Positive side	AR8033.14/ ADIN1300.14
J1.12	EC	ETH_TRX2_N		Signal source is Ethernet PHY. Differential Pair Negative side	AR8033.18/ ADIN1300.17
J1.10	EC	ETH_TRX2_P		Signal source is Ethernet PHY. Differential Pair Positive side	AR8033.17/ ADIN1300.16
J1.16	EC	ETH_TRX3_N		Signal source is Ethernet PHY. Differential Pair Negative side	AR8033.21/ ADIN1300.19
J1.14	EC	ETH_TRX3_P		Signal source is Ethernet PHY. Differential Pair Positive side	AR8033.20/ ADIN1300.18

Table 16: AR8033 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_LINK_10_100	OFF	OFF	ON	ON	OFF	OFF
LED_LINK_1000	OFF	OFF	OFF	OFF	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

Table 17: ADIN1300 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_LINK_10_100	OFF	OFF	OFF	OFF	OFF	OFF
LED_LINK_1000	ON	ON	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

8.3.2. 10/100/1000Mbps Ethernet MAC(ENET) Signals

Table 18: ENET Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.10	No EC	ENET_RD0	0	Powered by NVCC_ENET pin	SOC.AE27
J1.12	No EC	ENET_RD1	0	Powered by NVCC_ENET pin	SOC.AD27
J1.14	No EC	ENET_RD2	0	Powered by NVCC_ENET pin	SOC.AD26
J1.16	No EC	ENET_RD3	0	Powered by NVCC_ENET pin	SOC.AC26
J1.9	No EC	ENET_RX_CTL	0	Powered by NVCC_ENET pin	SOC.AF27
J1.7	No EC	ENET_RXC	0	Powered by NVCC_ENET pin	SOC.AE26
J1.4	No EC	ENET_TD0	0	Powered by NVCC_ENET pin	SOC.AG26
J1.2	No EC	ENET_TD1	0	Powered by NVCC_ENET pin	SOC.AF26
J1.6	No EC	ENET_TD2	0	Powered by NVCC_ENET pin	SOC.AG25
J1.8	No EC	ENET_TD3	0	Powered by NVCC_ENET pin	SOC.AF25
J1.3	No EC	ENET_TX_CTL	0	Powered by NVCC_ENET pin	SOC.AF24
J1.5	No EC	ENET_TXC	0	Powered by NVCC_ENET pin	SOC.AG24
J1.5	No EC	ENET_TX_ER	1	Powered by NVCC_ENET pin	SOC.AG24
J1.7	No EC	ENET_RX_ER	1	Powered by NVCC_ENET pin	SOC.AE26

8.3.3. MDIO, 1588 & Clock Signals

Table 19: MDIO, 1588 & Clock Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.60		ENET_1588_EVENT0_IN	1		SOC.AG10
J2.32		ENET_1588_EVENT1_IN	1		SOC.D10
J2.30		ENET_1588_EVENT1_OUT	1		SOC.D9
J1.13		ENET_MDC	0	Shared on SOM with "EC"; powered by NVCC_ENET.	SOC.AC27
J3.58		ENET_MDC	1		SOC.AG11
J1.11		ENET_MDIO	0	Shared on SOM with "EC"; Includes 1.5K Ohm PU to NVCC_ENET with "EC" Only;	SOC.AB27
J1.41		ENET_MDIO	1	Used internally with "EC" (ETH_PHY_3V3_EN_B).	SOC.AF11
J1.1		ENET_PHY_REF_CLK _ROOT_OUT	1		SOC.AG14
J1.6	No EC	IN=ENET_TX_CLK OUT=ENET_REF_CLK_ROOT	1	Powered by NVCC_ENET pin	SOC.AG25
J1.31		NVCC_ENET		ENET pins power IN and OUT: With "EC": AR8033 PHY - Outputs 2.5V, ADIN1300 - Outputs 1.8V. Without "EC" must supply - * RMII uses 1.8 or 3.3V. * RGMII uses 1.8 or 2.5V. * GPIO 1.8V/2.5V/3.3V	SOC.W22

8.4. Wi-Fi & BT

The DART-MX8M-MINI contains a certified high-performance Wi-Fi and Bluetooth (BT) module:

- IEEE 802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR
- BLE 5.2 capabilities
- Modules have an antenna connection through a U. FL JACK connector
- Antenna cable connected to module must have 50-Ω impedance

Figure 3 illustrates the DART-MX8M-MINI internal Wi-Fi and BT connectivity.

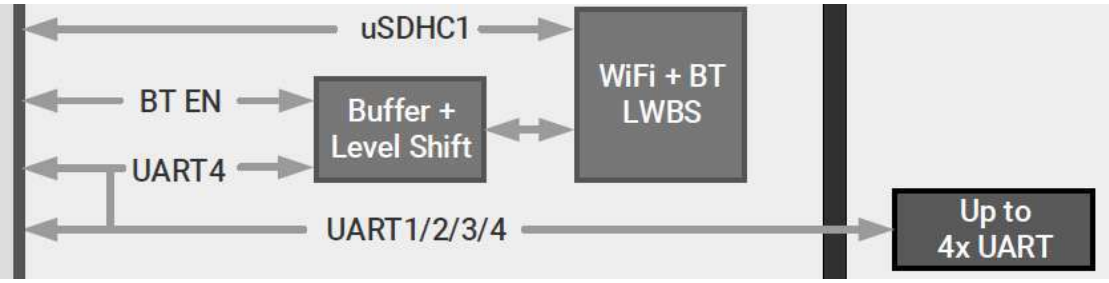


Figure 3: DART-MX8M-MINI Wi-Fi & BT Internal Connection

To allow the most flexible solution the following elements are added to the DART-MX8M-MINI:

- Tristate buffer on the BT link based on UART interface.
  Will allow isolation from the LWB5 module and the use by external circuity via the DART-MX8M-MINI connector.
- Dedicated uSDHC channel for the LWB5 interface.

NOTE

BT UART tristate buffer controlled using SPDIF_EXT_CLK pin alternate function GPIO5_IO05.

- Logic “Low” enables the buffer
- Logic “High” disable it and releases the signals to be used via SOM connectors.

8.4.1. Interface implementation options

8.4.1.1. Module configuration **with "WBD"** option

- System use: **Wi-Fi and Bluetooth**.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT buffer (using GPIO5_IO05) and BT function.
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi**.
  - Disable Wi-Fi function.
  - Enable the BT buffer (using GPIO5_IO05) and BT function.

8.4.1.2. Module configuration **without "WBD"** option

- System use: **No Wi-Fi and no BT**.
  - BT UART interface accessible externally with any of its alternative functions.

8.4.2. Bluetooth Interface signals

Table 20: BT UART interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.20		UART4_TXD	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.B8
J2.22		UART4_CTS_B	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.A8
J2.24		UART4_RXD	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.E6
J2.26		UART4_RTS_B	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.A6

8.4.3. Host Wake Interface signals

The SOM exposes the WIFI/BT module host wake signals together with a GPIO running on the same voltage level.

User is required to connect the relevant host wake signal to the GPIO according to his requirements if applicable.

In case both BT and WIFI wake are required, a logic gate should be included when interfacing GPIO2_IO09.

Table 21: WLAN/BT Host Wake

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.23	WBD	BT_HOST_WAKE		Output from the LWB5 module; Signal level is 1.8V.	LWB5.46
J1.25	WBD	WIFI_HOST_WAKE		Output from the LWB5 module; Signal level is 1.8V.	LWB5.17
J1.29		GPIO2_IO09_1V8	5	SD1_DATA7 can be used as GPIO2_IO09_1V8 to be connected to: BT or WIFI wake signals of LWB5	SOC.W26

8.5. MMC/SD/SDIO

The DART-MX8M-MINI exposes uSDHC2 interface of the iMX 8M-MINI SOC.
The following table list the interface pinout for SD1 signals.

The exposed uSDHC controller SD2 can support up to a 4-bit interface designed to support:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.0.
- 1.8 V and 3.3 V operation. Does not support 1.2 V operation
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode
- Up to SDR104 rate

8.5.1. SD1 signals

The uSDHC controller (SD1) is used internally for the Wi-Fi interface on the SOM.

8.5.2. SD2 signals

Table 22: SD2 interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.90		NVCC_SD2_1V8_3V3		Power output from SOM; Power the SD2 interface IO pins; Will change 1.8V/3.3V according to SD capabilities. Use for PU resistor on SD2_CD_B and SD2_CMD lines.	
J1.74		SD2_CD_B	0	Requires a PU to NVCC_SD2_1V8_3V3	SOC.AA26
J1.82		SD2_CLK	0		SOC.W23
J1.88		SD2_CMD	0	Includes 2.4K PU on SOM Optionally requires a PU to NVCC_SD2_1V8_3V3	SOC.W24
J1.86		SD2_DATA0	0		SOC.AB23
J1.80		SD2_DATA1	0		SOC.AB24
J1.78		SD2_DATA2	0		SOC.V24
J1.84		SD2_DATA3	0		SOC.V23
J1.28		SD2_RESET_B	0	Can be used to control the SD card power in order to perform RESET function.	SOC.AB26
J3.60		SD2_RESET_B	5		SOC.AG10

8.5.3. SD3 signals

The uSDHC controller (SD3) is used internally for the eMMC or NAND interface on the SOM.

8.6. USB Ports

Two USB controllers and PHYs that support USB 2.0 interface are exposed on the DART-MX8M-MINI connectors.
The USB 2.0 controller cores 0 and 1 are also named OTG1 and OTG2 Core respectively.

The following list provides features of each of the controller cores.

- High-Speed/Full-Speed/Low-Speed OTG core
- HS/FS/LS UTMI compliant interface connected to on-chip UTMI PHY
- High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
- High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, Session Request Protocol (SRP), Host Negotiation Protocol (HNP), and Attach Detection Protocol (ADP). ADP support includes dedicated timer hardware and register interface.
- Up to 8 bidirectional endpoints
- Core0(OTG1) Supports charger detection with register interface only
- Low-power mode with local and remote wake-up capability
- Embedded DMA controller in each core

8.6.1. USB Port1 interface signals

Table 23: USB2.0 Port 1 Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.67		USB1_D_N		Differential Pair Negative side	SOC.A22
J3.65		USB1_D_P		Differential Pair Positive side	SOC.B22
J3.56		USB1_ID		USB PHY ID pin	SOC.D22
J3.66		USB1_VBUS		USB PHY power pin; 5V tolerant	SOC.F22

8.6.2. USB Port2 interface signals

Table 24: USB2.0 Port 2 Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.49		USB2_D_N		Differential Pair Negative side	SOC.A23
J3.47		USB2_D_P		Differential Pair Positive side	SOC.B23
J3.44		USB2_ID		USB PHY ID pin	SOC.D23
J3.26		USB2_VBUS		USB PHY power pin; 5V tolerant	SOC.F23

8.6.3. USB OTG interface signals

Table below lists the available DART-MX8M-MINI exposed pins, which can be optionally used to implement a complete OTG functions.

Table 25: USB Port 1 & 2 OTG Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.52		USB1_OTG_ID	1	USB OTG ID alternative signal location. "Low" means the SoC is Host role "Float" means the SoC is Peripheral role.	SOC.AD10
J3.40		USB1_OTG_OC	1	USB OTG OC signal indicates that an overcurrent condition from an external current monitor on the downstream port occurred.	SOC.AD9
J3.50		USB1_OTG_PWR	1	USB OTG PWR signal, active high control signal used to enable power to the downstream port switch.	SOC.AB10
J3.30		USB2_OTG_ID	1		SOC.AC10
J3.38		USB2_OTG_OC	1		SOC.AB9
J3.48		USB2_OTG_PWR	1		SOC.AC9

8.7. PCIe

DART-MX8M-MINI PCI exposes one PCI Express GEN 2 single lane interface. The PCI Express port requires an external 100MHz PCIe compliant reference clock if the function is enabled.

PCI port features:

- Dual mode (DM) controller provides a solution to implement a PCI Express port for a PCI Express root complex or endpoint application.
- Port solution includes the controller, an analog PHY macro, and application logic to source and sink data.
- PCI Express base specification 2.0 with maximum 5.0Gbps lane rate.
- Native PCIe PM Mechanisms

The PCIe controller implements the following standards:

- PCI Express Base Specification, Revision 4.0, Version 0.7
- PIPE Specification for PCI Express, Version 4.3, Intel Corporation
- PCI Local Bus Specification, Revision 3.0
- PCI Bus Power Management Specification, Revision 1.2
- PCI Express Card Electromechanical Specification, Revision 1.1

Note: Access to the above specification requires membership in PCI-SIG.

8.7.1. PCIE Signals

Table 26: PCIE Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.51		PCIE1_REF_CLK_N	0	Differential Pair Negative side PCIE compliant 100MHz reference clock; Terminate with 49.9 Ohm close to the connector.	SOC.A21
J1.53		PCIE1_REF_CLK_P	0	Differential Pair Positive side PCIE compliant 100MHz reference clock; Terminate with 49.9 Ohm close to the connector.	SOC.B21
J1.57		PCIE1_TX_N	0	Differential Pair Negative side	SOC.A20
J1.59		PCIE1_TX_P	0	Differential Pair Positive side	SOC.B20
J1.60		PCIE1_RX_N	0	Differential Pair Negative side	SOC.A19
J1.62		PCIE1_RX_P	0	Differential Pair Positive side	SOC.B19

8.7.2. PCIE Side band signals

Table 27: PCIE Side band signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.3		PCIE1_CLKREQ_B	2		SOC.F19
J1.17		PCIE1_CLKREQ_B	2		SOC.D13

8.8. Audio

The DART-MX8M-MINI features analog and digital type of audio interfaces:

- WM8904 Audio codec Analog outputs & input interfaces:
  - Stereo line input
  - Stereo HP output
  - Digital microphone input
- **S**ynchronous **A**udio **I**nterface (SAI)
- **S**ony **P**hilips **D**igital **I**nter**F**ace (SPDIF)
- **P**ulse **D**ensity **M**odulation (PDM)

8.8.1. Analog Audio

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

Figure 4 illustrates the connectivity for no large AC coupling capacitors

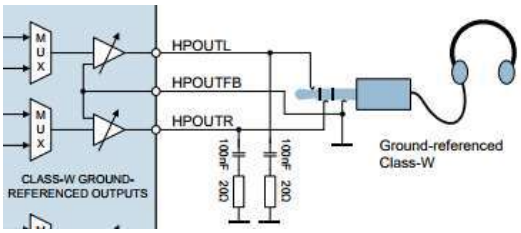


Figure 4: WM8904 Headphone connectivity

Refer to the official data sheet for detailed electrical characteristics of the relevant interfaces.

Table 28: Analog Audio Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.2	AC	HPLOUT		Signal source is Audio Codec. Left headphone output (line or headphone output)	WM8904.13
J2.4	AC	HPROUT		Signal source is Audio Codec. Right headphone output (line or headphone output)	WM8904.15
J2.6	AC	HPOUTFB		Signal source is Audio Codec. Headphone output ground loop noise rejection feedback	WM8904.14
J2.8	AC	LINEIN1_LP		Signal source is external audio driver. Left channel input	WM8904.26
J2.10	AC	LINEIN1_RP		Signal source is external audio driver. Right channel input	WM8904.24
J2.12		AGND		Audio Ground	AGND
J2.14	AC	DMIC_CLK		Signal source is external digital microphone.	WM8904.1
J2.16	AC	DMIC_DATA_1V8		Signal source is external digital microphone. Signal level is 1.8V;	WM8904.27

8.8.2. SAI - Synchronous Audio Interface

The I2S (or I2S) module of the iMX 8M-MINI SOC, provides a synchronous audio interface (SAI) that supports fullduplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.

Main Features of the SAI include:

- Transmitter with independent bit clock and frame sync supporting 8 data lines
- Receiver with independent bit clock and frame sync supporting 8 data lines
- Each data line can support a maximum Frame size of 32 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 8 x 32-bit FIFO for each transmit and receive data line
- Supports graceful restart after FIFO error
- Supports automatic restart after FIFO error without software intervention
- Supports packing of 8-bit and 16-bit data into each 32-bit FIFO word
- Supports combining multiple data line FIFOs into single data line FIFO
- Independent 32-bit timestamp counters and bit counters for monitoring transmit and
- receive progress

NOTE

Some of the features are not supported across all SAI instances; See i.MX 8M-MINI Applications Processors Reference Manual for further details.

Besides the general audio input/output function, the audio interfaces will support the following features:

- SAI-1 supports up to 16-channels TX (8 lanes) and RX (8 lanes) at 384KHz/32-bit
- SAI-5 supports up to 8-channels TX (4 lanes) and RX (4 lanes) at 384KHz/32-bit
- SAI-2/3 supports up to 4-channels TX (2 lanes) and RX (2 lanes) at 384KHz/32-bit
- SAI-6 support up to 2-channels TX (1 lane) and RX (1 lane) at 384KHz/32-bit
- SAI-1 supports glue-less switching between PCM and DSD operation for popular audio DACs
- SAI-1 and SAI-5 supports up-to 8 channels of PDM
- SPDIF supports raw capture mode that can save all the incoming bits into audio buffer

The DART-MX8M-MINI exposes all 5 SAI interfaces the iMX 8M-MINI SOC presents.

The SAI-1/2/3/5/6 and SPDIF-1 share GPIO pads on the chip through IOMUX. Common **U**se **C**ases (UC) supported by the audio interfaces are listed in the table below (many other configurations are possible). The number is the data lanes supported.

8.8.2.1. SAI Signals Definitions

The following table details the SAI interface signals definition.

Table 29: SAI interface signals definition

NAME	FUNCTION	DIR
SAI_TXC	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_TXFS	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_TXD[0:0]	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristate whenever not transmitting a word	O
SAI_RXC	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_RXFS	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_RXD [0:0]	Receive Data. The receive data is sampled synchronously by the bit clock.	I
SAI_MCLK	Audio Master Clock.	I

8.8.2.2. SAI1 Signals

Table 30: SAI1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.82		SAI1_MCLK	0		SOC.AB18
J2.57		SAI1_RXC	0		SOC.AF16
J2.61		SAI1_RXD0	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG15
J2.59		SAI1_RXD1	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF15
J2.63		SAI1_RXD2	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG17
J2.62		SAI1_RXD3	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF17
J2.65		SAI1_RXD4	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG18
J2.69		SAI1_RXD5	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF18
J2.66		SAI1_RXD6	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG19
J2.68		SAI1_RXD7	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF19
J2.55		SAI1_RXFS	0		SOC.AG16
J2.69		SAI1_RXFS	3	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF18
J2.46		SAI1_TXC	1		SOC.AD15
J2.72		SAI1_TXC	0		SOC.AC18
J2.82		SAI1_TXC	2		SOC.AB18
J2.34		SAI1_TXD0	1		SOC.AB15
J2.70		SAI1_TXD0	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG20
J2.40		SAI1_TXD1	1		SOC.AC15

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.61		SAI1_TXD1	2	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG15
J2.67		SAI1_TXD1	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF20
J2.36		SAI1_TXD2	1		SOC.AD18
J2.78		SAI1_TXD2	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG21
J2.42		SAI1_TXD3	1		SOC.AC14
J2.73		SAI1_TXD3	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF21
J2.38		SAI1_TXD4	1		SOC.AD13
J2.68		SAI1_TXD4	3	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF19
J2.74		SAI1_TXD4	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG22
J2.44		SAI1_TXD5	1		SOC.AC13
J2.71		SAI1_TXD5	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF22
J2.80		SAI1_TXD6	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG23
J2.76		SAI1_TXD7	0	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF23
J2.38		SAI1_TXFS	2		SOC.AD13
J2.42		SAI1_TXFS	2		SOC.AC14
J2.44		SAI1_TXFS	2		SOC.AC13
J2.64		SAI1_TXFS	0		SOC.AB19
J2.68		SAI1_TXFS	2	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF19

[1] For boot configuration refer to section 76

8.8.2.3. SAI2 Signals

Table 31: SAI2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.54		SAI2_MCLK	0		SOC.AD19
J2.50		SAI2_RXC	0		SOC.AB22
J2.58		SAI2_RXD0	0		SOC.AC24
J2.48		SAI2_RXD1	3		SOC.AC19
J2.48		SAI2_RXFS	0		SOC.AC19
J2.56		SAI2_TXC	0		SOC.AD22
J2.60		SAI2_TXD0	0		SOC.AC22
J2.52		SAI2_TXD1	3		SOC.AD23
J2.52		SAI2_TXFS	0		SOC.AD23

8.8.2.4. SAI3 Signals

Table 32: SAI3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.2	No AC	SAI3_RXD	0	With “AC” configuration do not alter PINMUX function.	SOC.AF7
J2.4	No AC	SAI3_TXC	0	With “AC” configuration do not alter PINMUX function.	SOC.AG6
J2.6	No AC	SAI3_RXFS	0	With “AC” configuration do not alter PINMUX function.	SOC.AG8
J2.6	No AC	SAI3_RXD1	3	With “AC” configuration do not alter PINMUX function.	SOC.AG8
J2.8	No AC	SAI3_RXC	0	With “AC” configuration do not alter PINMUX function.	SOC.AG7
J2.10	No AC	SAI3_TXFS	0	With “AC” configuration do not alter PINMUX function.	SOC.AC6
J2.10	No AC	SAI3_TXD1	3	With “AC” configuration do not alter PINMUX function.	SOC.AC6
J2.14	No AC	SAI3_TXD	0	With “AC” configuration do not alter PINMUX function.	SOC.AF6
J2.16	No AC	SAI3_MCLK	0	With “AC” configuration do not alter PINMUX function.	SOC.AD6

8.8.2.5. SAI5 Signals

Table 33: SAI5 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.16	No AC	SAI5_MCLK	2	With "AC" configuration do not alter PINMUX function.	SOC.AD6
J2.46		SAI5_MCLK	0		SOC.AD15
J2.54		SAI5_MCLK	1		SOC.AD19
J2.82		SAI5_MCLK	1		SOC.AB18
J2.8	No AC	SAI5_RXC	2	With "AC" configuration do not alter PINMUX function.	SOC.AG7
J2.40		SAI5_RXC	0		SOC.AC15
J2.57		SAI5_RXC	1		SOC.AF16
J2.2	No AC	SAI5_RXD0	2	With "AC" configuration do not alter PINMUX function.	SOC.AF7
J2.36		SAI5_RXD0	0		SOC.AD18
J2.61		SAI5_RXD0	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG15
J2.10	No AC	SAI5_RXD1	2	With "AC" configuration do not alter PINMUX function.	SOC.AC6
J2.42		SAI5_RXD1	0		SOC.AC14
J2.59		SAI5_RXD1	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF15
J2.4	No AC	SAI5_RXD2	2	With "AC" configuration do not alter PINMUX function.	SOC.AG6
J2.38		SAI5_RXD2	0		SOC.AD13
J2.63		SAI5_RXD2	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG17
J2.14	No AC	SAI5_RXD3	2	With "AC" configuration do not alter PINMUX function.	SOC.AF6
J2.44		SAI5_RXD3	0		SOC.AC13
J2.62		SAI5_RXD3	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF17
J2.6	No AC	SAI5_RXFS	2	With "AC" configuration do not alter PINMUX function.	SOC.AG8
J2.34		SAI5_RXFS	0		SOC.AB15
J2.55		SAI5_RXFS	1		SOC.AG16
J2.38		SAI5_TXC	3		SOC.AD13
J2.50		SAI5_TXC	1		SOC.AB22
J2.72		SAI5_TXC	1		SOC.AC18
J2.44		SAI5_TXD0	3		SOC.AC13
J2.58		SAI5_TXD0	1		SOC.AC24
J2.70		SAI5_TXD0	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG20
J2.48		SAI5_TXD1	2		SOC.AC19
J2.52		SAI5_TXD1	1		SOC.AD23
J2.67		SAI5_TXD1	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF20
J2.56		SAI5_TXD2	1		SOC.AD22
J2.78		SAI5_TXD2	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG21
J2.60		SAI5_TXD3	1		SOC.AC22
J2.73		SAI5_TXD3	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF21
J2.42		SAI5_TXFS	3		SOC.AC14
J2.48		SAI5_TXFS	1		SOC.AC19
J2.64		SAI5_TXFS	1		SOC.AB19

[1] For boot configuration refer to section 76

8.8.2.6. SAI6 Signals

Table 34: SAI6 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.68		SAI6_MCLK	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF19
J2.76		SAI6_MCLK	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF23
J2.65		SAI6_RXC	2	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG18
J2.74		SAI6_RXC	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG22
J2.69		SAI6_RXD0	2	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF18
J2.71		SAI6_RXD0	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF22
J2.66		SAI6_RXFS	2	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG19
J2.80		SAI6_RXFS	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG23
J2.65		SAI6_TXC	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG18
J2.74		SAI6_TXC	2	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG22
J2.69		SAI6_TXD0	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF18
J2.71		SAI6_TXD0	2	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF22
J2.66		SAI6_TXFS	1	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG19
J2.80		SAI6_TXFS	2	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG23

[1] For boot configuration refer to section 76

8.8.3. PDM - Microphone Interface (MICFIL)

The PDM module of the iMX 8M-MINI SOC, provides a popular way to deliver audio from microphones to the processor in several applications, such as mobile telephones.
Up to 8 channels can be implemented with 4 lanes.

PDM block main features are:
Fixed filtering characteristics for audio application.

- Full or partial set of channels operation with individual enable control.
- Programmable PDM clock generator.
- Programmable decimation rate.
- 16-bit signed output result.
- Overall stopband attenuation more than 80dB.
- Overall passband ripple less than 0.2dB.
- CIC filter
    - 5th order.
    - Programmable decimation rate.
- DC remover
    - First order IIR filter.
    - Programmable cut-off frequency.
- FIFOs with DMA capability.
    - Each FIFO is 8 entries length.
- Hardware Voice Activity Detector (HWVAD).
    - Interrupt capability.
    - Zero-Crossing Detection (ZCD) option.

The PDM Microphone Interface module is composed of:

- An input interface for each pair of PDM microphones.
- A decimation filter by channel.
- A FIFO by channel.
- A time generation unit.
- Shared interfaces to DMA, interrupts and SoC.
- One or more Hardware Voice Activity Detectors (HWVAD).

8.8.3.1. PDM Signals

Table 35: PDM Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.36		PDM_BIT0	4		SOC.AD18
J2.61		PDM_BIT0	3	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG15
J2.42		PDM_BIT1	4		SOC.AC14
J2.59		PDM_BIT1	3	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF15
J2.38		PDM_BIT2	4		SOC.AD13
J2.63		PDM_BIT2	3	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG17
J2.44		PDM_BIT3	4		SOC.AC13
J2.62		PDM_BIT3	3	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF17
J2.40		PDM_CLK	4		SOC.AC15
J2.76		PDM_CLK	3	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF23
J2.82		PDM_CLK	3		SOC.AB18

[1] For boot configuration refer to section 8.19.176

8.8.4. SPDIF – Sony Philips Digital Interface Format

A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality including frequency measurement block that allows the precise measurement of an incoming sampling frequency.
The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs with Channel Status and User bits.
For the SPDIF transmitter, the audio data is provided by the processor dedicated registers along with Channel Status and User bits.

8.8.4.1. SPDIF Signals

Table 36: SPDIF Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.28		SPDIF_RX	0		SOC.AG9
J3.32		SPDIF_EXT_CLK	0	Used internally with "WBD" as (GPIO5_IO05) BT_BUF_EN_B; Set this pin HIGH to disable BT buffer in order to release BT UART pins.	SOC.AF8
J3.36		SPDIF_TX	0		SOC.AF9

8.9. UART Interfaces

The DART-MX8M-MINI exposes up to **four** UART interfaces some of which are multiplexed with other peripherals. UART4 is used on SOM for Bluetooth interface and can be accessible only if the on SOM buffer disabled or without ***"WBD" Configuration***.

The UART includes the following features:

- High-speed TIA/EIA-232-F compatible, up to 4.15 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9-bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
- RS-485 driver direction control via CTS_B signal
- Edge-selectable RTS_B and edge-detect interrupts
- Transmitter FIFO empty interrupt suppression
- Can serve both as DTE or DCE device
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode
- RTS_B, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE) interrupts wake the processor from STOP mode

Table 37: UART I/O Configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_ DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX _DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

8.9.1.1. UART1 Signals

Table 38: UART1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.52		UART1_CTS_B	4		SOC.AD23
J2.87		UART1_CTS_B	1		SOC.E18
J2.58		UART1_RTS_B	4		SOC.AC24
J2.89		UART1_RTS_B	1		SOC.D18
J2.50		UART1_RXD	4		SOC.AB22
J2.88		UART1_RXD	0	Used as debug UART on Variscite base board.	SOC.E14
J2.48		UART1_TXD	4		SOC.AC19
J2.90		UART1_TXD	0	Used as debug UART on Variscite base board.	SOC.F13

8.9.1.2. UART2 Signals

Table 39: UART2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.8	No AC	UART2_CTS_B	4	With “AC” configuration do not alter PINMUX function.	SOC.AG7
J3.3		UART2_CTS_B	1		SOC.F19
J2.2	No AC	UART2_RTS_B	4	With “AC” configuration do not alter PINMUX function.	SOC.AF7
J3.1		UART2_RTS_B	1		SOC.F18
J2.10	No AC	UART2_RXD	4	With “AC” configuration do not alter PINMUX function.	SOC.AC6
J2.85		UART2_RXD	0		SOC.F15
J2.4	No AC	UART2_TXD	4	With “AC” configuration do not alter PINMUX function.	SOC.AG6
J2.86		UART2_TXD	0		SOC.E15

8.9.1.3. UART3 Signals

Table 40: UART3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.81		UART3_CTS_B	1		SOC.A7
J2.79		UART3_RTS_B	1		SOC.B6
J2.77		UART3_RXD	1		SOC.D6
J2.87		UART3_RXD	0		SOC.E18
J2.83		UART3_TXD	1		SOC.B7
J2.89		UART3_TXD	0		SOC.D18

8.9.1.4. UART4 Signals

Table 41: UART4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.20		UART4_TXD	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.B8
J2.22		UART4_CTS_B	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.A8
J2.24		UART4_RXD	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.E6
J2.26		UART4_RTS_B	1	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.A6
J3.1		UART4_TXD	0		SOC.F18
J3.3		UART4_RXD	0		SOC.F19

8.10. ECSPI - Enhanced Configurable SPI

DART-MX8M-MINI exposes all ECSPI1/ ECSPI2/ ECSPI3 pins.
ECSPI2 signals used on SOM for alternate function of BT UART with ***"WBD" Configuration.*** In case other alternative function is required with the ***"WBD"*** users can either order without Wi-Fi configuration, or alternatively disable the BT UART buffer driving this interface.

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block with full-duplex enhanced Synchronous Serial Interface and data rate up to 52 Mbit/s.

Key features of the ECSPI include:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Refer to the product data sheet for the maximum operating frequency

8.10.1.1. ECSPI1 Signals

Table 42: ECSPI1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.77		ECSPI1_SCLK	0	SPI Serial Clock	SOC.D6
J2.79		ECSPI1_SS0	0	SPI Slave Select Signal	SOC.B6
J2.81		ECSPI1_MISO	0	SPI Master data In - Slave data Out signal	SOC.A7
J2.83		ECSPI1_MOSI	0	SPI Master data Out - Slave data In signal	SOC.B7

8.10.1.2. ECSPI2 Signals

Table 43: ECSPI2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.20		ECSPI2_MOSI	0	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.B8
J2.22		ECSPI2_MISO	0	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.A8
J2.24		ECSPI2_SCLK	0	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.E6
J2.26		ECSPI2_SS0	0	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.A6

8.10.1.3. ECSPI3 Signals

Table 44: ECSPI3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.85		ECSPI3_MISO	1		SOC.F15
J2.86		ECSPI3_SS0	1		SOC.E15
J2.88		ECSPI3_SCLK	1	Used as debug UART on Variscite base board.	SOC.E14
J2.90		ECSPI3_MOSI	1	Used as debug UART on Variscite base board.	SOC.F13

8.11. QSPI/FlexSPI - Quad Serial Peripheral Interface

DART-MX8M-MINI exposes **one** out of the two QSPI interfaces which can also be configured as FlexSPI interface. DART-MX8M-MINI exposes one slave select signal.

The Quad SPI module acts as an interface to external serial flash devices. It can function as one of the boot devices.

The DART-MX8M-MINI QSPI module features:

- Can be configured as 1/2/4-bit operation
- Single-channel operation
- Support both SDR mode and DDR mode
- Support up to 166MHz SDR Mode and 166MHz DDR Mode (with external Flash device DQS input)
- Support up to 133MHz SDR Mode and 66MHz DDR Mode (with internal DQS loopback mode)

The DART-MX8M-MINI FlexSPI module features:

- Flexible sequence engine (LUT table) to support various vendor devices
    - Serial NOR Flash or other device with similar SPI protocol as Serial NOR Flash
    - Serial NAND Flash
    - HyperBus device (HyperFlash/HyperRAM)
    - FPGA device
- Flash access mode
    - Single/Dual/Quad mode
    - SDR/DDR mode
    - Individual mode
- Support several sampling clock modes
- Automatic Data Learning to select correct sample clock phase
- Memory mapped read/write access by AHB Bus
- Software triggered Flash read/write access by IP Bus

8.11.1. QSPI A Signals

Table 45: QSPI_A Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.48	eMMC	QSPIA_DATA0_1V8	1	Can be used as QSPIA_D0_1V8; DO NOT connect with NAND configuration!	SOC.P23
J1.32	eMMC	QSPIA_DATA1_1V8	1	Can be used as QSPIA_D1_1V8; DO NOT connect with NAND configuration!	SOC.K24
J1.50	eMMC	QSPIA_DATA2_1V8	1	Can be used as QSPIA_D2_1V8; DO NOT connect with NAND configuration!	SOC.K23
J1.46	eMMC	QSPIA_DATA3_1V8	1	Can be used as QSPIA_D3_1V8; DO NOT connect with NAND configuration!	SOC.N23
J1.38	eMMC	QSPIA_DQS_1V8	1	Can be used as QSPIA_DQS_1V8; DO NOT connect with NAND configuration!	SOC.R22
J1.40	eMMC	QSPIA_SCLK_1V8	1	Can be used as QSPIA_SCLK_1V8; DO NOT connect with NAND configuration!	SOC.N22
J1.34	eMMC	QSPIA_SS0_B_1V8	1	Can be used as QSPIA_SS0_B_1V8; DO NOT connect with NAND configuration!	SOC.N24

8.11.2. QSPI B Signals

QSPI B signals are used internally for the eMMC/NAND interface on the SOM.

8.12. NAND

The DART-MX8M-MINI can be configured with NAND memory instead of an eMMC device.
All NAND signals are used internally and are not exposed to the connector.

8.13. I²C

The DART-MX8M-MINI SOM exposes up to three I2C interfaces on the connectors: I2C2, I2C3 and I2C4.

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices.
This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The I2C has the following key features:

- Compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).
- Multi-master operation.
- After a reset, the I2C defaults to Slave Receive operations.
- Software programmability for one of 64 different serial clock frequencies:
  - Standard mode, I2C supports the data transfer rates up to 100 Kbits/s
  - In Fast mode, data transfer rates up to 400 Kbits/s can be achieved
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

8.13.1. I2C2 Signals

Table 46: I2C2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.30		I2C2_SDA	0		SOC.D9
J2.32		I2C2_SCL	0		SOC.D10

8.13.2. I2C3 Signals

Table 47: I2C3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.42		I2C3_SDA	0	10K internal PU included; Shared with “AC”	SOC.F10
J3.46		I2C3_SCL	0	10K internal PU included; Shared with “AC”	SOC.E10

8.13.3. I2C4 Signals

Table 48: I2C4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.17		I2C4_SCL	0		SOC.D13
J1.19		I2C4_SDA	0		SOC.E13

8.14. PWM - Pulse Width Modulation

The DART-MX8M-MINI exposes all 4 of the PWM outputs.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- Can be programmed to select one of three clock signals as its source frequency, with a maximum of 66MHz
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

8.14.1. PWM Signals

Table 49: PWM Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.19		PWM1_OUT	1		SOC.E13
J3.32	WBD			Used internally with "WBD" as (GPIO5_IO05) BT_BUF_EN_B; Set this pin HIGH to disable BT buffer in order to release BT UART pins.	SOC.AF8
J3.32	No WBD	PWM1_OUT	1		SOC.AF8
J3.64		PWM1_OUT	1		SOC.AF14
J1.17		PWM2_OUT	1		SOC.D13
J3.28		PWM2_OUT	1		SOC.AG9
J3.40		PWM2_OUT	5		SOC.AD9
J3.36		PWM3_OUT	1		SOC.AF9
J3.42		PWM3_OUT	1	10K internal PU included;	SOC.F10
J3.48		PWM3_OUT	5		SOC.AC9
J2.16	No AC	PWM4_OUT	1		SOC.AD6
J3.38		PWM4_OUT	5		SOC.AB9
J3.46		PWM4_OUT	1	10K internal PU included;	SOC.E10

8.15. GPT – General Purpose Timer

The DART-MX8M-MINI exposes the GPT interface on its connectors.

Each GPT has a 32-bit up-counter. The timer counter value can be captured in a register using an event on an external pin. The capture trigger can be programmed to be a rising or/and falling edge. The GPT can also generate an event on the output compare pins and an interrupt when the timer reaches a programmed value. The GPT has a 12-bit prescaler, which provides a programmable clock frequency derived from multiple clock sources.

GPT Features include:

- One 32-bit up-counter with clock source selection, including external clock
- Two input capture channels with a programmable trigger edge
- Three outputs compare channels with a programmable output mode. A "forced compare" feature is also available
- Can be programmed to be active in low power and debug modes
- Interrupt generation at capture, compare, and rollover events
- Restart or free-run modes for counter operations

8.15.1. GPT Signals

Table 50: GPT Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.6	No AC	GPT1_CAPTURE1	1	With “AC” configuration do not alter PINMUX function.	SOC.AG8
J2.10	No AC	GPT1_CAPTURE2	1	With “AC” configuration do not alter PINMUX function.	SOC.AC6
J2.8	No AC	GPT1_CLK	1	With “AC” configuration do not alter PINMUX function.	SOC.AG7
J2.2	No AC	GPT1_COMPARE1	1	With “AC” configuration do not alter PINMUX function.	SOC.AF7
J2.4	No AC	GPT1_COMPARE2	1	With “AC” configuration do not alter PINMUX function.	SOC.AG6
J2.14	No AC	GPT1_COMPARE3	1	With “AC” configuration do not alter PINMUX function.	SOC.AF6
J3.46		GPT2_CLK	2	10K internal PU included;	SOC.E10
J3.42		GPT3_CLK	2	10K internal PU included;	SOC.F10

8.16. Reference Clocks

Up to eight clock outputs from the CCM available from normal GPIO pads via IOMUX can be used to clock external devices.

CLKIN and CLKOUT runs at 1.8V primary used for testing purposes.

8.16.1. Clock Signals

Table 51: Clock Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.35		CLKIN1_1V8	0	Optional clock input for CCM Analog	SOC.H27
J1.37		CLKIN2_1V8	0	Optional clock input for CCM Analog	SOC.J27
J3.48		CLKO1	6	SOC CCM Clock OUT 1	SOC.AC9
J3.38		CLKO2	6	SOC CCM Clock OUT 2	SOC.AB9
J1.45		CLKOUT1_1V8	0	CCM Analog internal clocks test output	SOC.H26
J1.47		CLKOUT2_1V8	0	CCM Analog internal clocks test output	SOC.J26
J1.1		EXT_CLK1	6	SOC CCM External Clock 1	SOC.AG14
J3.64		EXT_CLK2	6	SOC CCM External Clock 2	SOC.AF14
J3.58		EXT_CLK3	6	SOC CCM External Clock 3	SOC.AG11
J1.41		EXT_CLK4	6	Used internally with "EC" (ETH_PHY_3V3_EN_B). SOC CCM External Clock 4	SOC.AF11
J3.64		REF_CLK_24M	5	SOC ANAMIX 24Mhz reference clock	SOC.AF14
J1.1		REF_CLK_32K	5	SOC ANAMIX 32KHz reference clock	SOC.AG14

8.17. GPIO - General Purpose Input Output

The GPIO general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

- **When configured as an output:**
  It is possible to write to an internal register to control the state driven on the output pin
- **When configured as an input:**
  It is possible to detect the state of the input by reading the state of an internal register
- GPIO peripheral can produce CORE interrupts
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control
- Up to 111 GPIO are available on the DART-MX8M-MINI

8.17.1. GPIO Signals

The DART-MX8M-MINI exposes up to 111 GPIO lines.

- Out of the 111 GPIO signals 8 run at 1.8V while others at 3.3V levels.

- Signals running on 1.8V denoted by "**_1V8**" in their name and care should be noted not drive them with higher voltage.

Table 52: GPIO Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.1		GPIO1_IO00	0		SOC.AG14
J3.64		GPIO1_IO01	0		SOC.AF14
J2.28		GPIO1_IO02	0	As WDOG_B alternate pin function could be used to initiate power up sequence in case of a watch dog event. See footnote [1];	SOC.AG13
J3.54		GPIO1_IO03	0		SOC.AF13
J3.62		GPIO1_IO05	0		SOC.AF12
J3.58		GPIO1_IO06	0		SOC.AG11
J1.41		GPIO1_IO07	0	Used internally with "EC" (ETH_PHY_3V3_EN_B).	SOC.AF11
J3.60		GPIO1_IO08	0		SOC.AG10
J3.52		GPIO1_IO10	0		SOC.AD10
J3.30		GPIO1_IO11	0		SOC.AC10
J3.50		GPIO1_IO12	0		SOC.AB10
J3.40		GPIO1_IO13	0		SOC.AD9
J3.48		GPIO1_IO14	0		SOC.AC9
J3.38		GPIO1_IO15	0		SOC.AB9
J1.13		GPIO1_IO16	5	Shared on SOM with "EC"; Powered by NVCC_ENET.	SOC.AC27
J1.11		GPIO1_IO17	5	Shared on SOM with "EC"; Includes 1.5K Ohm PU to NVCC_ENET with "EC" Only;	SOC.AB27
J1.8	No EC	GPIO1_IO18	5	Powered by NVCC_ENET pin RGMII Data out	SOC.AF25
J1.6	No EC	GPIO1_IO19	5	Powered by NVCC_ENET pin RGMII Data out	SOC.AG25
J1.2	No EC	GPIO1_IO20	5	Powered by NVCC_ENET pin RGMII Data out	SOC.AF26
J1.4	No EC	GPIO1_IO21	5	Powered by NVCC_ENET pin RGMII Data out	SOC.AG26
J1.3	No EC	GPIO1_IO22	5	Powered by NVCC_ENET pin RGMII Transmit data Control	SOC.AF24

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.5	No EC	GPIO1_IO23	5	Powered by NVCC_ENET pin ENET RGMII Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	SOC.AG24
J1.9	No EC	GPIO1_IO24	5	Powered by NVCC_ENET pin RGMII Receive data Control	SOC.AF27
J1.7	No EC	GPIO1_IO25	5	Powered by NVCC_ENET pin ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	SOC.AE26
J1.10	No EC	GPIO1_IO26	5	Powered by NVCC_ENET pin RGMII Data in	SOC.AE27
J1.12	No EC	GPIO1_IO27	5	Powered by NVCC_ENET pin RGMII Data in	SOC.AD27
J1.14	No EC	GPIO1_IO28	5	Powered by NVCC_ENET pin RGMII Data in	SOC.AD26
J1.16	No EC	GPIO1_IO29	5	Powered by NVCC_ENET pin RGMII Data in	SOC.AC26
J1.74		GPIO2_IO012	5	Requires a PU to NVCC_SD2_1V8_3V3	SOC.AA26
J1.29		GPIO2_IO09_1V8	5	SD1_DATA7 can be used as GPIO2_IO09_1V8 to be connected to: BT or WIFI wake signals of LWB5	SOC.W26
J1.82		GPIO2_IO13	5		SOC.W23
J1.88		GPIO2_IO14	5	Includes 2.4K PU on SOM Optionally requires a PU to NVCC_SD2_1V8_3V3	SOC.W24
J1.86		GPIO2_IO15	5		SOC.AB23
J1.80		GPIO2_IO16	5		SOC.AB24
J1.78		GPIO2_IO17	5		SOC.V24
J1.84		GPIO2_IO18	5		SOC.V23
J1.28		GPIO2_IO19	5	Can be used to control the SD card power in order to perform SD RESET function.	SOC.AB26
J1.40	eMMC	GPIO3_IO00_1V8	5	Can be used as QSPIA_SCLK_1V8; DO NOT connect with NAND configuration !	SOC.N22
J1.34	eMMC	GPIO3_IO01_1V8	5	Can be used as QSPIA_SS0_B_1V8; DO NOT connect with NAND configuration !	SOC.N24
J1.48	eMMC	GPIO3_IO06_1V8	5	Can be used as QSPIA_D0_1V8; DO NOT connect with NAND configuration !	SOC.P23
J1.32	eMMC	GPIO3_IO07_1V8	5	Can be used as QSPIA_D1_1V8; DO NOT connect with NAND configuration !	SOC.K24
J1.50	eMMC	GPIO3_IO08_1V8	5	Can be used as QSPIA_D2_1V8; DO NOT connect with NAND configuration !	SOC.K23
J1.46	eMMC	GPIO3_IO09_1V8	5	Can be used as QSPIA_D3_1V8; DO NOT connect with NAND configuration !	SOC.N23
J1.38	eMMC	GPIO3_IO14_1V8	5	Can be used as QSPIA_DQS_1V8; DO NOT connect with NAND configuration !	SOC.R22
J2.34		GPIO3_IO19	5		SOC.AB15
J2.40		GPIO3_IO20	5		SOC.AC15
J2.36		GPIO3_IO21	5		SOC.AD18
J2.42		GPIO3_IO22	5		SOC.AC14
J2.38		GPIO3_IO23	5		SOC.AD13
J2.44		GPIO3_IO24	5		SOC.AC13
J2.46		GPIO3_IO25	5		SOC.AD15
J2.55		GPIO4_IO00	5		SOC.AG16
J2.57		GPIO4_IO01	5		SOC.AF16
J2.61		GPIO4_IO02	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG15
J2.59		GPIO4_IO03	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF15
J2.63		GPIO4_IO04	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG17
J2.62		GPIO4_IO05	5	Pin value latched with rise of POR_B;	SOC.AF17

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
				Set BOOG_CFG value; See footnote [1]	
J2.65		GPIO4_IO06	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG18
J2.69		GPIO4_IO07	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF18
J2.66		GPIO4_IO08	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG19
J2.68		GPIO4_IO09	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF19
J2.64		GPIO4_IO10	5		SOC.AB19
J2.72		GPIO4_IO11	5		SOC.AC18
J2.70		GPIO4_IO12	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG20
J2.67		GPIO4_IO13	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF20
J2.78		GPIO4_IO14	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG21
J2.73		GPIO4_IO15	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF21
J2.74		GPIO4_IO16	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG22
J2.71		GPIO4_IO17	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF22
J2.80		GPIO4_IO18	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AG23
J2.76		GPIO4_IO19	5	Pin value latched with rise of POR_B; Set BOOG_CFG value; See footnote [1]	SOC.AF23
J2.82		GPIO4_IO20	5		SOC.AB18
J2.48		GPIO4_IO21	5		SOC.AC19
J2.50		GPIO4_IO22	5		SOC.AB22
J2.58		GPIO4_IO23	5		SOC.AC24
J2.52		GPIO4_IO24	5		SOC.AD23
J2.56		GPIO4_IO25	5		SOC.AD22
J2.60		GPIO4_IO26	5		SOC.AC22
J2.54		GPIO4_IO27	5		SOC.AD19
J2.6	No AC	GPIO4_IO28	5	With “AC” configuration do not alter PINMUX function.	SOC.AG8
J2.8	No AC	GPIO4_IO29	5	With “AC” configuration do not alter PINMUX function.	SOC.AG7
J2.2	No AC	GPIO4_IO30	5	With “AC” configuration do not alter PINMUX function.	SOC.AF7
J2.10	No AC	GPIO4_IO31	5	With “AC” configuration do not alter PINMUX function.	SOC.AC6
J2.4	No AC	GPIO5_IO00	5	With “AC” configuration do not alter PINMUX function.	SOC.AG6
J2.14	No AC	GPIO5_IO01	5	With “AC” configuration do not alter PINMUX function.	SOC.AF6
J2.16	No AC	GPIO5_IO02	5	With “AC” configuration do not alter PINMUX function.	SOC.AD6
J3.36		GPIO5_IO03	5		SOC.AF9
J3.28		GPIO5_IO04	5		SOC.AG9
J3.32		GPIO5_IO05	5	Used internally with "WBD" as (GPIO5_IO05) BT_BUF_EN_B; Set this pin HIGH to disable BT buffer in order to release BT UART pins.	SOC.AF8
J2.77		GPIO5_IO06	5		SOC.D6
J2.83		GPIO5_IO07	5		SOC.B7
J2.81		GPIO5_IO08	5		SOC.A7
J2.79		GPIO5_IO09	5		SOC.B6
J2.24		GPIO5_IO10	5	Used internally with "WBD";	SOC.E6

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
				Function can be released if BT Buffer disabled. Always exposed;	
J2.20		GPIO5_IO11	5	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.B8
J2.22		GPIO5_IO12	5	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.A8
J2.26		GPIO5_IO13	5	Used internally with "WBD"; Function can be released if BT Buffer disabled. Always exposed;	SOC.A6
J2.32		GPIO5_IO16	5		SOC.D10
J2.30		GPIO5_IO17	5		SOC.D9
J3.46		GPIO5_IO18	5	10K internal PU included;	SOC.E10
J3.42		GPIO5_IO19	5	10K internal PU included;	SOC.F10
J1.17		GPIO5_IO20	5		SOC.D13
J1.19		GPIO5_IO21	5		SOC.E13
J2.88		GPIO5_IO22	5	Used as debug UART on Variscite base board.	SOC.E14
J2.90		GPIO5_IO23	5	Used as debug UART on Variscite base board.	SOC.F13
J2.85		GPIO5_IO24	5		SOC.F15
J2.86		GPIO5_IO25	5		SOC.E15
J2.87		GPIO5_IO26	5		SOC.E18
J2.89		GPIO5_IO27	5		SOC.D18
J3.3		GPIO5_IO28	5		SOC.F19
J3.1		GPIO5_IO29	5		SOC.F18

8.18. JTAG

The System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

The JTAG port allows debug-related control and status, such as putting selected cores into reset and/or debug mode and the ability to monitor individual core status signals via JTAG. JTAG port interfaces the M4 and Cortex A53 Cores DAP - debug access port.
The DART-MX8M-MINI JTAG MOD pin is hardware tied low and enables the Daisy chain ALL mode only, used for common SW debug (High speed and production).

8.18.1. JTAG signals

Table 53: JTAG Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.1		JTAG_TCK	0	Need to include an external PD of 4.7K Ohm	SOC.F26
J2.7		JTAG_TDI	0		SOC.E27
J2.9		JTAG_TDO	0		SOC.E26
J2.3		JTAG_TMS	0		SOC.F27
J2.5		JTAG_TRST_B	0	Active low signal;	SOC.C27

8.19. General System Control

8.19.1. Boot configuration

The DART-MX8M-MINI can be programmed to boot from the following sources:

- Internal source:
  - eMMC Flash memory
  - NAND Memory **(Currently not released!)**
- External source:
  - SD Card

The selection of the boot mode is done via strap options resistors on BOOT_CFG lines, which are latched on POR_B signal rise (values should remain valid 1ms after rise).

ATTENTION

External drivers connected to BOOT_CFG lines should be disabled on during reset (POR_B) on pins used as inputs to the SOM, otherwise they may change the boot option and the SOM will not boot.

8.19.2. Boot Configuration Signals

Table 54: Boot Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.13		BOOT_MODE0		Boot mode bit 0; For normal boot apply 4.7K PD or stronger	SOC.G26
J2.11		BOOT_MODE1		Boot mode bit 1; For normal boot apply 4.7K PU (or stronger) to NVCC_3V3	SOC.G27
J2.61		BOOT_CFG00	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AG15
J2.59		BOOT_CFG01	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AF15
J2.63		BOOT_CFG02	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AG17
J2.62		BOOT_CFG03	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AF17
J2.65		BOOT_CFG04	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AG18
J2.69		BOOT_CFG05	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AF18
J2.66		BOOT_CFG06	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AG19
J2.68		BOOT_CFG07	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AF19
J2.70		BOOT_CFG08	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AG20
J2.67		BOOT_CFG09	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AF20
J2.78		BOOT_CFG10	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AG21
J2.73		BOOT_CFG11	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AF21
J2.74		BOOT_CFG12	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AG22

J2.71		BOOT_CFG13	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AF22
J2.80		BOOT_CFG14	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AG23
J2.76		BOOT_CFG15	6	Pin value latched with rise of POR_B; Set BOOG_CFG value;	SOC.AF23

Table 55 details the boot options for the DART-MX8M-MINI. All other Boot configuration lines can be left floating, as the internal pull down will drive them Low.

Table 55: Boot Options

	External Source	Internal Source
BOOT_CFG10	High	Low
BOOT_CFG12	High	Low
BOOT_CFG13	Low	High

BOOT_CFG11

The i.MX8M-MINI SoC differs from the i.MX8M SoC with regards to BOOT_CFG11 boot configuration strapping. In order for both the DART-MX8M and the DART-MX8M-MINI to be able to boot from same boot source (Internal/External) using the same boot configuration strappings, the boot strapping of BOOT_CFG11 is handled internally on the DART-MX8M-MINI using an on-SOM buffer.

The Buffer, active only on boot time, drives BOOT_CFG11 according to the logic level of J2.71 (SAI1_TXD5) BOOT_CFG13 signal:
When BOOT_CFG13 is Low -> BOOT_CFG11 is driven Low
When BOOT_CFG13 is High -> BOOT_CFG11 is driven High

This fulfills the i.MX8M-MINI SoC datasheet requirement in regards to BOOT_CFG11 signal strapping for supporting External/Internal source boot.

NOTE

Low – Represents pull down or floating.
High – Represents pull up of 4.7KΩ to 1KΩ.
External Source: refers to device connected to SD2 pins e.g. SD card; see section SD2 signals
Internal Source: Refers to the device configured as SOM storage: eMMC or NAND

8.19.3. General System Control Signals

The user must ensure not to drive any pins/function of the SOM before the appropriate IO domain power is up.

NVCC_3V3 SOM output is used to power most of the SOM pins and could be used to control the custom board power. Refer to DART-MX8M CustomBoard schematics for implementation suggestion.

Table 56 details the SOM system control signals.

NOTE

General control signals: ONOFF, PMIC_ON_REQ, PMIC_STBY_REQ and POR_B are powered by NVCC_SNVS_**1V8**; as appose to the DART-MX8M which runs from NVCC_SNVS_**3V3** domain;

Table 56: System Control Signals

PIN#	ALT_NAME	ALT#	NOTES	BALL
J1.20	ONOFF	0	**SOC input with internal PU** **Note: Internal PU on SOM to NVCC_SNVS_1V8** ***In OFF mode***: brief connection to GND causes the internal power management state machine to change state to ON. ***In ON mode***: brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). ***To Force OFF***: approximate 5 second or more connection to GND **Not used leave Floating**	SOC.A25
J1.22	PMIC_ON_REQ	0	**SOC output (OD with PU) controls the PMIC state**; **Note: Internal PU on SOM to NVCC_SNVS_1V8** Open Drain output from SoC which controls the SOM power up/ down sequence; Pulling the signal to GND will force the SOM to power OFF; **External delay on this pin is recommended, see DART-MX8M customBoard schematics for reference.** Can be used to control the custom board power.	SOC.A24
J1.26	PMIC_STBY_REQ	0	**SOC output controls the PMIC state;** **Note: Internal PD on SOM (NVCC_SNVS_1V8 level)** Signal output from SoC controlling it's PMIC; ***Transition 0 to 1:*** Enter Standby ***Transition 1 to 0:*** Wake up from standby Can be used to control custom board power.	SOC.E24
J1.24	POR_B	0	**PMIC output (OD with PU) connected to SOC;** Can be pulled low externally to cause hot reset (Not recommended) **Note: OD output from PMIC; Include 100K PU to NVCC_SNVS_1V8** Signal Asserted from assertion of PMIC_ON_REQ and valid VBAT; will Negates at the end of power up sequence. Could be used to control buffers driving the Configuration pins.	SOC.B24
J2.28	WDOG_B	1	As WDOG_B alternate pin function could be used to initiate power up sequence in case of a watch dog event. See footnote [1];	SOC.AG13

[1] Once the **WDOG** is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon timeout, the WDOG asserts the internal system reset signal, WDOG_RESET_B to the System Reset Controller (SRC). There is also a provision for WDOG signal assertion by timeout counter expiration. There is an option of programmable interrupt generation before the counter actually times out. The time at which the interrupt needs to be generated prior to counter timeout is programmable. There is a power down counter which is enabled out of any reset (POR, Warm/Cold). This counter has a fixed timeout period of 16 seconds, upon which it asserts the WDOG signal.
WDOG runs at 3.3V as part of the GPIO1 bank.

8.20. Power

8.20.1. Power

Table 57: Power Pins

PIN#	ALT_NAME	ALT#	NOTES	BALL
J3.71	VBAT		SOM Power	
J3.73	VBAT		SOM Power	
J3.75	VBAT		SOM Power	
J3.77	VBAT		SOM Power	
J3.79	VBAT		SOM Power	
J3.81	VBAT		SOM Power	
J3.83	VBAT		SOM Power	
J3.85	VBAT		SOM Power	
J3.87	VBAT		SOM Power	
J3.89	VBAT		SOM Power	
J1.15	NVCC_SNVS_1V8		**Power output from SOM; Valid with VBAT.** **Max. 1mA draw allowed;** See footnote [1]	
J1.27	NVCC_3V3		**Power output from SOM;** Rises after last power rail; Can be used to control base board power. **Max. See Section 9.3 for Maximum allowed current;**	
J1.31	NVCC_ENET		**ENET pins group power IN(No "EC") or OUT("EC"):** ***"EC" configuration***: * AR8033 PHY - Outputs 2.5V, ADIN1300 PHY – Outputs 1.8V * Leave Floating! * No current draw allowed.! ***No "EC" configuration:*** Must supply one option (Max. 50mA required) - * RMII uses 1.8 or 3.3V. * RGMII uses 1.8 or 2.5V. * GPIO 1.8V/2.5V/3.3V	SOC.W22
J1.90	NVCC_SD2_1V8_3V3		**Power output from SOM;** Power the SD2 interface IO pins; **Will change 1.8V/3.3V according to SD capabilities.** Use for PU resistor on SD2_CD_B and SD2_CMD lines.	
J3.66	USB1_VBUS	0	USB PHY power pin; 5V tolerant	SOC.F22
J3.26	USB2_VBUS	0	USB PHY power pin; 5V tolerant	SOC.F23

[1] NVCC_SNVS_1V8 power used for SOC internal RTC and SNVS domains, also powers signals controlling the power management of the SOC.
Variscite recommends using an external low power time keeping circuitry which is more power efficient than the SOC RTC core; See DART-MX8M CustomBoard for reference design supported by the BSP.

8.20.2. Ground

Table 58: Ground Pins

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.12		AGND		Audio Ground	
J1.18		GND		Digital Ground	
J1.21		GND		Digital Ground	
J1.30		GND		Digital Ground	
J1.33		GND		Digital Ground	
J1.49		GND		Digital Ground	
J1.52		GND		Digital Ground	
J1.55		GND		Digital Ground	
J1.58		GND		Digital Ground	
J1.61		GND		Digital Ground	
J1.64		GND		Digital Ground	
J1.67		GND		Digital Ground	
J1.70		GND		Digital Ground	
J1.76		GND		Digital Ground	
J1.85		GND		Digital Ground	
J2.18		GND		Digital Ground	
J2.23		GND		Digital Ground	
J2.47		GND		Digital Ground	
J2.53		GND		Digital Ground	
J2.75		GND		Digital Ground	
J2.84		GND		Digital Ground	
J3.9		GND		Digital Ground	
J3.10		GND		Digital Ground	
J3.15		GND		Digital Ground	
J3.21		GND		Digital Ground	
J3.24		GND		Digital Ground	
J3.27		GND		Digital Ground	
J3.33		GND		Digital Ground	
J3.34		GND		Digital Ground	
J3.39		GND		Digital Ground	
J3.45		GND		Digital Ground	
J3.51		GND		Digital Ground	
J3.57		GND		Digital Ground	
J3.63		GND		Digital Ground	
J3.68		GND		Digital Ground	
J3.74		GND		Digital Ground	

8.20.3. Not Connected Pins

Table 59: NC Pins

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.3	EC	NC		With "EC" configuration this pin in Not Connected.	NC_EC
J1.36		NC		Not Connected	NC
J1.39		NC		Not Connected	NC
J1.42		NC		Not Connected	NC
J1.43		NC		Not Connected	NC
J1.44		NC		Not Connected	NC
J1.54		NC		Not Connected	NC
J1.56		NC		Not Connected	NC
J1.63		NC		Not Connected	NC
J1.65		NC		Not Connected	NC
J1.66		NC		Not Connected	NC
J1.68		NC		Not Connected	NC
J1.72		NC		Not Connected	NC
J2.15		NC		Not Connected	NC
J2.17		NC		Not Connected	NC
J2.19		NC		Not Connected	NC
J2.21		NC		Not Connected	NC
J2.25		NC		Not Connected	NC
J2.27		NC		Not Connected	NC
J2.29		NC		Not Connected	NC
J2.31		NC		Not Connected	NC
J2.33		NC		Not Connected	NC
J2.35		NC		Not Connected	NC
J2.37		NC		Not Connected	NC
J2.39		NC		Not Connected	NC
J2.41		NC		Not Connected	NC
J2.43		NC		Not Connected	NC
J2.45		NC		Not Connected	NC
J2.49		NC		Not Connected	NC
J2.51		NC		Not Connected	NC
J3.2	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
J3.4	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
J3.5	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
J3.6	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
J3.7	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
J3.8	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
J3.11	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
J3.13	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
J3.17	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
J3.19	No LD	NC		Pin not connected with No "LD" configuration!	NC_No_LD
J3.35		NC		Not Connected	NC
J3.37		NC		Not Connected	NC
J3.41		NC		Not Connected	NC
J3.43		NC		Not Connected	NC
J3.53		NC		Not Connected	NC
J3.55		NC		Not Connected	NC
J3.59		NC		Not Connected	NC
J3.61		NC		Not Connected	NC
J3.69		NC		Not Connected	NC
J3.70		NC		Not Connected	NC
J3.72		NC		Not Connected	NC
J3.76		NC		Not Connected	NC
J3.78		NC		Not Connected	NC
J3.80		NC		Not Connected	NC
J3.82		NC		Not Connected	NC

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.84		NC		Not Connected	NC
J3.86		NC		Not Connected	NC
J3.88		NC		Not Connected	NC
J3.90		NC		Not Connected	NC

9. Electrical specifications

9.1. Absolute maximum ratings

Table 60: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VBAT	-0.3	5.5	V
USB_VBUS	-0.3	5.25	V

9.2. Operating conditions

Table 61: Operating Ranges

Parameter	Min.	Typ.	Max.	Unit
VBAT	3.5	3.7	5	V
USB_VBUS	4.75	5	5.25	V

9.3. NVCC_3V3 output power supply capabilities

Table 62: NVCC_3V3 Maximum Current

Parameter	NVCC_3V3 Maximum current	Units
VBAT < 3.7V	100	mA
VBAT > 3.7V	300	mA

9.4. Power consumption

Table 63: DART-MX8M-MINI Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.52V	0.67A	2.36W	Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz
Run	3.52V	0.61A	2.15W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	3.52V	0.33A	1.16W	Linux up
VFHD video playback	3.52V	0.46A	1.62W	On 800x400 LCD
Off (RTC)	3.56V	0.256mA	<1mW	All power rails are Off, only Internal SoC RTC is powered
Suspend	3.52V	6.95mA	~25mW	Memory in retention mode [1]

[1] NOTE: Tested with IT module grade having 2GB DRAM

9.5. Peripheral Voltage Levels

Most of the peripheral interface lines used as inputs or output to the DART-MX8M-MINI uses 3.3V LVCMOS levels, except the following interfaces: SD2, ENET, MDIO/MDC, PCIe, USB, MIPI-DSI, MIPI-CSI, QSPI-A. **Interfaces with "_1V8" in their name runs at 1.8V**; Do not drive these pins with higher voltage.

***PCIe/USB/MIPI-DSI/ MIPI-CSI*:** Interfaces follow a different standard since they are high-speed signals.

SD2: (SDIO lines) interface IOs will change voltage between 3.3V and 1.8V depending on the SD card capabilities.

ENET: interface available in case SOM is ordered **without "EC"** configuration. IOs will run according to the power fed to NVCC_ENET (J1.31) (1.8V/2.5V/3.3V).

MDIO/MDC:
MDIO, MDC signals (pins J1.11, J1.13 respectively) are referenced to VDD_ENET rail.
In case a SOM is ordered **with "EC"** Configuration, VDD_ENET is produced internally on SOM and is set to 1.8V or 2.5V depending on the SOM revision:
In SOM revisions up to v1.2 which use ETH PHY AR8033 - VDD_ENET is set to 2.5V
In SOM revisions v1.3 and higher which use ETH PHY ADIN1300 - VDD_ENET is set to 1.8V

CODEC: DMIC interface available with "AC" configuration is a mixed voltage; DMIC_CLK outputs at 3.3V levels, but the DMIC_DATA input tolerates 1.8V levels only.

10. Environmental Specifications

Table 64: Environmental Specifications

Parameter	Min	Max
Commercial Operating Temperature Range	0°C	70°C
Extended Operating Temperature Range	-25°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Prediction Method Model: Telcordia Technologies Special Report SR-332, Issue 4 50°C, GB	> 5737 Khrs	

NOTE

Extended and industrial temperature ranges based only on the operating temperature grade of the SOM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

11. Mechanical Drawings

11.1. Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

NOTE

The size and footprint of SOM 90-pin connectors Hirose P/N: DF40C-90DP-0.4V(51) are different from mating carrier board 90-pin connectors (see section 7.1).

To ensure correct positioning of the carrier board connectors and holes please refer to VAR-DT8MCustomBoard DXF available here (under documentation tab): http://www.variscite.com/products/single-board-computers/var-dt8mcustomboard

It is recommended NOT to place any components under the SOM.

11.2. Standoffs

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

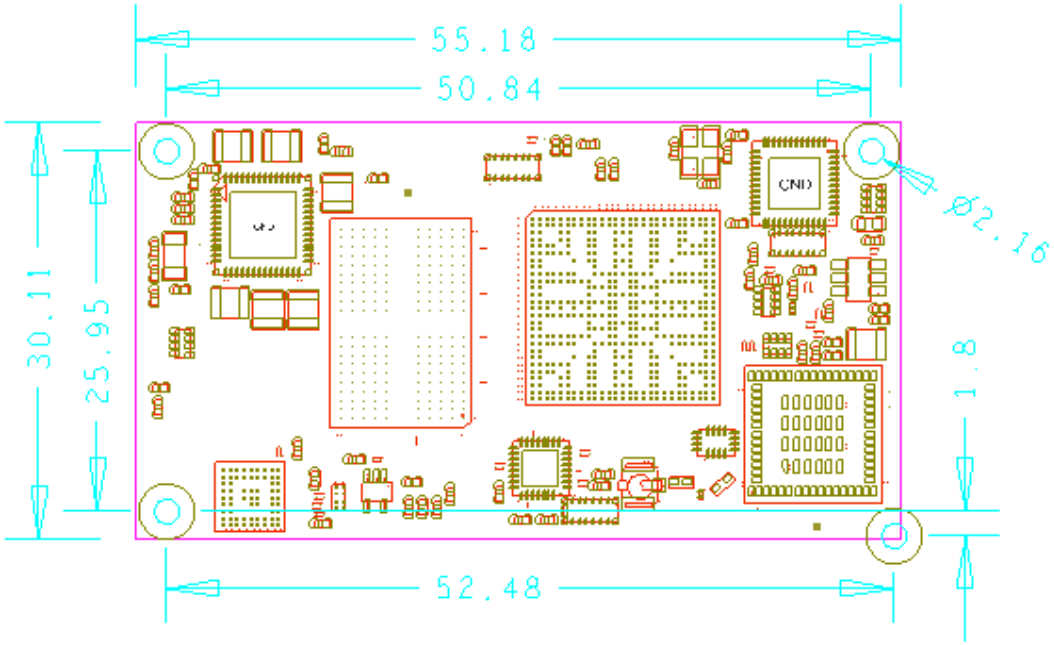
Manufacturer: **MAC8**

PN: **TH-1.6-1.5-M2**

Link: http://www.mac8japan.com/English%20Catalog/TH1.6%20Series-2.pdf

11.3. SOM Dimensions

Figure 5 illustrates the top view of the DART-MX8M-MINI size and mounting holes relative location. **All dimensions given in millimeter and [mils] units**.



UNITS: Milimeters

Figure 5: DART-MX8M-MINI Top View Mechanics

Dimensioning:

Width: 55.18 mm

Length: 30.11 mm

Height: 5.13 mm (Carrier PCB to highest component on SOM)

11.3.1. CAD Files

CAD files are available for download at http://www.variscite.com/

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