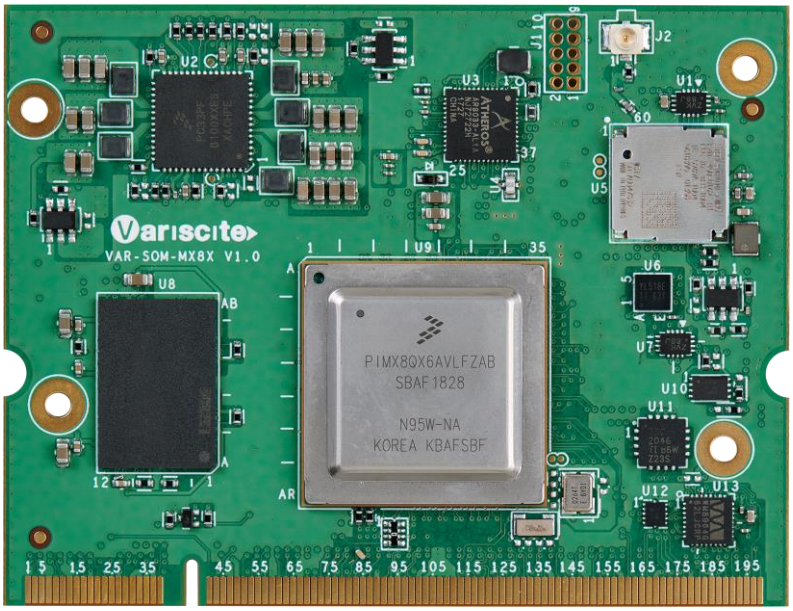
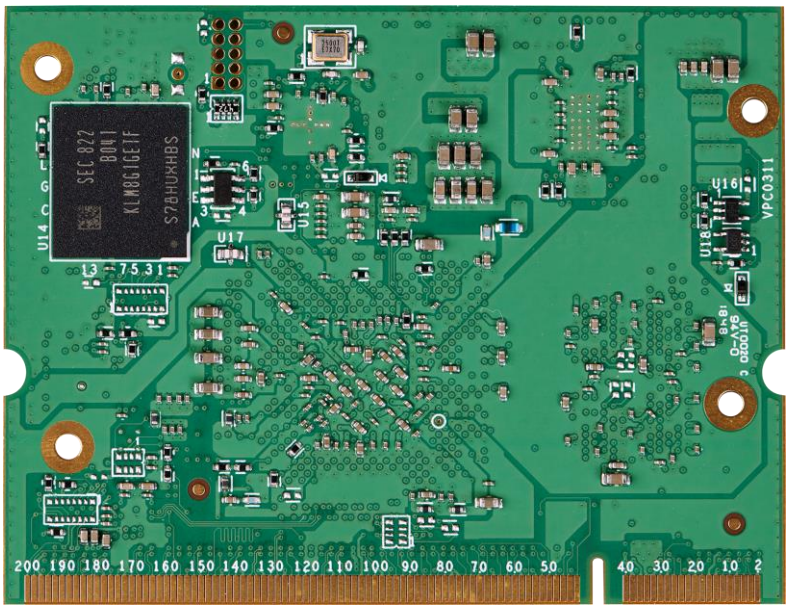
VARISCITE LTD.

# VAR-SOM-MX8X V1.x Datasheet

## NXP i.MX 8QXP™/8DXP™ - based System-on-Module



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# 1. Document Revision History

| Revision | Date | Notes |
|---|---|---|
| 1.0 | Jan 27, 2019 | Initial - Preliminary |
| 1.01 | Apr 01, 2019 | Updated sections 9.4,10,11<br>Updated sections 7.4,9.2 Pins 31,33,35 |
| 1.02 | Jun 03, 2019 | Updated sections 4.3, 9.4 |
| 1.03 | Jul 18, 2019 | Updated block diagram section 4.3 |
| 1.04 | Oct 16, 2019 | Updated section 11.3 |
| 1.05 | Nov 11, 2021 | Added EEPROM section 5.8, Updated EEPROM in block diagram section 4.3 |
| 1.06 | Apr 25, 2022 | Added Ethernet PHY ADIN1300 – Updated sections 4.3, 5.6, 7.4, 8.3<br>Updated section 5.3<br>Following NXP iMX8QXP datasheet Rev 4:<br>Removed MLB I/F from sections 4.3, 7.5, 8<br>Updated Table 70<br>Updated section 13 SMT spacer P/N |
| 1.07 | May 1, 2022 | Updated sections: 4.2, 5.4, 8.4 |
| 1.08 | May 17, 2022 | Corrected note for pin 98<br>Following NXP iMX8QXP datasheet Rev 4:<br>Removed Tamper I/F from sections 4.3, 7.5, 8<br>Updated note on PCIE sections 7.4, 8.10<br>Updated section 13 SMT Heat spreader P/N |
| 1.09 | Jun 15, 2022 | Table 1 – Corrected description for EC assembly option |
| 1.10 | Sep 14, 2022 | Updated section 13.2 |
| 1.11 | Jan 3, 2023 | Updated Key Features section 5.4 |
| 1.12 | Feb 26, 2023 | Updated section 12<br>Updated the eMMC sections 4.2, 5.2 |

# 2. Table of Contents

# 3. List of Tables

# 4. Overview

## 4.1 General Information

The VAR-SOM-MX8X offers a high-performance processing for a low-power System-on-Module. The product is based on the NXP i.MX 8QuadXPlus and 8DualXPlus processors comprehensive multimedia device targeting high-end automotive and Infotainment market segments.

The i.MX 8X processors consist of three to five ARM® cores (two to four ARM Cortex®-A35 and one Cortex-M4F). All devices include separate GPU and VPU subsystems as well as a failover-ready display controller.
Advanced multicore audio processing is supported by the ARM cores and a high performance Tensilica® HiFi 4 DSP for pre- and post-audio processing as well as voice recognition.
The i.MX 8X Family supports up to three displays with multiple display output options, including parallel, MIPI-DSI, and LVDS.

A wide range of peripheral I/Os such as CAN, parallel or MIPI CSI camera input, Gigabit Ethernet, USB 2.0 OTG, USB 3.0, ADC, and PCIe 3.0 provide impressive flexibility.

The VAR-SOM-MX8X provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

- Symphony-Board – evaluation board
  - ✓ Carrier Board, compatible with VAR-SOM-MX8X
  - ✓ Schematics
- VAR-DVK-MX8X full development kit, including:
  - ✓ Symphony-Board
  - ✓ VAR-SOM-MX8X
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

Contact Variscite support services for further information: mailto:support@variscite.com.

## 4.2 Feature Summary

- NXP i.MX8QXP/ i.MX8DXP series SOC
  - 4x/2x Cortex A35 up to @ 1.2 GHz
  - 1x Cortex M4 @ 264 MHz
  - Up to 4GB LPDDR4 RAM @ 1200Mhz
  - 8-bit up to 128GB eMMC boot and storage
- Display Support
  - 2x MIPI-DSI/LVDS interface 4-lane each, up to 1080p60
  - 24-bit parallel LCD up to 720p60
- Networking
  - 2x 10/100/1000 Mbit/s Ethernet Interface
  - Certified Wi-Fi 802.11 ac/a/b/g/n
  - Bluetooth: 5.2/BLE
- Camera
  - 1x MIPI CSI – CMOS Serial camera Interface 4 lanes.
  - 1x CSI – CMOS Parallel camera 8-bit/10-bit Interface.
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - 7x Digital audio (SAI, ESAI, SPDIF, MQS)
- USB
  - 1x USB 3.0/2.0 OTG
  - 1x USB 2.0 Host/Device
- Other Interfaces
  - SDIO/MMC
  - 1x PCIe v3.0
  - Resistive touch controller
  - Serial interfaces (LPSPI, QSPI, I2C, UART, CAN, JTAG)
  - ADC 6 x 12-bit
  - GPIOs
- Single power supply: 3.3V
- Dimensions (W x L x H): 67 mm x 51.6 mm x 4.87mm
- Industrial temperature range -40°C to 85°C

## 4.3 Block Diagram

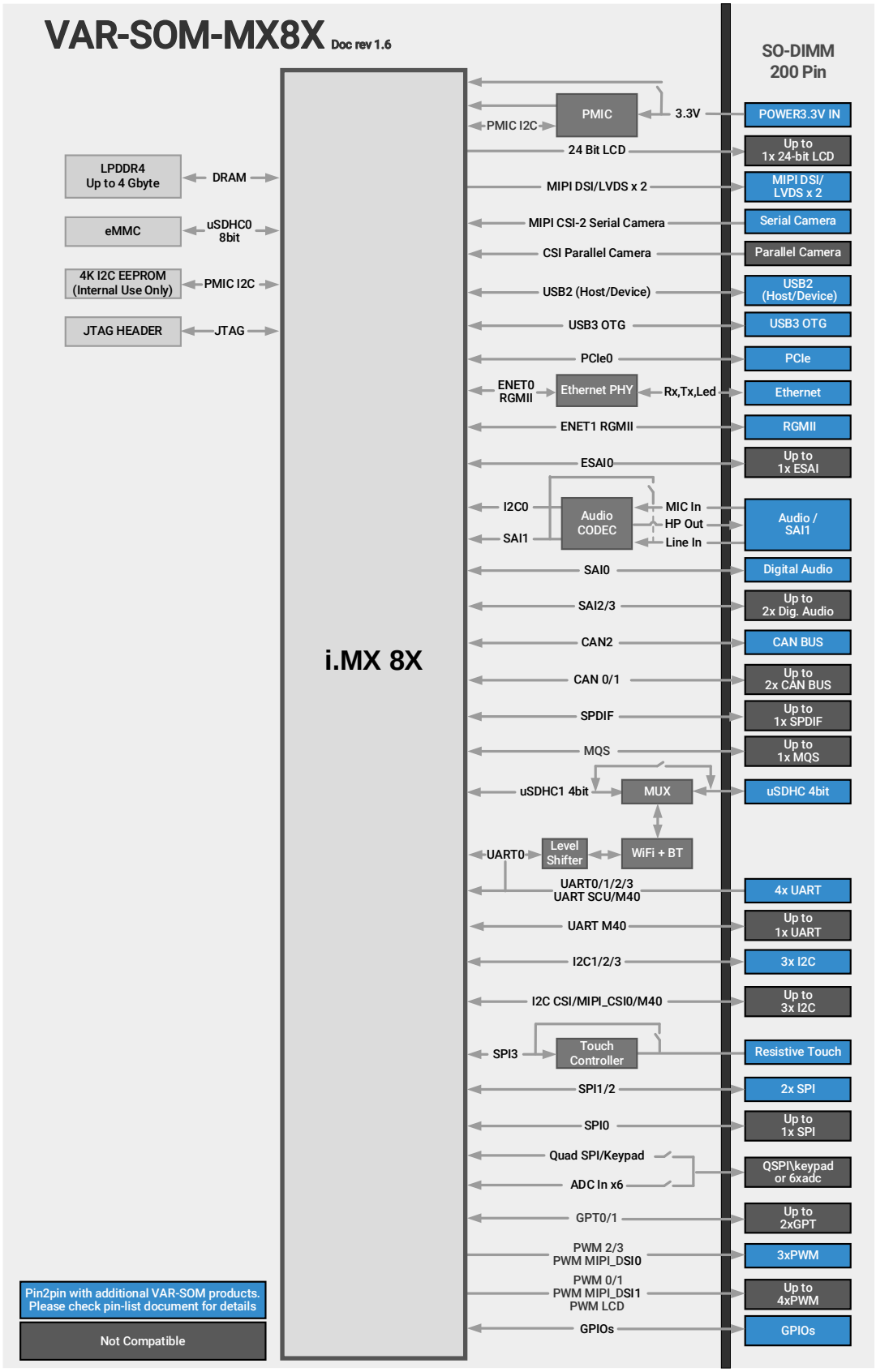



*Figure 1 : VAR-SOM-MX8X Block Diagram*

# 5. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-MX8X.

## 5.1 NXP i.MX8QXP/i.MX8DXP

### 5.1.1 Overview

The VAR-SOM-MX8X offers a high-performance processing for a low-power System-on-Module. The product is based on the NXP i.MX 8QuadXPlus and i.MX 8DualXPlus. These devices are fully comprehensive multimedia application processors targeting mid-range automotive and industrial market segments. The flexibility of the architecture allows for use in a wide variety of general embedded applications. These devices are designed to achieve both high performance and low power consumption. The computing power of these chips lies on the power efficient quad/dual (Cortex-A35 cluster. The Cortex-A35 provides full 64-bit ARMv8-A support while maintaining seamless backwards compatibility with 32-bit ARMv7-A software.

Graphics processing is handled by a dedicated Graphics Processing Unit (GPU) supporting some of the latest graphic APIs. Video is managed by a dedicated video engine decoding formats, H.265 HEVC (Main Profile) up to 4K30 and H.264 up to 1080p60, as well as encoding up to 1080p30.

The i.MX 8QuadXPlus and i.MX 8DualXPlus provides additional computing resources and peripherals:

- A dedicated System Control Unit (SCU) and a dedicated Security subsystem which provides Secure Boot features and cryptographic acceleration
- An Audio DMA subsystem with a wide range of audio and general-purpose interfaces
- A general-purpose Cortex-M4 with its own set of peripherals
- A large set of peripherals that are commonly used in automotive and industrial markets
- A Tensilica Hi-Fi 4 DSP geared for efficient execution of audio and voice codecs and pre- and post-processing modules to offload the ARM core

### 5.1.2 i.MX8X Block Diagram

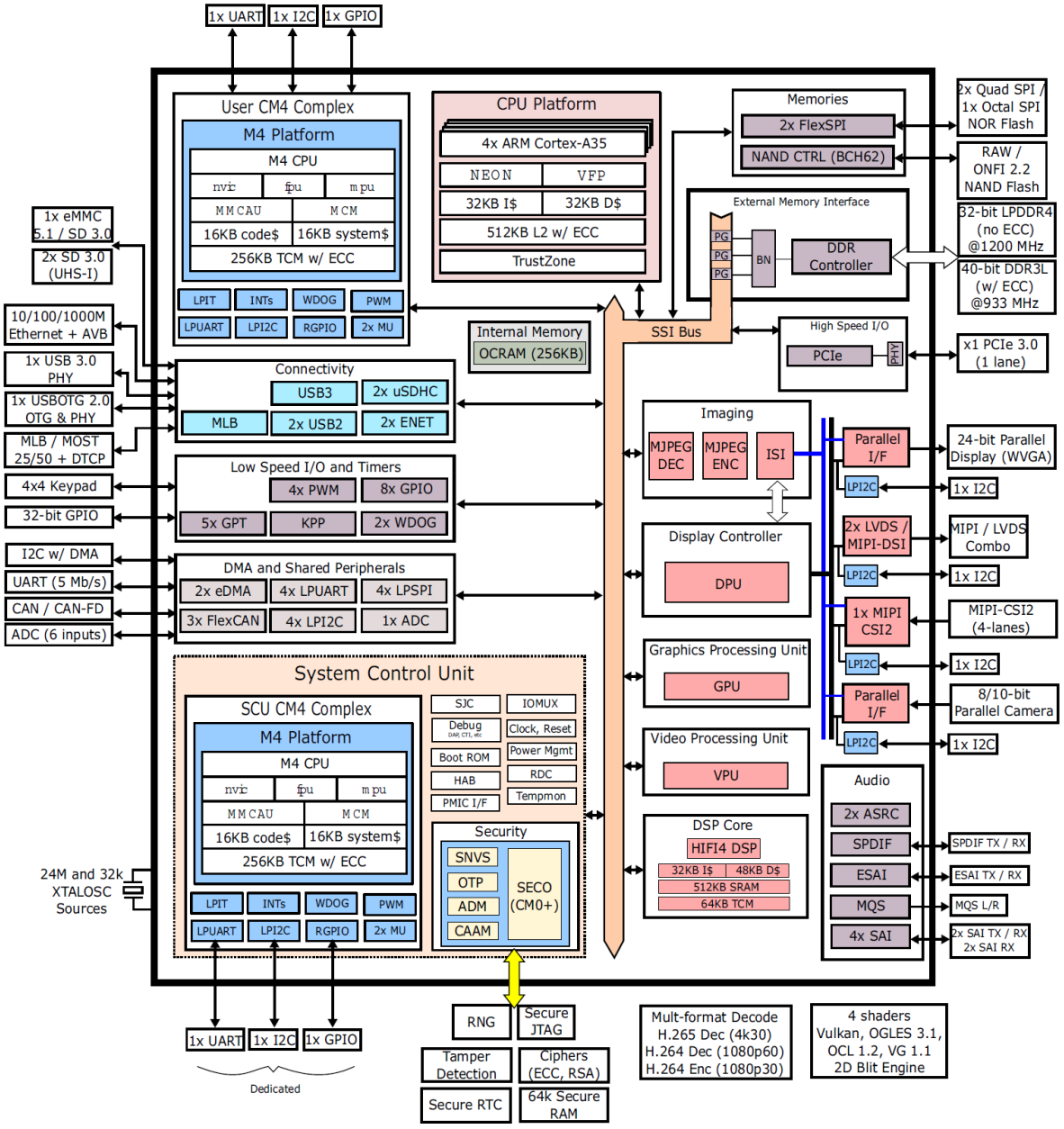



***Figure 2 : i.MX 8QuadXPlus/8DualXPlus Block Diagram***

### 5.1.3 ARM Cortex-A35 Platform

The i.MX8QXP/ i.MX8DXP family Applications Processors are based on the ARM Cortex-A35 platform, which has the following features:

- 32KB of L1 instruction cache per CPU core
- 32KB of L1 data cache per CPU core
- 512KB of L2 unified cache shared by the four CPUs with ECC protection mechanism (Single Error Correction and Double Error Detection)
- Advanced SIMD and FP
- Crypto acceleration

### 5.1.4 Arm Cortex-M4 Platform

Cortex-M4 core platform includes the following features:

- Cortex M4 Processor:
    - 16KB of Code Bus Cache with parity protection
    - 16KB of System Bus Cache with parity protection
    - 256KB of Tightly Coupled Memory with ECC
    - FPU (Floating Point Unit)
    - MPU (Memory Protection Unit)
    - Support for exclusive access on the system bus
    - MMCAU (Crypto Acceleration Unit)
    - MCM (Miscellaneous Control Module)
    - Nested Vector Interrupt Controller (NVIC)
- 2x MU (Messaging Unit)
- 1x LPIT (Low-power Periodic Interrupt Timer)
- 1x Watch dog
- 1x Wakeup Interrupt Controller (WIC)
- 1x GPIO module with 32 GPIO
- 1x UART with HW flow control
- 1x TPM (Timer PWM Module) with 2 channels

## 5.2 Memory

### 5.2.1 RAM

The VAR-SOM-MX8X is available with up to 4 GB of LPDDR4 memory capable of running up to 2400MTS.

### 5.2.2 Non-volatile Storage Memory

The VAR-SOM-MX8X is available with a non-volatile storage memory with optional densities. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.
The VAR-SOM-MX8X can arrive with up to 128GB MLC eMMC

## 5.3 Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

## 5.4 Wi-Fi + BT (LWB5™)

The VAR-SOM-MX8X contains LSR's pre-certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 5.2 wireless connectivity.

The VAR-SOM-MX8X module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

Key Features:

- IEEE 802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, and BLE 5.2
- U.F.L connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- Industrial operating Temperature Range: -40 to +85

## 5.5 PMIC

The VAR-SOM-MX8X features Freescale/NXP's PF8100 chip as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX8QXP/ i.MX8DXP series of application processors. The PF8100 regulates all power rails required on SOM from a single 3.3V power supply.
The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

## 5.6 Dual Ethernet MAC and on-board 10/100/1000 Mbps Ethernet Transceiver

The SOM can be ordered with an Integrated Ethernet Transceiver connected to ENET0 RGMII signals, Qualcomm Atheros AR8033 or Analog Devices ADIN1300.
Please contact sales@variscite.com for inquiries about P/N assembled on your SOM.

An additional Ethernet Transceiver can be connected to ENET1 signals exported from SOM connector pins. Connecting an external Ethernet Transceiver requires a single 1.8/2.5V power supply for RGMII interfaces or 3.3V for RMII interface.

### 5.6.1 Qualcomm Atheros AR8033 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- 1000BASE-T PCS and auto-negotiation with next page support
- Green ETHOS power saving modes with internal automatic DSP power saving scheme
- IEEE 802.3az EEE
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Robust operation over up to 140 meters of CAT5 cable
- Automatic Channel Swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction ν IEEE 802.3u compliant auto-negotiation
- Jumbo frame supports up to 10 KB (full-duplex)
- Integrated termination circuitry at the line side

### 5.6.2 Analog Devices ADIN1300 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.
- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover

- Autonegotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

## 5.7 Resistive Touch controller (TSC2046)

The VAR-SOM-MX8X features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

## 5.8 EEPROM

The SOM uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters.
This EEPROM is connected to SCU I2C bus and intended only for holding the above information.
The SOM may not boot if the contents of EEPROM device are corrupted.

# 6. VAR-SOM-MX8X Hardware Configuration

The table below lists the Hardware configurations options orderable for the VAR-SOM-MX8X.

***Table 1 Hardware Configuration Options***

| Option | Description |
|---|---|
| *EC* | Ethernet PHY assembled on SOM |
| *AC* | Audio Codec assembled on SOM |
| *WBD* | Dual band Wi-Fi and BT/BLE combo assembled on SOM |
| *TP* | Resistive Touch controller assembled on SOM |
| *ADC* | ADC balls exported via SOM connector pins |

Note: Other orderable options are available and are not part of this datasheet.
Please refer to Variscite official website for full list of configuration options.

# 7. External Connectors

## 7.1 Board to Board Connector

The VAR-SOM-MX8X exposes a 200-pin SO-DIMM connector.

- The recommended mating connectors for baseboard interfacing are:
  1. Concraft - 0701A0BE52E
  2. Tyco Electronics -1565917-4

## 7.2 Wi-Fi & BT Connector

In Modules with Wi-Fi "WBD" Configuration - a combined Wi-Fi + BT antenna connector is assembled.

- Connector type: U.FL JACK connector
- Cable and antenna shall have a 50 Ohm characteristic impedance

## 7.3 JTAG Header

In addition to the 200-pin SO-DIMM interface, the SOM exposes JTAG interface via an optional 10-pin header.

## 7.4 VAR-SOM-MX8X Connector Pin-out

***Table 2: VAR-SOM-MX8X J1 Pinout***

| Pin # | Assembly | Pin Name | Notes | GPIO | Ball |
|---|---|---|---|---|---|
| 1 | | GND | | | |
| 2 | | GND | | | |
| 3 | EC | ETH0_MDI_A_P | | | AR8033.11/ ADIN1300.12 |
| 4 | EC | ETH0_MDI_C_P | | | AR8033.17/ ADIN1300.16 |
| 5 | EC | ETH0_MDI_A_M | | | AR8033.12/ ADIN1300.13 |
| 6 | EC | ETH0_MDI_C_M | | | AR8033.18/ ADIN1300.17 |
| 7 | | GND | | | |
| 8 | | GND | | | |
| 9 | EC | ETH0_MDI_B_P | | | AR8033.14/ ADIN1300.14 |
| 10 | EC | ETH0_MDI_D_P | | | AR8033.20/ ADIN1300.18 |
| 11 | EC | ETH0_MDI_B_M | | | AR8033.15/ ADIN1300.15 |
| 12 | EC | ETH0_MDI_D_M | | | AR8033.21/ ADIN1300.19 |
| 13 | | GND | | | |
| 14 | | GND | | | |
| 15 | EC | ETH0_LED_ACT | Ethernet PHY Activity LED, active low | | AR8033.23/ ADIN1300.21 |
| 16 | EC | ETH0_LED_LINK_10_100_1000 | Ethernet PHY Link LED, active low | | AR8033.24_26/ ADIN1300.26 via inverting FET |
| 17 | | MIPI_DSI0_GPIO0_00 | | GPIO1_IO27 | AD32 |
| 18 | AC | DMIC_CLK | Digital microphone clock output | | WM8904CGEFL.1 |
| 18 | No AC | FLEXCAN1_RX | Available in SOM without AC | GPIO1_IO17 | AA33 |
| 19 | | GND | | | |
| 20 | AC | DMIC_DATA | Digital microphone data input | | WM8904CGEFL.27 |
| 20 | No AC | MCLK_OUT0 | Available in SOM without AC | GPIO0_IO20 | L29 |
| 21 | | SPI0_CS0 | | GPIO1_IO08 | R33 |
| 22 | | SPI0_CS1 | | GPIO1_IO07 | R35 |
| 23 | | SAI1_RXD | | GPIO0_IO29 | M32 |
| 24 | | SPI0_SDO | | GPIO1_IO06 | R31 |
| 25 | | SPI0_SCK | | GPIO1_IO04 | P30 |
| 26 | | SPI0_SDI | | GPIO1_IO05 | P34 |
| 27 | | GND | | | |
| 28 | | GND | | | |
| 29 | | MIPI_CSI0_MCLK_OUT | | GPIO3_IO04 | AN25 |

| Pin # | Assembly | Pin Name | Notes | GPIO | Ball |
|---|---|---|---|---|---|
| 30 | | ENET0_MDIO | Pin alternate function cannot be changed when using SOM with EC assembled | GPIO5_IO10 | B32 |
| 31 | | NC | | | |
| 32 | | VBAT | | | |
| 33 | | NC | | | |
| 34 | | VBAT | | | |
| 35 | | NC | | | |
| 36 | | LICELL | RTC back-up battery 1.8V/3.0V/3.3V supply voltage input | | PF8100.46 |
| 37 | | GND | | | |
| 38 | | VDD_ENET1_1P8_2P5_3P3_IN | VAR-SOM-MX8X 1.8V/2.5V/3.3V supply voltage input.<br><br>The following SOM pins are referenced to this voltage:<br>40,54,55,56,57,71,73,81,96,113,120,122,177<br><br>When using the above pins for alternate functions of ENET1:<br>• For RMII - connect to 3.3V<br>• For RGMII - connect to 1.8V/2.5V | | N25 |
| 39 | | SPI2_CS0 | | GPIO1_IO00 | P28 |
| 40 | | SPDIF0_EXT_CLK | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO12 | E35 |
| 41 | | MCLK_IN0 | | GPIO0_IO19 | G35 |
| 42 | | USB_SS3_TC1 | Pin Used for Boot mode setting,<br>Please see Boot Configuration section. | GPIO4_IO04 | H14 |
| 43 | | SPI2_SCK | | GPIO1_IO03 | R29 |
| 44 | | FLEXCAN2_TX | | GPIO1_IO20 | AA31 |
| 45 | | SPI2_SDO | | GPIO1_IO01 | P32 |
| 46 | | FLEXCAN2_RX | | GPIO1_IO19 | AB34 |
| 47 | | GND | | | |
| 48 | | CSI_EN | | GPIO3_IO02 | AP28 |
| 49 | | SW_3P3 | SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply.<br>Connect to pin 38 in case of 3.3V supply. | | |
| 50 | | FLEXCAN0_RX | Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | GPIO1_IO15 | Y34 |
| 51 | | FLEXCAN0_TX | Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | GPIO1_IO16 | Y32 |

| Pin # | Assembly | Pin Name | Notes | GPIO | Ball |
|---|---|---|---|---|---|
| 52 | | UART0_TX | Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | GPIO1_IO22 | AA29 |
| 53 | | UART0_RX | Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | GPIO1_IO21 | AB32 |
| 54 | | ESAI0_TX1 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO05 | B34 |
| 55 | | ESAI0_SCKT | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO03 | E31 |
| 56 | | ESAI0_FST | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO01 | G29 |
| 57 | | ESAI0_TX0 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO04 | D32 |
| 58 | | GND | | | |
| 59 | | GND | | | |
| 60 | | USDHC1_CLK | Not connected when Wi-Fi is enabled | GPIO4_IO23 | G23 |
| 61 | | USDHC1_DATA2 | Not connected when Wi-Fi is enabled | GPIO4_IO27 | D26 |
| 62 | | USDHC1_DATA0 | Not connected when Wi-Fi is enabled | GPIO4_IO25 | A27 |
| 63 | | USDHC1_DATA1 | Not connected when Wi-Fi is enabled | GPIO4_IO26 | B26 |
| 64 | | USDHC1_CMD | Not connected when Wi-Fi is enabled | GPIO4_IO24 | C25 |
| 65 | | USDHC1_DATA3 | Not connected when Wi-Fi is enabled | GPIO4_IO28 | E25 |
| 66 | | GND | | | |
| 67 | | GND | | | |
| 68 | | UART1_CTS_B | | GPIO0_IO24 | K32 |
| 69 | | UART1_RTS_B | | | N29 |
| 70 | | CSI_MCLK | | GPIO3_IO01 | AM26 |
| 71 | | ESAI0_TX2_RX3 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO06 | K28 |
| 72 | | ENET0_REFCLK_125M_25M | | GPIO5_IO09 | F28 |
| 73 | | ESAI0_TX4_RX1 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO08 | F32 |
| 74 | | ENET0_MDC | Pin alternate function cannot be changed when using SOM with EC assembled | GPIO5_IO11 | D30 |
| 75 | | SAI0_TXFS | | GPIO0_IO28 | L33 |
| 76 | | GND | | | |
| 77 | | SAI0_TXC | | GPIO0_IO26 | J35 |
| 78 | | GND | | | |
| 79 | | CSI_RESET | | GPIO3_IO03 | AR27 |
| 80 | | USDHC1_CD_B | | GPIO4_IO22 | E23 |
| 81 | | ESAI0_TX3_RX2 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO07 | C33 |
| 82 | | USDHC1_WP | | GPIO4_IO21 | D24 |

| Pin # | Assembly | Pin Name | Notes | GPIO | Ball |
|---|---|---|---|---|---|
| 83 | | SCU_GPIO0_00 | Pin is routed via on SOM buffer, set as Input by default.<br>Pin direction can be controlled by GPIO1_26:<br>Low - Output from SoC<br>High - Input to SoC | GPIO2_IO03 | AF28 |
| 84 | | CSI_PCLK | | GPIO3_IO00 | AK26 |
| 85 | | SCU_GPIO0_01 | Pin is routed via on SOM buffer set as Output by default.<br>Pin direction can be controlled by GPIO1_25:<br>Low - Output from SoC<br>High - Input to SoC | | AH30 |
| 86 | | QSPI0B_SS1_B | | GPIO3_IO24 | AJ9 |
| 87 | | USB_SS3_TC2 | | GPIO4_IO05 | G15 |
| 88 | | USB_SS3_TC0 | | GPIO4_IO03 | F14 |
| 89 | | GND | | | |
| 90 | | MIPI_DSI1_GPIO0_01 | | GPIO2_IO00 | AF34 |
| 91 | | USB_SS3_RX_N | | | B18 |
| 92 | | MIPI_DSI1_GPIO0_00 | | GPIO1_IO31 | AD30 |
| 93 | | USB_SS3_RX_P | | | A19 |
| 94 | | USB_OTG2_ID | | | F16 |
| 95 | | GND | | | |
| 96 | | ESAI0_FSR | Referenced to pin 38 supply (1.8V/2.5/3.3V) | | F30 |
| 97 | | USB_SS3_TX_P | | | B16 |
| 98 | | POR_B_3V3 | System Reset Input. Active on falling edge. A logic low ‘0’ on this pin will reset the system. | | |
| 99 | | USB_SS3_TX_N | | | A15 |
| 100 | | PCIE_REFCLK100M_N | PCIe compliant 100MHz reference clock. Can be exported from SOM or input to the SOM.<br><br>The internal PCIe reference clock is not spread spectrum capable. For PCIe Gen 3.0 or EMC/EMI sensitive applications, it is recommended to connect to an external HCSL-compatible clock source. | | D12 |
| 101 | | GND | | | |
| 102 | | PCIE_REFCLK100M_P | PCIe compliant 100MHz reference clock. Can be exported from SOM or input to the SOM.<br><br>The internal PCIe reference clock is not spread spectrum capable. For PCIe Gen 3.0 or EMC/EMI sensitive applications, it is recommended to connect to an external HCSL-compatible clock source. | | E11 |

| Pin # | Assembly | Pin Name | Notes | GPIO | Ball |
|---|---|---|---|---|---|
| 103 | | VBAT | | | |
| 104 | | USB_OTG1_VBUS | USB Host VBUS (5V) input | | H18 |
| 105 | | VBAT | | | |
| 106 | | USB_OTG2_VBUS | USB OTG VBUS (5V) input | | H16 |
| 107 | | VBAT | | | |
| 108 | | USB_OTG1_DN | | | E19 |
| 109 | | VBAT | | | |
| 110 | | USB_OTG1_DP | | | D18 |
| 111 | | VBAT | | | |
| 112 | | GND | | | |
| 113 | | ESAI0_SCKR | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO02 | H28 |
| 114 | | USB_OTG2_DN | | | D16 |
| 115 | | UART2_RX | | GPIO1_IO24 | AD34 |
| 116 | | USB_OTG2_DP | | | E17 |
| 117 | | QSPI0B_SS0_B | | GPIO3_IO23 | AH10 |
| 118 | | GND | | | |
| 119 | | MIPI_CSI0_DATA0_P | | | AP22 |
| 120 | | SPDIF0_TX | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO11 | D34 |
| 121 | | MIPI_CSI0_DATA0_N | | | AM22 |
| 122 | | SPDIF0_RX | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO10 | G31 |
| 123 | | MIPI_CSI0_DATA1_N | | | AM20 |
| 124 | | UART1_TX | | GPIO0_IO21 | H34 |
| 125 | | MIPI_CSI0_DATA1_P | | | AP20 |
| 126 | | GND | | | |
| 127 | | MIPI_CSI0_DATA2_P | | | AR23 |
| 128 | | PCIE0_TX0_N | | | A9 |
| 129 | | MIPI_CSI0_DATA2_N | | | AN23 |
| 130 | | PCIE0_TX0_P | | | B10 |
| 131 | | MIPI_CSI0_DATA3_N | | | AN19 |
| 132 | | GND | | | |
| 133 | | MIPI_CSI0_DATA3_P | | | AR19 |
| 134 | | PCIE0_RX0_P | | | A13 |
| 135 | | MIPI_CSI0_CLK_P | | | AR21 |
| 136 | | PCIE0_RX0_N | | | B12 |
| 137 | | MIPI_CSI0_CLK_N | | | AN21 |
| 138 | | GND | | | |
| 139 | | GND | | | |
| 140 | No ADC | QSPI0B_DATA2 | | GPIO3_IO20 | AJ11 |

| Pin # | Assembly | Pin Name | Notes | GPIO | Ball |
|---|---|---|---|---|---|
| 140 | ADC | ADC_IN0 | Available in SOM with ADC (referenced to 1.8V) | GPIO1_IO10 | U35 |
| 141 | No ADC | QSPI0B_DATA1 | | GPIO3_IO19 | AL9 |
| 141 | ADC | ADC_IN2 | Available in SOM with ADC (referenced to 1.8V) | GPIO1_IO12 | V32 |
| 142 | No ADC | QSPI0B_DATA0 | | GPIO3_IO18 | AM10 |
| 142 | ADC | ADC_IN1 | Available in SOM with ADC (referenced to 1.8V) | GPIO1_IO09 | U33 |
| 143 | No ADC | QSPI0B_DATA3 | | GPIO3_IO21 | AM8 |
| 143 | ADC | ADC_IN3 | Available in SOM with ADC (referenced to 1.8V) | GPIO1_IO11 | V30 |
| 144 | | GND | | | |
| 145 | No ADC | QSPI0B_DQS | | GPIO3_IO22 | AK10 |
| 145 | ADC | ADC_IN5 | Available in SOM with ADC (referenced to 1.8V) | GPIO1_IO13 | V34 |
| 146 | | SCU_BOOT_MODE1 | Pin Used for Boot mode setting, Please see Boot Configuration section. (referenced to 1.8V) | | AK32 |
| 147 | No ADC | QSPI0B_SCLK | | GPIO3_IO17 | AR11 |
| 147 | ADC | ADC_IN4 | Available in SOM with ADC (referenced to 1.8V) | GPIO1_IO14 | W29 |
| 148 | | CSI_D04 | | | AN29 |
| 149 | | GND | | | |
| 150 | | CSI_D00 | | | AK28 |
| 151 | | CSI_D07 | | | AM28 |
| 152 | | CSI_D01 | | | AL29 |
| 153 | | CSI_D06 | | | AJ25 |
| 154 | | CSI_HSYNC | | | AR29 |
| 155 | | CSI_D03 | | | AJ27 |
| 156 | | CSI_D05 | | | AM30 |
| 157 | | CSI_D02 | | | AP30 |
| 158 | | GND | | | |
| 159 | | GND | | | |
| 160 | | MIPI_DSI0_DATA1_N | | | AJ17 |
| 161 | | MIPI_DSI0_DATA0_N | | | AJ21 |
| 162 | | MIPI_DSI0_DATA1_P | | | AK18 |
| 163 | | MIPI_DSI0_DATA0_P | | | AK22 |
| 164 | | MIPI_DSI0_DATA2_N | | | AJ23 |
| 165 | | MIPI_DSI0_DATA3_N | | | AJ15 |
| 166 | | MIPI_DSI0_DATA2_P | | | AK24 |
| 167 | | MIPI_DSI0_DATA3_P | | | AK16 |
| 168 | | MIPI_DSI0_CLK_N | | | AJ19 |
| 169 | | GND | | | |

| Pin # | Assembly | Pin Name | Notes | GPIO | Ball |
|---|---|---|---|---|---|
| 170 | | MIPI_DSI0_CLK_P | | | AK20 |
| 171 | | UART2_TX | | GPIO1_IO23 | AC35 |
| 172 | | GND | | | |
| 173 | | CSI_VSYNC | | | AL27 |
| 174 | | SPI3_CS1 | | | K30 |
| 175 | | UART1_RX | | GPIO0_IO22 | L31 |
| 176 | | MCLK_IN1 | | | M28 |
| 177 | | ESAI0_TX5_RX0 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | GPIO0_IO09 | J29 |
| 178 | | GND | | | |
| 179 | | GND | | | |
| 180 | | MIPI_DSI1_CLK_N | | | AM16 |
| 181 | | MIPI_DSI1_DATA3_P | | | AP18 |
| 182 | | MIPI_DSI1_CLK_P | | | AP16 |
| 183 | | MIPI_DSI1_DATA3_N | | | AM18 |
| 184 | | MIPI_DSI1_DATA0_N | | | AN15 |
| 185 | | GND | | | |
| 186 | | MIPI_DSI1_DATA0_P | | | AR15 |
| 187 | TP | TS_X- | | | TSC2046.8 |
| 187 | No TP | SPI3_SDO | Available in SOM without TP | GPIO0_IO14 | F34 |
| 188 | | MIPI_DSI1_DATA1_N | | | AN17 |
| 189 | TP | TS_X+ | | | TSC2046.6 |
| 189 | No TP | SPI3_SCK | Available in SOM without TP | GPIO0_IO13 | H32 |
| 190 | | MIPI_DSI1_DATA1_P | | | AR17 |
| 191 | TP | TS_Y+ | | | TSC2046.7 |
| 191 | No TP | SPI3_CS0 | Available in SOM without TP | GPIO0_IO16 | J31 |
| 192 | | MIPI_DSI1_DATA2_N | | | AM14 |
| 193 | TP | TS_Y- | | | TSC2046.9 |
| 193 | No TP | SPI3_SDI | Available in SOM without TP | GPIO0_IO15 | G33 |
| 194 | | MIPI_DSI1_DATA2_P | | | AP14 |
| 195 | AC | AGND | Audio interface ground reference | | Audio AGND |
| 196 | AC | HPOUTFB | Headphone output ground loop noise rejection feedback | | WM8904CGEFL.14 |
| 196 | No AC | SAI0_RXD | Available in SOM without AC | GPIO0_IO27 | M34 |
| 197 | AC | LINEIN1_LP | Left channel input | | WM8904CGEFL.26 |
| 197 | No AC | SAI0_TXD | Available in SOM without AC | GPIO0_IO25 | K34 |
| 198 | AC | HPLOUT | Left headphone output (line or headphone output) | | WM8904CGEFL.13 |
| 198 | No AC | FLEXCAN1_TX | Available in SOM without AC | GPIO1_IO18 | AA35 |
| 199 | AC | LINEIN1_RP | Right channel input | | WM8904CGEFL.24 |
| 199 | No AC | SAI1_RXFS | Available in SOM without AC | GPIO0_IO31 | N35 |

| Pin # | Assembly | Pin Name | Notes | GPIO | Ball |
|---|---|---|---|---|---|
| 200 | AC | HPROUT | Right headphone output (line or headphone output) | | WM8904CGEFL.15 |
| 200 | No AC | SAI1_RXC | Available in SOM without AC | GPIO0_IO30 | L35 |

## 7.5 VAR-SOM-MX8X Connector Pin Mux

***Table 3: VAR-SOM-MX8X PINMUX***

| Pin | Assembly | Ball | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 |
|---|---|---|---|---|---|---|---|
| 17 | | AD32 | MIPI_DSI0.GPIO0.IO00 | ADMA.I2C1.SCL | MIPI_DSI0.PWM0.OUT | | LSIO.GPIO1.IO27 |
| 18 | No AC | AA33 | ADMA.FLEXCAN1.RX | ADMA.SAI2.RXFS | ADMA.FTM.CH2 | ADMA.SAI1.TXD | LSIO.GPIO1.IO17 |
| 20 | No AC | L29 | ADMA.ACM.MCLK_OUT0 | ADMA.ESAI0.TX_HF_CLK | ADMA.LCD_CLK | ADMA.SPI2.SDO | LSIO.GPIO0.IO20 |
| 21 | | R33 | ADMA.SPI0.CS0 | ADMA.SAI0.RXD | M40.TPM0.CH1 | M40.GPIO0.IO03 | LSIO.GPIO1.IO08 |
| 22 | | R35 | ADMA.SPI0.CS1 | ADMA.SAI0.RXC | ADMA.SAI1.TXD | ADMA.LCD_PWM0 | LSIO.GPIO1.IO07 |
| 23 | | M32 | ADMA.SAI1.RXD | ADMA.SAI0.RXFS | ADMA.SPI1.CS1 | ADMA.LCD_D21 | LSIO.GPIO0.IO29 |
| 24 | | R31 | ADMA.SPI0.SDO | ADMA.SAI0.TXFS | M40.I2C0.SDA | M40.GPIO0.IO01 | LSIO.GPIO1.IO06 |
| 25 | | P30 | ADMA.SPI0.SCK | ADMA.SAI0.TXC | M40.I2C0.SCL | M40.GPIO0.IO00 | LSIO.GPIO1.IO04 |
| 26 | | P34 | ADMA.SPI0.SDI | ADMA.SAI0.TXD | M40.TPM0.CH0 | M40.GPIO0.IO02 | LSIO.GPIO1.IO05 |
| 29 | | AN25 | MIPI_CSI0.ACM.MCLK_OUT | | | | LSIO.GPIO3.IO04 |
| 30 | | B32 | CONN.ENET0.MDIO | ADMA.I2C3.SDA | CONN.ENET1.MDIO | | LSIO.GPIO5.IO10 |
| 39 | | P28 | ADMA.SPI2.CS0 | | | | LSIO.GPIO1.IO00 |
| 40 | | E35 | ADMA.SPDIF0.EXT_CLK | | ADMA.LCD_D12 | CONN.ENET1.REFCLK_125M_25M | LSIO.GPIO0.IO12 |
| 41 | | G35 | ADMA.ACM.MCLK_IN0 | ADMA.ESAI0.RX_HF_CLK | ADMA.LCD_VSYNC | ADMA.SPI2.SDI | LSIO.GPIO0.IO19 |
| 42 | | H14 | ADMA.I2C1.SCL | CONN.USB_OTG2.PWR | | | LSIO.GPIO4.IO04 |
| 43 | | R29 | ADMA.SPI2.SCK | | | | LSIO.GPIO1.IO03 |
| 44 | | AA31 | ADMA.FLEXCAN2.TX | ADMA.SAI3.RXFS | ADMA.UART3.TX | ADMA.SAI1.RXC | LSIO.GPIO1.IO20 |
| 45 | | P32 | ADMA.SPI2.SDO | | | | LSIO.GPIO1.IO01 |
| 46 | | AB34 | ADMA.FLEXCAN2.RX | ADMA.SAI3.RXD | ADMA.UART3.RX | ADMA.SAI1.RXFS | LSIO.GPIO1.IO19 |
| 48 | | AP28 | CI_PI.CSI_EN | CI_PI.CSI_I2C.SCL | ADMA.I2C3.SCL | ADMA.SPI1.SDI | LSIO.GPIO3.IO02 |

| Pin | Assembly | Ball | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 |
|---|---|---|---|---|---|---|---|
| 50 | | Y34 | ADMA.FLEXCAN0.RX | ADMA.SAI2.RXC | ADMA.UART0.RTS_B | ADMA.SAI1.TXC | LSIO.GPIO1.IO15 |
| 51 | | Y32 | ADMA.FLEXCAN0.TX | ADMA.SAI2.RXD | ADMA.UART0.CTS_B | ADMA.SAI1.TXFS | LSIO.GPIO1.IO16 |
| 52 | | AA29 | ADMA.UART0.TX | ADMA.MQS.L | ADMA.FLEXCAN0.TX | SCU.UART0.TX | LSIO.GPIO1.IO22 |
| 53 | | AB32 | ADMA.UART0.RX | ADMA.MQS.R | ADMA.FLEXCAN0.RX | SCU.UART0.RX | LSIO.GPIO1.IO21 |
| 54 | | B34 | ADMA.ESAI0.TX1 | | ADMA.LCD_D05 | CONN.ENET1.RGMII_RXD3 | LSIO.GPIO0.IO05 |
| 55 | | E31 | ADMA.ESAI0.SCKT | | ADMA.LCD_D03 | CONN.ENET1.RGMII_TXD3 | LSIO.GPIO0.IO03 |
| 56 | | G29 | ADMA.ESAI0.FST | | ADMA.LCD_D01 | CONN.ENET1.RGMII_TXD2 | LSIO.GPIO0.IO01 |
| 57 | | D32 | ADMA.ESAI0.TX0 | | ADMA.LCD_D04 | CONN.ENET1.RGMII_RXC | LSIO.GPIO0.IO04 |
| 60 | | G23 | CONN.USDHC1.CLK | | ADMA.UART3.RX | | LSIO.GPIO4.IO23 |
| 61 | | D26 | CONN.USDHC1.DATA2 | CONN.NAND.WE_B | ADMA.UART3.CTS_B | | LSIO.GPIO4.IO27 |
| 62 | | A27 | CONN.USDHC1.DATA0 | CONN.NAND.CE1_B | ADMA.MQS.L | | LSIO.GPIO4.IO25 |
| 63 | | B26 | CONN.USDHC1.DATA1 | CONN.NAND.RE_B | ADMA.UART3.TX | | LSIO.GPIO4.IO26 |
| 64 | | C25 | CONN.USDHC1.CMD | CONN.NAND.CE0_B | ADMA.MQS.R | | LSIO.GPIO4.IO24 |
| 65 | | E25 | CONN.USDHC1.DATA3 | CONN.NAND.ALE | ADMA.UART3.RTS_B | | LSIO.GPIO4.IO28 |
| 68 | | K32 | ADMA.UART1.CTS_B | LSIO.PWM3.OUT | ADMA.LCD_D17 | LSIO.GPT1.COMPARE | LSIO.GPIO0.IO24 |
| 69 | | N29 | ADMA.UART1.RTS_B | LSIO.PWM2.OUT | ADMA.LCD_D16 | LSIO.GPT1.CAPTURE | LSIO.GPT0.CLK |
| 70 | | AM26 | CI_PI.CSI_MCLK | MIPI_CSI0.I2C0.SDA | | ADMA.SPI1.SDO | LSIO.GPIO3.IO01 |
| 71 | | K28 | ADMA.ESAI0.TX2_RX3 | CONN.ENET1.RMII_RX_ER | ADMA.LCD_D06 | CONN.ENET1.RGMII_RXD2 | LSIO.GPIO0.IO06 |
| 72 | | F28 | CONN.ENET0.REFCLK_125M_25M | CONN.ENET0.PPS | CONN.ENET1.PPS | | LSIO.GPIO5.IO09 |
| 73 | | F32 | ADMA.ESAI0.TX4_RX1 | | ADMA.LCD_D08 | CONN.ENET1.RGMII_TXD0 | LSIO.GPIO0.IO08 |
| 74 | | D30 | CONN.ENET0.MDC | ADMA.I2C3.SCL | CONN.ENET1.MDC | | LSIO.GPIO5.IO11 |
| 75 | | L33 | ADMA.SAI0.TXFS | ADMA.SPI2.CS1 | ADMA.SPI1.SCK | | LSIO.GPIO0.IO28 |
| 77 | | J35 | ADMA.SAI0.TXC | ADMA.SAI1.TXD | ADMA.SPI1.SDI | ADMA.LCD_D19 | LSIO.GPIO0.IO26 |
| 79 | | AR27 | CI_PI.CSI_RESET | CI_PI.CSI_I2C.SDA | ADMA.I2C3.SDA | ADMA.SPI1.CS0 | LSIO.GPIO3.IO03 |
| 80 | | E23 | CONN.USDHC1.CD_B | CONN.NAND.DQS_P | ADMA.SPI2.CS0 | CONN.NAND.DQS | LSIO.GPIO4.IO22 |

| Pin | Assembly | Ball | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 |
|---|---|---|---|---|---|---|---|
| 81 | | C33 | ADMA.ESAI0.TX3_RX2 | | ADMA.LCD_D07 | CONN.ENET1.RGMII_RXD1 | LSIO.GPIO0.IO07 |
| 82 | | D24 | CONN.USDHC1.WP | CONN.NAND.DQS_N | ADMA.SPI2.SDI | | LSIO.GPIO4.IO21 |
| 83 | | AF28 | SCU.GPIO0.IO00 | SCU.UART0.RX | M40.UART0.RX | ADMA.UART3.RX | LSIO.GPIO2.IO03 |
| 84 | | AK26 | CI_PI.CSI_PCLK | MIPI_CSI0.I2C0.SCL | | ADMA.SPI1.SCK | LSIO.GPIO3.IO00 |
| 85 | | AH30 | SCU.GPIO0.IO01 | SCU.UART0.TX | M40.UART0.TX | ADMA.UART3.TX | SCU.WDOG0.WDOG_OUT |
| 86 | | AJ9 | LSIO.QSPI0B.SS1_B | LSIO.QSPI1A.SS1_B | LSIO.KPP0.ROW3 | | LSIO.GPIO3.IO24 |
| 87 | | G15 | ADMA.I2C1.SDA | CONN.USB_OTG1.OC | CONN.USB_OTG2.OC | | LSIO.GPIO4.IO05 |
| 88 | | F14 | ADMA.I2C1.SCL | CONN.USB_OTG1.PWR | CONN.USB_OTG2.PWR | | LSIO.GPIO4.IO03 |
| 90 | | AF34 | MIPI_DSI1.GPIO0.IO01 | ADMA.I2C2.SDA | | | LSIO.GPIO2.IO00 |
| 91 | | B18 | CONN.USB_SS3.RX_M_LN_0 | | | | |
| 92 | | AD30 | MIPI_DSI1.GPIO0.IO00 | ADMA.I2C2.SCL | MIPI_DSI1.PWM0.OUT | | LSIO.GPIO1.IO31 |
| 93 | | A19 | CONN.USB_SS3.RX_P_LN_0 | | | | |
| 94 | | F16 | CONN.USB_OTG2.ID | | | | |
| 96 | | F30 | ADMA.ESAI0.FSR | CONN.ENET1.RCLK50M_OUT | ADMA.LCD_D00 | CONN.ENET1.RGMII_TXC | CONN.ENET1.RCLK50M_IN |
| 97 | | B16 | CONN.USB_SS3.TX_P_LN_0 | | | | |
| 99 | | A15 | CONN.USB_SS3.TX_M_LN_0 | | | | |
| 100 | | D12 | HSIO.PCIE_IOB.EXT_REFCLK100M_N | | | | |
| 102 | | E11 | HSIO.PCIE_IOB.EXT_REFCLK100M_P | | | | |
| 104 | | H18 | CONN.USB_OTG1.VBUS | | | | |
| 106 | | H16 | CONN.USB_OTG2.VBUS | | | | |
| 108 | | E19 | CONN.USB_OTG1.DN | | | | |
| 110 | | D18 | CONN.USB_OTG1.DP | | | | |
| 113 | | H28 | ADMA.ESAI0.SCKR | | ADMA.LCD_D02 | CONN.ENET1.RGMII_TX_CTL | LSIO.GPIO0.IO02 |
| 114 | | D16 | CONN.USB_OTG2.DM | | | | |
| 115 | | AD34 | ADMA.UART2.RX | ADMA.FTM.CH0 | ADMA.FLEXCAN1.RX | | LSIO.GPIO1.IO24 |

| Pin | Assembly | Ball | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 |
|---|---|---|---|---|---|---|---|
| 116 | | E17 | CONN.USB_OTG2.DP | | | | |
| 117 | | AH10 | LSIO.QSPI0B.SS0_B | LSIO.QSPI1A.SS0_B | LSIO.KPP0.ROW2 | | LSIO.GPIO3.IO23 |
| 119 | | AP22 | MIPI_CSI0.DP0 | | | | |
| 120 | | D34 | ADMA.SPDIF0.TX | ADMA.MQS.L | ADMA.LCD_D11 | CONN.ENET1.RGMII_RX_CTL | LSIO.GPIO0.IO11 |
| 121 | | AM22 | MIPI_CSI0.DN0 | | | | |
| 122 | | G31 | ADMA.SPDIF0.RX | ADMA.MQS.R | ADMA.LCD_D10 | CONN.ENET1.RGMII_RXD0 | LSIO.GPIO0.IO10 |
| 123 | | AM20 | MIPI_CSI0.DN1 | | | | |
| 124 | | H34 | ADMA.UART1.TX | LSIO.PWM0.OUT | LSIO.GPT0.CAPTURE | | LSIO.GPIO0.IO21 |
| 125 | | AP20 | MIPI_CSI0.DP1 | | | | |
| 127 | | AR23 | MIPI_CSI0.DP2 | | | | |
| 128 | | A9 | HSIO.PCIE0.TX0_N | | | | |
| 129 | | AN23 | MIPI_CSI0.DN2 | | | | |
| 130 | | B10 | HSIO.PCIE0.TX0_P | | | | |
| 131 | | AN19 | MIPI_CSI0.DN3 | | | | |
| 133 | | AR19 | MIPI_CSI0.DP3 | | | | |
| 134 | | A13 | HSIO.PCIE0.RX0_P | | | | |
| 135 | | AR21 | MIPI_CSI0.CKP | | | | |
| 136 | | B12 | HSIO.PCIE0.RX0_N | | | | |
| 137 | | AN21 | MIPI_CSI0.CKN | | | | |
| 140 | No ADC | AJ11 | LSIO.QSPI0B.DATA2 | LSIO.QSPI1A.DATA2 | LSIO.KPP0.COL3 | | LSIO.GPIO3.IO20 |
| 140 | ADC | U35 | ADMA.ADC.IN0 | M40.I2C0.SCL | M40.GPIO0.IO00 | | LSIO.GPIO1.IO10 |
| 141 | No ADC | AL9 | LSIO.QSPI0B.DATA1 | LSIO.QSPI1A.DATA1 | LSIO.KPP0.COL2 | | LSIO.GPIO3.IO19 |
| 141 | ADC | V32 | ADMA.ADC.IN2 | M40.UART0.RX | M40.GPIO0.IO02 | ADMA.ACM.MCLK_IN0 | LSIO.GPIO1.IO12 |
| 142 | No ADC | AM10 | LSIO.QSPI0B.DATA0 | LSIO.QSPI1A.DATA0 | LSIO.KPP0.COL1 | | LSIO.GPIO3.IO18 |
| 142 | ADC | U33 | ADMA.ADC.IN1 | M40.I2C0.SDA | M40.GPIO0.IO01 | | LSIO.GPIO1.IO09 |

| Pin | Assembly | Ball | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 |
|---|---|---|---|---|---|---|---|
| 143 | No ADC | AM8 | LSIO.QSPI0B.DATA3 | LSIO.QSPI1A.DATA3 | LSIO.KPP0.ROW0 | | LSIO.GPIO3.IO21 |
| 143 | ADC | V30 | ADMA.ADC.IN3 | M40.UART0.TX | M40.GPIO0.IO03 | ADMA.ACM.MCLK_OUT0 | LSIO.GPIO1.IO11 |
| 145 | No ADC | AK10 | LSIO.QSPI0B.DQS | LSIO.QSPI1A.DQS | LSIO.KPP0.ROW1 | | LSIO.GPIO3.IO22 |
| 145 | ADC | V34 | ADMA.ADC.IN5 | M40.TPM0.CH1 | M40.GPIO0.IO05 | | LSIO.GPIO1.IO13 |
| 146 | | AK32 | SCU.DSC.BOOT_MODE1 | | | | |
| 147 | No ADC | AR11 | LSIO.QSPI0B.SCLK | LSIO.QSPI1A.SCLK | LSIO.KPP0.COL0 | | LSIO.GPIO3.IO17 |
| 147 | ADC | W29 | ADMA.ADC.IN4 | M40.TPM0.CH0 | M40.GPIO0.IO04 | | LSIO.GPIO1.IO14 |
| 148 | | AN29 | CI_PI.CSI_D06 | | ADMA.SAI2.RXD | | |
| 150 | | AK28 | CI_PI.CSI_D02 | | ADMA.SAI0.RXC | | |
| 151 | | AM28 | CI_PI.CSI_D09 | | ADMA.SAI3.RXD | | |
| 152 | | AL29 | CI_PI.CSI_D03 | | ADMA.SAI0.RXD | | |
| 153 | | AJ25 | CI_PI.CSI_D08 | | ADMA.SAI3.RXC | | |
| 154 | | AR29 | CI_PI.CSI_HSYNC | CI_PI.CSI_D00 | ADMA.SAI3.RXFS | | |
| 155 | | AJ27 | CI_PI.CSI_D05 | | ADMA.SAI2.RXC | | |
| 156 | | AM30 | CI_PI.CSI_D07 | | ADMA.SAI2.RXFS | | |
| 157 | | AP30 | CI_PI.CSI_D04 | | ADMA.SAI0.RXFS | | |
| 160 | | AJ17 | MIPI_DSI0.DN1 | | | | |
| 161 | | AJ21 | MIPI_DSI0.DN0 | | | | |
| 162 | | AK18 | MIPI_DSI0.DP1 | | | | |
| 163 | | AK22 | MIPI_DSI0.DP0 | | | | |
| 164 | | AJ23 | MIPI_DSI0.DN2 | | | | |
| 165 | | AJ15 | MIPI_DSI0.DN3 | | | | |
| 166 | | AK24 | MIPI_DSI0.DP2 | | | | |
| 167 | | AK16 | MIPI_DSI0.DP3 | | | | |
| 168 | | AJ19 | MIPI_DSI0.CKN | | | | |

| Pin | Assembly | Ball | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 |
|---|---|---|---|---|---|---|---|
| 170 | | AK20 | MIPI_DSI0.CKP | | | | |
| 171 | | AC35 | ADMA.UART2.TX | ADMA.FTM.CH1 | ADMA.FLEXCAN1.TX | | LSIO.GPIO1.IO23 |
| 173 | | AL27 | CI_PI.CSI_VSYNC | CI_PI.CSI_D01 | | | |
| 174 | | K30 | ADMA.SPI3.CS1 | ADMA.I2C3.SCL | ADMA.LCD_RESET | ADMA.SPI2.CS0 | ADMA.LCD_D16 |
| 175 | | L31 | ADMA.UART1.RX | LSIO.PWM1.OUT | LSIO.GPT0.COMPARE | LSIO.GPT1.CLK | LSIO.GPIO0.IO22 |
| 176 | | M28 | ADMA.ACM.MCLK_IN1 | ADMA.I2C3.SDA | ADMA.LCD_EN | ADMA.SPI2.SCK | ADMA.LCD_D17 |
| 177 | | J29 | ADMA.ESAI0.TX5_RX0 | | ADMA.LCD_D09 | CONN.ENET1.RGMII_TXD1 | LSIO.GPIO0.IO09 |
| 180 | | AM16 | MIPI_DSI1.CKN | | | | |
| 181 | | AP18 | MIPI_DSI1.DP3 | | | | |
| 182 | | AP16 | MIPI_DSI1.CKP | | | | |
| 183 | | AM18 | MIPI_DSI1.DN3 | | | | |
| 184 | | AN15 | MIPI_DSI1.DN0 | | | | |
| 186 | | AR15 | MIPI_DSI1.DP0 | | | | |
| 187 | No TP | F34 | ADMA.SPI3.SDO | | ADMA.LCD_D14 | | LSIO.GPIO0.IO14 |
| 188 | | AN17 | MIPI_DSI1.DN1 | | | | |
| 189 | No TP | H32 | ADMA.SPI3.SCK | | ADMA.LCD_D13 | | LSIO.GPIO0.IO13 |
| 190 | | AR17 | MIPI_DSI1.DP1 | | | | |
| 191 | No TP | J31 | ADMA.SPI3.CS0 | ADMA.ACM.MCLK_OUT1 | ADMA.LCD_HSYNC | | LSIO.GPIO0.IO16 |
| 192 | | AM14 | MIPI_DSI1.DN2 | | | | |
| 193 | No TP | G33 | ADMA.SPI3.SDI | | ADMA.LCD_D15 | | LSIO.GPIO0.IO15 |
| 194 | | AP14 | MIPI_DSI1.DP2 | | | | |
| 196 | No AC | M34 | ADMA.SAI0.RXD | ADMA.SAI1.RXFS | ADMA.SPI1.CS0 | ADMA.LCD_D20 | LSIO.GPIO0.IO27 |
| 197 | No AC | K34 | ADMA.SAI0.TXD | ADMA.SAI1.RXC | ADMA.SPI1.SDO | ADMA.LCD_D18 | LSIO.GPIO0.IO25 |
| 198 | No AC | AA35 | ADMA.FLEXCAN1.TX | ADMA.SAI3.RXC | ADMA.DMA0.REQ_IN0 | ADMA.SAI1.RXD | LSIO.GPIO1.IO18 |
| 199 | No AC | N35 | ADMA.SAI1.RXFS | ADMA.SAI1.TXFS | | ADMA.LCD_D23 | LSIO.GPIO0.IO31 |

| Pin | Assembly | Ball | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 |
|---|---|---|---|---|---|---|---|
| 200 | No AC | L35 | ADMA.SAI1.RXC | ADMA.SAI1.TXC | | ADMA.LCD_D22 | LSIO.GPIO0.IO30 |

# 8. SOM's interfaces

**Trace Impedance**

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

***Table 4: SOM Signal Group Traces Impedance***

| Signal Group | Impedance |
|---|---|
| All single ended signals | 50 Ω Single ended |
| PCIe TX/RX data pairs | 85 Ω Differential |
| USB Differential signals | 90 Ω Differential |
| Differential signals including: Ethernet, PCIe clocks, MIPI (CSI and DSI), LVDS lines | 100 Ω Differential |

## 8.1 Display Interfaces

### 8.1.1 MIPI-DSI/LVDS

- MIPI-DSI/LVDS combo subsystem

  The i.MX8QXP/ i.MX8DXP MIPI consists of the DSI/ LVDS combo subsystem for interfacing MIPI-DSI or LVDS displays.

  The MIPI DSI supports the following features:

  - Can use up to 4-lane DSI Interface
  - Bi-direction Communication and Escape mode
  - Programmable display resolutions, from 160x120(QQVGA) to 1920x1200(WUXGA) @ 60 fps, 24bpp
  - Multiple Peripheral Support capability, configurable virtual channels
  - Video Mode Pixel Formats supported are 16bpp (RGB565), 18bpp(RGB666) packed, 18bpp (RGB666) loosely packed, 24bpp (RGB888).
  - Support for End of Transmission packet (EoTp)
  - Support for Ultra Low Power state Mode (ULPS)

  The LVDS supports the following features:

  - 4-lane LVDS Interface
  - Support display resolutions up to 1920x1080 (FHD) @ 60fps, 24bpp
  - Supports 18 bpp pixel format (RGB666) and 24 bpp pixel format (RGB888)
  - Synchronization and control capabilities
  - Arranging the data as required by the external display receiver and by the LVDS subsystem

*Table 5: MIPI-DSI/LVDS Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 17 | | MIPI_DSI0_GPIO0_IO00 | | AD32 |
| 92 | | MIPI_DSI1_GPIO0_IO00 | | AD30 |
| 17 | | MIPI_DSI0_PWM0_OUT | | AD32 |
| 92 | | MIPI_DSI1_PWM0_OUT | | AD30 |
| 168 | | MIPI_DSI0_CLK_N | | AJ19 |
| 170 | | MIPI_DSI0_CLK_P | | AK20 |
| 161 | | MIPI_DSI0_DATA0_N | | AJ21 |
| 163 | | MIPI_DSI0_DATA0_P | | AK22 |
| 160 | | MIPI_DSI0_DATA1_N | | AJ17 |
| 162 | | MIPI_DSI0_DATA1_P | | AK18 |
| 164 | | MIPI_DSI0_DATA2_N | | AJ23 |
| 166 | | MIPI_DSI0_DATA2_P | | AK24 |
| 165 | | MIPI_DSI0_DATA3_N | | AJ15 |
| 167 | | MIPI_DSI0_DATA3_P | | AK16 |
| 180 | | MIPI_DSI1_CLK_N | | AM16 |
| 182 | | MIPI_DSI1_CLK_P | | AP16 |
| 184 | | MIPI_DSI1_DATA0_N | | AN15 |
| 186 | | MIPI_DSI1_DATA0_P | | AR15 |
| 188 | | MIPI_DSI1_DATA1_N | | AN17 |
| 190 | | MIPI_DSI1_DATA1_P | | AR17 |
| 192 | | MIPI_DSI1_DATA2_N | | AM14 |
| 194 | | MIPI_DSI1_DATA2_P | | AP14 |
| 183 | | MIPI_DSI1_DATA3_N | | AM18 |
| 181 | | MIPI_DSI1_DATA3_P | | AP18 |

### 8.1.2 Parallel LCD

- Parallel LCDIF
  The i.MX8QXP/ i.MX8DXP consists of the LCDIF block to drive a wide range of display devices varying in size and capability.

  The LCDIF block supports the following:

  - Displays with an asynchronous parallel MPU interface for command and data transfer to an integrated frame buffer.
  - Displays that support moving pictures and require the RGB interface mode (DOTCLK interface).
  - VSYNC mode for high-speed data transfers.
  - Digital video encoders that accept ITU-R BT.656 format 4:2:2 YCbCr digital component video and convert it to analog TV signals.
  - Bus master interface to source frame buffer data for display refresh. This interface can also be used to drive data for "Smart" displays.
  - PIO interface to manage data transfers between "Smart" displays and SoC.
  - 8/16/18/24 bit LCD data bus support available depending on I/O mux options.
  - Programmable timing and parameters for MPU, VSYNC, and DOTCLK LCD interfaces to support a wide variety of displays.
  - ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.

*Table 6: Parallel LCD Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 20 | No AC | ADMA_LCD_CLK | Available in SOM without AC | L29 |
| 96 | | ADMA_LCD_D00 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | F30 |
| 56 | | ADMA_LCD_D01 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | G29 |
| 113 | | ADMA_LCD_D02 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | H28 |
| 55 | | ADMA_LCD_D03 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | E31 |
| 57 | | ADMA_LCD_D04 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | D32 |
| 54 | | ADMA_LCD_D05 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | B34 |
| 71 | | ADMA_LCD_D06 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | K28 |
| 81 | | ADMA_LCD_D07 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | C33 |
| 73 | | ADMA_LCD_D08 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | F32 |
| 177 | | ADMA_LCD_D09 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | J29 |
| 122 | | ADMA_LCD_D10 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | G31 |
| 120 | | ADMA_LCD_D11 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | D34 |
| 40 | | ADMA_LCD_D12 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | E35 |
| 189 | No TP | ADMA_LCD_D13 | Available in SOM without TP | H32 |
| 187 | No TP | ADMA_LCD_D14 | Available in SOM without TP | F34 |
| 193 | No TP | ADMA_LCD_D15 | Available in SOM without TP | G33 |
| 174 | | ADMA_LCD_D16 | | K30 |
| 69 | | ADMA_LCD_D16 | | N29 |
| 176 | | ADMA_LCD_D17 | | M28 |
| 68 | | ADMA_LCD_D17 | | K32 |
| 197 | No AC | ADMA_LCD_D18 | Available in SOM without AC | K34 |
| 77 | | ADMA_LCD_D19 | | J35 |
| 196 | No AC | ADMA_LCD_D20 | Available in SOM without AC | M34 |
| 23 | | ADMA_LCD_D21 | | M32 |
| 200 | No AC | ADMA_LCD_D22 | Available in SOM without AC | L35 |
| 199 | No AC | ADMA_LCD_D23 | Available in SOM without AC | N35 |
| 176 | | ADMA_LCD_EN | | M28 |
| 191 | No TP | ADMA_LCD_HSYNC | Available in SOM without TP | J31 |
| 22 | | ADMA_LCD_PWM0 | | R35 |
| 174 | | ADMA_LCD_RESET | | K30 |
| 41 | | ADMA_LCD_VSYNC | | G35 |

## 8.2 Camera Interface

### 8.2.1 MIPI CSI-2

The SOM consist of a CSI-2 Host Controller which implements all protocol functions defined in the MIPI CSI-2 specification, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 controller supports the following features:

- Implements all three CSI-2 MIPI layers (Pixel to byte packing, low level protocol, Lane management)
- Supports unidirectional Master operation
- Transmitter and receiver versions
- Scalable data lane support, 1 to 4 Data Lanes
- Supports high speed mode(80Mbps - 1.5Gbps) per lane, providing 4K@30fps capability for the 4 lanes
- Supports 10Mbps data rate in low power mode
- Includes high speed deserializers
- Loopback testability support
- Support for all CSI-2 data types
- Virtual Channel support
- Support for DPHY Ultra Low Power State (ULPS)
- Error collection support (Rx Only)
- Flexible pixel-based user interface
    - Supports user generated packets
    - Supports single, double, or quad pixel interface
- Supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs
    - Delivered fully integrate and verified with target MIPI D-PHY
- RX Video Interface
- APB Control and Status Register (CSR) interface with IRQ support
- Easy configuration and control via core ports
- Optimized for use in FPGAs and ASICs
- Provided with full-featured MIPI Test bench
    - Provides scripting, stimulus and data logging capabilities
    - Can be used for basic verification of user's design
- Source code option
- Provided with expert technical support
- Customization and integration services available

*Table 7: MIPI-CSI2 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 84 | | MIPI_CSI0_I2C0_SCL | | AK26 |
| 70 | | MIPI_CSI0_I2C0_SDA | | AM26 |
| 29 | | MIPI_CSI0_ACM_MCLK_OUT | | AN25 |
| 137 | | MIPI_CSI0_CKN | | AN21 |
| 135 | | MIPI_CSI0_CKP | | AR21 |
| 121 | | MIPI_CSI0_DN0 | | AM22 |
| 119 | | MIPI_CSI0_DP0 | | AP22 |
| 123 | | MIPI_CSI0_DN1 | | AM20 |
| 125 | | MIPI_CSI0_DP1 | | AP20 |
| 129 | | MIPI_CSI0_DN2 | | AN23 |
| 127 | | MIPI_CSI0_DP2 | | AR23 |
| 131 | | MIPI_CSI0_DN3 | | AN19 |
| 133 | | MIPI_CSI0_DP3 | | AR19 |

### 8.2.2 Parallel CSI

The Parallel Capture Subsystem consists of the Parallel Capture Interface (BT 656) and associated peripherals. It interfaces to the Parallel CSI sensor.
The PWM module provides support for camera sensor interface clocking requirements and to control illumination or optical zoom.
The I2C module is used to control and interact with image capture sensors.
The GPIO module is used to control internal logic and provide user defined control logic for sensor capture interfaces.

*Table 8: Parallel CSI Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 154 | | CI_PI_CSI_D00 | | AR29 |
| 173 | | CI_PI_CSI_D01 | | AL27 |
| 150 | | CI_PI_CSI_D02 | | AK28 |
| 152 | | CI_PI_CSI_D03 | | AL29 |
| 157 | | CI_PI_CSI_D04 | | AP30 |
| 155 | | CI_PI_CSI_D05 | | AJ27 |
| 148 | | CI_PI_CSI_D06 | | AN29 |
| 156 | | CI_PI_CSI_D07 | | AM30 |
| 153 | | CI_PI_CSI_D08 | | AJ25 |
| 151 | | CI_PI_CSI_D09 | | AM28 |
| 154 | | CI_PI_CSI_HSYNC | | AR29 |
| 173 | | CI_PI_CSI_VSYNC | | AL27 |
| 84 | | CI_PI_CSI_PCLK | | AK26 |
| 70 | | CI_PI_CSI_MCLK | | AM26 |
| 48 | | CI_PI_CSI_EN | | AP28 |
| 79 | | CI_PI_CSI_RESET | | AR27 |
| 48 | | CI_PI_CSI_I2C_SCL | | AP28 |
| 79 | | CI_PI_CSI_I2C_SDA | | AR27 |

## 8.3 Ethernet Interface

The iMX8QXP/iMX8DXP core implements a triple-speed 10/100/1000-Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full duplex 10/100-Mbit/s and full-duplex gigabit Ethernet LANs.
The core consists of the IEEE1588 time-stamping module. The IEEE 1588 standard provides accurate clock synchronization for distributed control nodes for industrial automation applications. The MAC interface supports also AVB (Audio Video Bridging, IEEE 802.1Qav)

The VAR-SOM-MX8X features on SOM a Gigabit PHY (Atheros AR8033 or ADIN1300) connected to ENET0 RGMII interface signals. External connector and magnetics should be implemented on carrier board complete the interface to the media.

ENET1 RGMII/RMII interface signals are exported through SO-DIMM connector.
Signals, in conjunction to MDIO signals exported from SO-DIMM connector, can be used to interface an external Ethernet PHY.

ENET1 pins are referenced to SOM pin 38 VDD_ENET1_1P8_2P5_3P3_IN.
Reference voltage should be supplied to SOM pin 38.
For RMII - 3.3 V
For RGMII - 1.8V or 2.5V

The Following External Gigabit magnetics are required to complete the ENET0 RGMII interface to the media.

***Table 9: Gigabit Ethernet Magnetics***

| Vendor | P/N | Package | Cores | Configuration |
|---|---|---|---|---|
| Pulse | H5007NL | Transformer | 8 | Auto-MDX |
| TDK | TLA-7T101LF | Transformer | 8 | Auto-MDX |
| Pulse | J0G-0009NL | Integrated RJ45 | 8 | Auto-MDX |

*Table 10: Ethernet0 PHY Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 5 | EC | ETH0_MDI_A_M | | AR8033.12/ ADIN1300.13 |
| 3 | EC | ETH0_MDI_A_P | | AR8033.11/ ADIN1300.12 |
| 11 | EC | ETH0_MDI_B_M | | AR8033.15/ ADIN1300.15 |
| 9 | EC | ETH0_MDI_B_P | | AR8033.14/ ADIN1300.14 |
| 6 | EC | ETH0_MDI_C_M | | AR8033.18/ ADIN1300.17 |
| 4 | EC | ETH0_MDI_C_P | | AR8033.17/ ADIN1300.16 |
| 12 | EC | ETH0_MDI_D_M | | AR8033.21/ ADIN1300.19 |
| 10 | EC | ETH0_MDI_D_P | | AR8033.20/ ADIN1300.18 |
| 15 | EC | ETH0_LED_ACT | Ethernet PHY Activity LED, active low | AR8033.23/ ADIN1300.21 |
| 16 | EC | ETH0_LED_LINK_10_100_1000 | Ethernet PHY Link LED, active low | AR8033.24_26/ ADIN1300.26 via inv. FET |

*Table 11: AR8033 Ethernet PHY LED Behavior*

| Symbol | 10M link | 10M active | 100M link | 100M active | 1000M link | 1000M active |
|---|---|---|---|---|---|---|
| LED_10_100_1000 | OFF | OFF | ON | ON | ON | ON |
| LED_ACT | ON | BLINK | ON | BLINK | ON | BLINK |
| ON = active; OFF = inactive | | | | | | |

*Table 12: ADIN1300 Ethernet PHY LED Behavior*

| Symbol | 10M link | 10M active | 100M link | 100M active | 1000M link | 1000M active |
|---|---|---|---|---|---|---|
| LED_10_100_1000 | ON | ON | ON | ON | ON | ON |
| LED_ACT | ON | BLINK | ON | BLINK | ON | BLINK |
| ON = active; OFF = inactive | | | | | | |

*Table 13: ENET1 Supply voltage input Signal*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 38 | | VDD_ENET1_1P8_2P5_3P3_IN | VAR-SOM-MX8X 1.8V/2.5V/3.3V supply voltage input.<br><br>The following SOM pins are referenced to this voltage:<br>40,54,55,56,57,71,73,81,96,113,120,122,177<br><br>When using the above pins for alternate functions of ENET1:<br>• For RMII - connect to 3.3V<br>• For RGMII - connect to 1.8V/2.5V | N25 |

*Table 14: ENET1 RGMII Port 1 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 40 | | CONN_ENET1_REFCLK_125M_25M | Referenced to pin 38 supply (1.8V/2.5/3.3V) | E35 |
| 120 | | CONN_ENET1_RGMII_RX_CTL | Referenced to pin 38 supply (1.8V/2.5/3.3V) | D34 |
| 57 | | CONN_ENET1_RGMII_RXC | Referenced to pin 38 supply (1.8V/2.5/3.3V) | D32 |
| 122 | | CONN_ENET1_RGMII_RXD0 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | G31 |
| 81 | | CONN_ENET1_RGMII_RXD1 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | C33 |
| 71 | | CONN_ENET1_RGMII_RXD2 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | K28 |
| 54 | | CONN_ENET1_RGMII_RXD3 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | B34 |
| 113 | | CONN_ENET1_RGMII_TX_CTL | Referenced to pin 38 supply (1.8V/2.5/3.3V) | H28 |
| 96 | | CONN_ENET1_RGMII_TXC | Referenced to pin 38 supply (1.8V/2.5/3.3V) | F30 |
| 73 | | CONN_ENET1_RGMII_TXD0 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | F32 |
| 177 | | CONN_ENET1_RGMII_TXD1 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | J29 |
| 56 | | CONN_ENET1_RGMII_TXD2 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | G29 |
| 55 | | CONN_ENET1_RGMII_TXD3 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | E31 |

*Table 15: ENET1 RMII Port 1 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 96 | | CONN_ENET1_RCLK50M_IN | ENET1 RMII RCLK50M Input Clock (see note [1]). Referenced to pin 38 supply (1.8V/2.5/3.3V) | F30 |
| 96 | | CONN_ENET1_RCLK50M_OUT | ENET1 RMII RCLK50M Output Clock (see note [1]). Referenced to pin 38 supply (1.8V/2.5/3.3V) | F30 |
| 120 | | CONN_ENET1_RGMII_RX_CTL | ENET1 RMII_CRS_DV Referenced to pin 38 supply (1.8V/2.5/3.3V) | D34 |
| 122 | | CONN_ENET1_RGMII_RXD0 | ENET1 RMII_RXD0 Referenced to pin 38 supply (1.8V/2.5/3.3V) | G31 |
| 81 | | CONN_ENET1_RGMII_RXD1 | ENET1 RMII_RXD1 Referenced to pin 38 supply (1.8V/2.5/3.3V) | C33 |
| 71 | | CONN_ENET1_RMII_RX_ER | ENET1 RMII_RXER (see note [1]). Referenced to pin 38 supply (1.8V/2.5/3.3V) | K28 |
| 113 | | CONN_ENET1_RGMII_TX_CTL | ENET1 RMII_TXEN Referenced to pin 38 supply (1.8V/2.5/3.3V) | H28 |
| 73 | | CONN_ENET1_RGMII_TXD0 | ENET1 RMII_TXD0 Referenced to pin 38 supply (1.8V/2.5/3.3V) | F32 |
| 177 | | CONN_ENET1_RGMII_TXD1 | ENET1 RMII_TXD1 Referenced to pin 38 supply (1.8V/2.5/3.3V) | J29 |

Note:

[1] Except for RCLK50M and RMII_RXER, all other RMII functions are using the same pin muxing mode of RGMII

*Table 16: MDIO & 1588 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 74 | | CONN_ENET0_MDC | Pin alternate function cannot be changed when using SOM with EC assembled | D30 |
| 30 | | CONN_ENET0_MDIO | Pin alternate function cannot be changed when using SOM with EC assembled | B32 |
| 74 | | CONN_ENET1_MDC | Pin alternate function cannot be changed when using SOM with EC assembled | D30 |
| 30 | | CONN_ENET1_MDIO | Pin alternate function cannot be changed when using SOM with EC assembled | B32 |
| 72 | | CONN_ENET1_PPS | | F28 |

## 8.4 Wi-Fi & BT & MMC/SD/SDIO

The VAR-SOM-MX8X contains a certified high-performance Wi-Fi and Bluetooth (BT) module:

- IEEE 802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR
- BLE 5.2 capabilities
- Modules have an antenna connection through a U.FL JACK connector
- Antenna cable connected to module must have 50-Ω impedance

Figure 3 illustrates the VAR-SOM-MX8X internal Wi-Fi and BT connectivity.

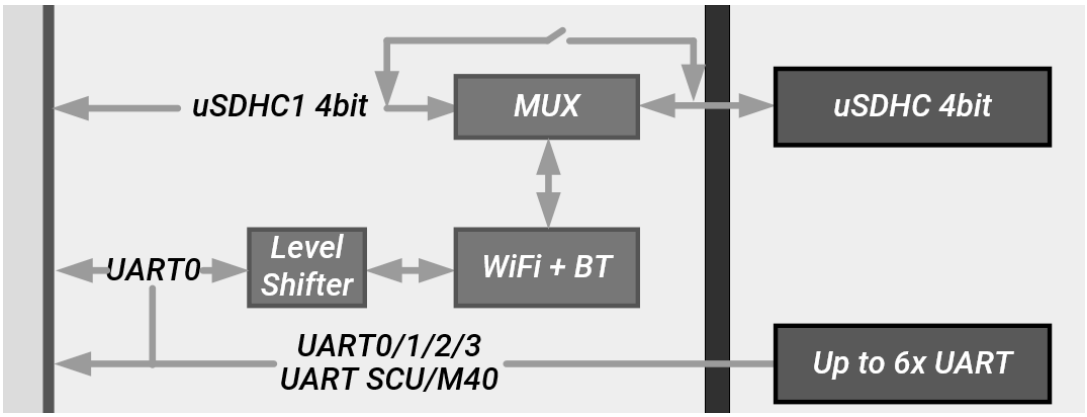



*Figure 3: VAR-SOM-MX8X Wi-Fi & BT Internal Connection*

To allow the most flexible solution the following elements are added to the VAR-SOM-MX8X:

- Tristate buffer on the BT link based on UART interface.
  Will allow isolation from the LWB5 module and the use by external circuity via the SO-DIMM connector.
- Multiplexer is used on the Usdhc1 (SOC uSDHC1 interface) 4-bit bus controlled using an internal GPIO.

Notes:

[1] BT UART tristate buffer controlled using MIPI_DSI1_I2C0_SCL pin alternate function GPIO1_29. A logic "Low" enables the buffer.

[2] Multiplexer controlled using QSPI0A_DATA0 alternate function GPIO3_9.
A "High" connects the USDHC1 interface to the Wi-Fi SDIO lines.
A "Low" connect the USDHC1 interface to the connector CONN_USDHC1 lines.

### 8.4.1 Interface implementation options

#### 8.4.1.1 Module configuration with "WBD" option

System use case:

**Wi-Fi and Bluetooth**.

- All external pins of the interfaces should float.

**Wi-Fi and No BT**.

- In this case, disable the BT buffer and BT function.
- BT UART interface pins can be used externally with any of the alternative functions.

**BT and No Wi-Fi**.

- In this case, SET the SDIO multiplexer to the connector state and disable the Wi-Fi interface.
- uSDHC1 lines can be connected externally.

#### 8.4.1.2 Module configuration without "WBD" option

System use case:

**No Wi-Fi and No BT**.

- SDIO signals bypassed and BT buffer not assembled.
- All the interfaces are accessible externally with alternative functions.

A second interface, uSDHC0 is used by the on SOM internal eMMC for boot and storage.

#### 8.4.1.3 SD Card recovery & development

To allow SD Card recovery and to ease the development process, booting from the SD card must be done with the kernel that does not have W-Fi module enabled i.e. Wi-Fi interface is not accessible when booting from SD card.

### 8.4.2 Bluetooth Interface signals

***Table 17: BT UART interface signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 50 | | ADMA_UART0_RTS_B | UART0 Request to Send Output.<br>Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | Y34 |
| 51 | | ADMA_UART0_CTS_B | UART0 Clear to Send Input.<br>Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | Y32 |
| 53 | | ADMA_UART0_RX | UART0 Receive Data Input.<br>Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | AB32 |
| 52 | | ADMA_UART0_TX | UART0 Transmit Data Output.<br>Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | AA29 |

### 8.4.3 uSDHC1 Interface signals

The exposed controller uSDHC1 can only support up to a 4-bit interface designed to support:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.0.
- 1.8 V and 3.3 V operation
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode
- Up to SDR104 rate

The uSDHC controller uSDHC0 can support up to an 8-bit interface is used internally for the eMMC interface on the SOM.

*Table 18: uSDHC1 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 82 | | CONN_USDHC1_WP | | D24 |
| 80 | | CONN_USDHC1_CD_B | | E23 |
| 60 | | CONN_USDHC1_CLK | Not connected when Wi-Fi is enabled | G23 |
| 64 | | CONN_USDHC1_CMD | Not connected when Wi-Fi is enabled | C25 |
| 62 | | CONN_USDHC1_DATA0 | Not connected when Wi-Fi is enabled | A27 |
| 63 | | CONN_USDHC1_DATA1 | Not connected when Wi-Fi is enabled | B26 |
| 61 | | CONN_USDHC1_DATA2 | Not connected when Wi-Fi is enabled | D26 |
| 65 | | CONN_USDHC1_DATA3 | Not connected when Wi-Fi is enabled | E25 |

## 8.5 USB 2.0

The SOM consists of a two USB controller blocks which provides 2 high-performance USB functionality USB ports that conform to the USB 2.0 specification.
Port 1 supports Host/Peripheral modes.
Port 2 supports OTG functionality as well as Host/Peripheral modes.

*Table 19: USB 2.0 Port 1 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 108 | | CONN_USB_OTG1_DN | | E19 |
| 110 | | CONN_USB_OTG1_DP | | D18 |
| 104 | | CONN_USB_OTG1_VBUS | USB Host VBUS (5V) input | H18 |

*Table 20: USB 2.0 Port 2 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 114 | | CONN_USB_OTG2_DN | | D16 |
| 116 | | CONN_USB_OTG2_DP | | E17 |
| 106 | | CONN_USB_OTG2_VBUS | USB OTG VBUS (5V) input | H16 |

### 8.5.1 USB OTG interface signals

The VAR-SOM-MX8X exposes pins, which can be optionally used to implement a complete OTG functions.

*Table 21: USB Port 1 & 2 OTG Interface signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 87 | | CONN_USB_OTG1_OC | | G15 |
| 88 | | CONN_USB_OTG1_PWR | | F14 |

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 94 | | CONN_USB_OTG2_ID | | F16 |
| 87 | | CONN_USB_OTG2_OC | | G15 |
| 88 | | CONN_USB_OTG2_PWR | | F14 |

## 8.6 USB 3.0

The SOM includes a Super-speed USB 3.0 core consisting of:

- Super Speed (5 Gbps), High Speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps)
- Fully compatible with the USB 3.0 specification (backward compatible with USB 2.0)
- Fully compatible with the USB On-The-Go supplement to the USB 2.0 specification
- Hardware support for OTG signaling
- Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) implemented in hardware, which can also be controlled by software

***Table 22: USB3 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 91 | | CONN_USB_SS3_RX_M_LN_0 | | B18 |
| 93 | | CONN_USB_SS3_RX_P_LN_0 | | A19 |
| 99 | | CONN_USB_SS3_TX_M_LN_0 | | A15 |
| 97 | | CONN_USB_SS3_TX_P_LN_0 | | B16 |

## 8.7 Audio

The SOM features three audio interfaces

- WM8904CGEFL Audio codec interfaces:
  - Analog outputs & inputs: stereo line-in & Stereo HP out.
  - Digital microphone input
- Enhanced Serial Audio Interface
- Serial Audio Interface
- S/PDIF in/out
- MQS (Medium Quality Sound)

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only. The codec interfaces the SoC via SAI1 lines, when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

The following figure illustrates the connectivity for no large AC coupling capacitors implemented on SOM.

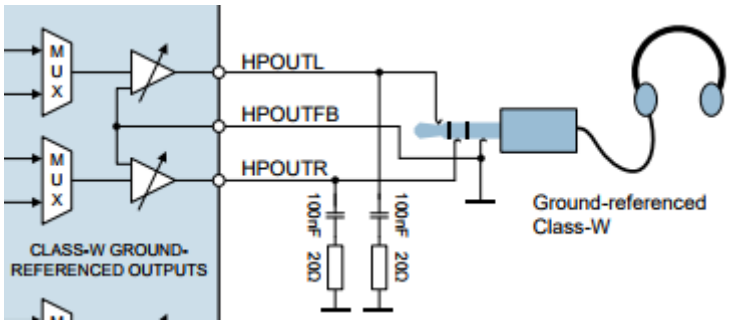



***Figure 4: WM8904 Headphone connectivity***

### 8.7.1 WM8904CGEFL Audio Codec

***Table 23: Analog audio Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 195 | AC | AGND | Audio interface ground reference | Audio AGND |
| 18 | AC | DMIC_CLK | Digital microphone clock output | WM8904CGEFL.1 |
| 20 | AC | DMIC_DATA | Digital microphone data input | WM8904CGEFL.27 |
| 198 | AC | HPLOUT | Left headphone output (line or headphone output) | WM8904CGEFL.13 |

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 196 | AC | HPOUTFB | Headphone output ground loop noise rejection feedback | WM8904CGEFL.14 |
| 200 | AC | HPROUT | Right headphone output (line or headphone output) | WM8904CGEFL.15 |
| 197 | AC | LINEIN1_LP | Left channel input | WM8904CGEFL.26 |
| 199 | AC | LINEIN1_RP | Right channel input | WM8904CGEFL.24 |

### 8.7.2 Enhanced Serial Audio Interface

The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available.

***Table 24: Enhanced Serial Audio Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 96 | | ADMA_ESAI0_FSR | Referenced to pin 38 supply (1.8V/2.5/3.3V) | F30 |
| 56 | | ADMA_ESAI0_FST | Referenced to pin 38 supply (1.8V/2.5/3.3V) | G29 |
| 113 | | ADMA_ESAI0_SCKR | Referenced to pin 38 supply (1.8V/2.5/3.3V) | H28 |
| 55 | | ADMA_ESAI0_SCKT | Referenced to pin 38 supply (1.8V/2.5/3.3V) | E31 |
| 57 | | ADMA_ESAI0_TX0 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | D32 |
| 54 | | ADMA_ESAI0_TX1 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | B34 |
| 71 | | ADMA_ESAI0_TX2_RX3 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | K28 |
| 81 | | ADMA_ESAI0_TX3_RX2 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | C33 |
| 73 | | ADMA_ESAI0_TX4_RX1 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | F32 |
| 177 | | ADMA_ESAI0_TX5_RX0 | Referenced to pin 38 supply (1.8V/2.5/3.3V) | J29 |
| 41 | | ADMA_ESAI0_RX_HF_CLK | | G35 |
| 20 | No AC | ADMA_ESAI0_TX_HF_CLK | Available in SOM without AC | L29 |

### 8.7.3 Serial Audio Interface

SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

***Table 25: Serial Audio Interface 0 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 22 | | ADMA_SAI0_RXC | | R35 |
| 150 | | ADMA_SAI0_RXC | | AK28 |
| 196 | No AC | ADMA_SAI0_RXD | Available in SOM without AC | M34 |
| 21 | | ADMA_SAI0_RXD | | R33 |
| 152 | | ADMA_SAI0_RXD | | AL29 |
| 23 | | ADMA_SAI0_RXFS | | M32 |
| 157 | | ADMA_SAI0_RXFS | | AP30 |
| 77 | | ADMA_SAI0_TXC | | J35 |
| 25 | | ADMA_SAI0_TXC | | P30 |
| 197 | No AC | ADMA_SAI0_TXD | Available in SOM without AC | K34 |
| 26 | | ADMA_SAI0_TXD | | P34 |
| 75 | | ADMA_SAI0_TXFS | | L33 |
| 24 | | ADMA_SAI0_TXFS | | R31 |

***Table 26: Serial Audio Interface 1 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 197 | No AC | ADMA_SAI1_RXC | Available in SOM without AC | K34 |
| 200 | No AC | ADMA_SAI1_RXC | Available in SOM without AC | L35 |
| 44 | | ADMA_SAI1_RXC | | AA31 |
| 23 | | ADMA_SAI1_RXD | | M32 |
| 198 | No AC | ADMA_SAI1_RXD | Available in SOM without AC | AA35 |
| 196 | No AC | ADMA_SAI1_RXFS | Available in SOM without AC | M34 |
| 199 | No AC | ADMA_SAI1_RXFS | Available in SOM without AC | N35 |
| 46 | | ADMA_SAI1_RXFS | | AB34 |
| 50 | | ADMA_SAI1_TXC | Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control. | Y34 |
| 200 | No AC | ADMA_SAI1_TXC | Available in SOM without AC | N35 |
| 77 | | ADMA_SAI1_TXD | | J35 |
| 22 | | ADMA_SAI1_TXD | | R35 |
| 18 | No AC | ADMA_SAI1_TXD | Available in SOM without AC | AA33 |
| 51 | | ADMA_SAI1_TXFS | Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control. | Y32 |
| 199 | No AC | ADMA_SAI1_TXFS | Available in SOM without AC | L35 |

*Table 27: Serial Audio Interface 2 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 50 | | ADMA_SAI2_RXC | Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control. | Y34 |
| 155 | | ADMA_SAI2_RXC | | AJ27 |
| 51 | | ADMA_SAI2_RXD | Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control. | Y32 |
| 148 | | ADMA_SAI2_RXD | | AN29 |
| 18 | No AC | ADMA_SAI2_RXFS | Available in SOM without AC | AA33 |
| 156 | | ADMA_SAI2_RXFS | | AM30 |

*Table 28: Serial Audio Interface 3 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 198 | No AC | ADMA_SAI3_RXC | Available in SOM without AC | AA35 |
| 153 | | ADMA_SAI3_RXC | | AJ25 |
| 46 | | ADMA_SAI3_RXD | | AB34 |
| 151 | | ADMA_SAI3_RXD | | AM28 |
| 44 | | ADMA_SAI3_RXFS | | AA31 |
| 154 | | ADMA_SAI3_RXFS | | AR29 |

The following table details the SAI interface signals definition.

*Table 29: SAI interface signals definition*

| Name | Function | DIR |
|---|---|---|
| **SAI_TXC** | **Transmit Bit Clock.** The bit clock is an input when externally generated and an output when internally generated. | I/O |
| **SAI_TXFS** | **Transmit Frame Sync.** The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated. | I/O |
| **SAI_TXD** | **Transmit Data.** The transmit data is generated synchronously by the bit clock and is tristate whenever not transmitting a word | O |
| **SAI_RXC** | **Receive Bit Clock.** The bit clock is an input when externally generated and an output when internally generated. | I/O |
| **SAI_RXFS** | **Receive Frame Sync.** The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated. | I/O |
| **SAI_RXD** | **Receive Data.** The receive data is sampled synchronously by the bit clock. | I |

### 8.7.4 Sony Phillips Digital Interface In/Out

Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. The SPDIF transceiver allows the handling of both SPDIF channel status (CS) and User (U) data and includes a frequency measurement block that allows the precise measurement of an incoming sampling frequency.

***Table 30: S/PDIF Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 40 | | ADMA_SPDIF0_EXT_CLK | Referenced to pin 38 supply (1.8V/2.5/3.3V) | E35 |
| 122 | | ADMA_SPDIF0_RX | Referenced to pin 38 supply (1.8V/2.5/3.3V) | G31 |
| 120 | | ADMA_SPDIF0_TX | Referenced to pin 38 supply (1.8V/2.5/3.3V) | D34 |

### 8.7.5 Medium quality sound (MQS)

Medium quality sound (MQS) is used to generate medium quality audio via a standard GPIO in the Pin mux, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip. MQS accepts the following inputs:

- 2-channel, LSB-valid 16-bit, MSB shift-out first serial data (sdata)
- Frame sync asserting with the first bit of the frame (fs)
- Bit clock used to shift data out on the positive clock edge (bclk)

***Table 31: MQS Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 120 | | ADMA_MQS_L | Referenced to pin 38 supply (1.8V/2.5/3.3V) | D34 |
| 52 | | ADMA_MQS_L | Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control. | AA29 |
| 62 | | ADMA_MQS_L | Not connected when Wi-Fi is enabled | A27 |
| 122 | | ADMA_MQS_R | Referenced to pin 38 supply (1.8V/2.5/3.3V) | G31 |
| 53 | | ADMA_MQS_R | Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control. | AB32 |
| 64 | | ADMA_MQS_R | Not connected when Wi-Fi is enabled | C25 |

## 8.8 Audio Clock Mux (ACM)

The SOM exports the Audio Clock Mux signals for connecting to Audio peripherals.

***Table 32: ACM Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 41 | | ADMA_ACM_MCLK_IN0 | | G35 |
| 141 | ADC | ADMA_ACM_MCLK_IN0 | Available in SOM with ADC (referenced to 1.8V) | V32 |
| 176 | | ADMA_ACM_MCLK_IN1 | | M28 |
| 20 | No AC | ADMA_ACM_MCLK_OUT0 | Available in SOM without AC | L29 |
| 143 | ADC | ADMA_ACM_MCLK_OUT0 | Alternate function can be used in SOM without AC<br>Available in SOM with ADC (referenced to 1.8V) | V30 |
| 191 | No TP | ADMA_ACM_MCLK_OUT1 | Available in SOM without TP | J31 |

## 8.9 Resistive Touch

The VAR-SOM-MX8X features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

The Resistive Touch is available only in SOMs with the “TP” assembly option

***Table 33: Resistive Touch Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 187 | TP | TS_X- | | TSC2046.8 |
| 189 | TP | TS_X+ | | TSC2046.6 |
| 191 | TP | TS_Y+ | | TSC2046.7 |
| 193 | TP | TS_Y- | | TSC2046.9 |

## 8.10 PCIe

The VAR-SOM-MX8X exposes a single PCI Express Gen 3.0 single lane interface.

The following list the key features of the PCIe PHY:

- 1.5 / 2.5 / 3.0 / 5.0 / 6.0 Gbps Serializer / Deserializer
- 100 MHz Reference Clock
- K28.5 Detection for Word Alignment
- 8B/10B Encoding / Decoding
- Supports Spread Spectrum Clocking in Transmitter and Receiver

The PCIe controller implements the following standards:

- PCI Express Base Specification, Revision 4.0, Version 0.7
- PIPE Specification for PCI Express, Version 4.3, Intel Corporation
- PCI Local Bus Specification, Revision 3.0
- PCI Bus Power Management Specification, Revision 1.2
- PCI Express Card Electromechanical Specification, Revision 1.1

Note: Access to the above specification requires membership in PCI-SIG.

***Table 34: PCIE Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 100 | | HSIO_PCIE_IOB_EXT_REFCLK100M_N | PCIe compliant 100MHz reference clock.<br>Can be exported from SOM or input to the SOM.<br><br>The internal PCIe reference clock is not spread spectrum capable.<br>For PCIe Gen 3.0 or EMC/EMI sensitive applications, it is recommended to connect to an external HCSL-compatible clock source. | D12 |
| 102 | | HSIO_PCIE_IOB_EXT_REFCLK100M_P | PCIe compliant 100MHz reference clock.<br>Can be exported from SOM or input to the SOM.<br><br>The internal PCIe reference clock is not spread spectrum capable.<br>For PCIe Gen 3.0 or EMC/EMI sensitive applications, it is recommended to connect to an external HCSL-compatible clock source. | E11 |
| 136 | | HSIO_PCIE0_RX0_N | | B12 |
| 134 | | HSIO_PCIE0_RX0_P | | A13 |
| 128 | | HSIO_PCIE0_TX0_N | | A9 |
| 130 | | HSIO_PCIE0_TX0_P | | B10 |

## 8.11 UART

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or multi drop mode (RS-485) support (automatic slave address detection)
- 7, 8, 9, or 10-bit data characters (7-bits only with parity), 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for RTS and CTS signals

***Table 35: UART0 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 51 | | ADMA_UART0_CTS_B | UART0 Clear to send input.<br>Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | Y32 |
| 50 | | ADMA_UART0_RTS_B | UART0 Request to send Output.<br>Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | Y34 |
| 53 | | ADMA_UART0_RX | UART0 Receive Data Input.<br>Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | AB32 |
| 52 | | ADMA_UART0_TX | UART0 Transmit Data Output.<br>Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | AA29 |

***Table 36: UART1 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 68 | | ADMA_UART1_CTS_B | UART1 Clear to send Input | K32 |
| 69 | | ADMA_UART1_RTS_B | UART1 Request to send Output | N29 |
| 175 | | ADMA_UART1_RX | UART1 Receive Data Input | L31 |
| 124 | | ADMA_UART1_TX | UART1 Transmit Data Output | H34 |

***Table 37: UART2 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 115 | | ADMA_UART2_RX | UART2 Receive Data Input | AD34 |
| 171 | | ADMA_UART2_TX | UART2 Transmit Data Output | AC35 |

*Table 38: UART3 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 61 | | ADMA_UART3_CTS_B | UART3 Clear to send Input.<br>Not connected when Wi-Fi is enabled | D26 |
| 65 | | ADMA_UART3_RTS_B | UART3 Request to send Output.<br>Not connected when Wi-Fi is enabled | E25 |
| 46 | | ADMA_UART3_RX | UART3 Receive Data Input. | AB34 |
| 83 | | ADMA_UART3_RX | UART3 Receive Data Input.<br>Pin is routed via on SOM buffer, set as Input by default.<br>Pin direction can be controlled by GPIO1_26:<br>Low - Output from SoC<br>High - Input to SoC | AF28 |
| 60 | | ADMA_UART3_RX | UART3 Receive Data Input.<br>Not connected when Wi-Fi is enabled | G23 |
| 44 | | ADMA_UART3_TX | UART3 Transmit Data Output. | AA31 |
| 85 | | ADMA_UART3_TX | UART3 Transmit Data Output.<br>Pin is routed via on SOM buffer set as Output by default.<br>Pin direction can be controlled by GPIO1_25:<br>Low - Output from SoC<br>High - Input to SoC | AH30 |
| 63 | | ADMA_UART3_TX | UART3 Transmit Data Output<br>Not connected when Wi-Fi is enabled | B26 |

## 8.12 Flexible Controller Area Network

The Flexible Controller Area Network (FLEXCAN) module is a communication controller supporting CAN-FD (CAN Flexible Data Rate) and CAN2.0B specification.
Signal Description:

- CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
- CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

***Table 39: FLEXCAN0 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 50 | | ADMA_FLEXCAN0_RX | Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control. | Y34 |
| 53 | | ADMA_FLEXCAN0_RX | Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control. | AB32 |
| 51 | | ADMA_FLEXCAN0_TX | Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control. | Y32 |
| 52 | | ADMA_FLEXCAN0_TX | Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control. | AA29 |

***Table 40: FLEXCAN1 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 18 | No AC | ADMA_FLEXCAN1_RX | Available in SOM without AC | AA33 |
| 115 | | ADMA_FLEXCAN1_RX | | AD34 |
| 198 | No AC | ADMA_FLEXCAN1_TX | Available in SOM without AC | AA35 |
| 171 | | ADMA_FLEXCAN1_TX | | AC35 |

***Table 41: FLEXCAN2 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 46 | | ADMA_FLEXCAN2_RX | | AB34 |
| 44 | | ADMA_FLEXCAN2_TX | | AA31 |

## 8.13 LPSPI

The LPSPI is a low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus, either as a master and/or as a slave.
The LPSPI supports:

- Word size = 32 bits
- Configurable clock polarity and clock phase
- Master operation supporting up to 4 peripheral chip select
- Slave operation
- Command/transmit FIFO of 64 words
- Receive FIFO of 64 words
- Flexible timing parameters in master mode, including SCK frequency and delays between PCS and SCK edges
- Support for full duplex transfers supporting 1-bit transmit and receive on each clock edge
- Support for half duplex transfers supporting 1-bit transmit or receive on each clock edge
- Support for half duplex transfers supporting 2-bit or 4-bit transmit or receive on each clock edge (master only)
- Host request input can be used to control the start time of an SPI bus transfer (master only)
- Receive data match logic supporting wakeup on data match

***Table 42: SPI0 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 21 | | ADMA_SPI0_CS0 | | R33 |
| 22 | | ADMA_SPI0_CS1 | | R35 |
| 25 | | ADMA_SPI0_SCK | | P30 |
| 26 | | ADMA_SPI0_SDI | | P34 |
| 24 | | ADMA_SPI0_SDO | | R31 |

***Table 43: SPI1 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 196 | No AC | ADMA_SPI1_CS0 | Available in SOM without AC | M34 |
| 79 | | ADMA_SPI1_CS0 | | AR27 |
| 23 | | ADMA_SPI1_CS1 | | M32 |
| 75 | | ADMA_SPI1_SCK | | L33 |
| 84 | | ADMA_SPI1_SCK | | AK26 |
| 48 | | ADMA_SPI1_SDI | | AP28 |
| 70 | | ADMA_SPI1_SDO | | AM26 |

*Table 44: SPI2 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 39 | | ADMA_SPI2_CS0 | | P28 |
| 80 | | ADMA_SPI2_CS0 | | E23 |
| 75 | | ADMA_SPI2_CS1 | | L33 |
| 43 | | ADMA_SPI2_SCK | | R29 |
| 82 | | ADMA_SPI2_SDI | | D24 |
| 20 | No AC | ADMA_SPI2_SDO | Available in SOM without AC | L29 |
| 45 | | ADMA_SPI2_SDO | | P32 |

*Table 45: SPI3 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 191 | No TP | ADMA_SPI3_CS0 | Available in SOM without TP | J31 |
| 174 | | ADMA_SPI3_CS1 | | K30 |
| 189 | No TP | ADMA_SPI3_SCK | Available in SOM without TP | H32 |
| 193 | No TP | ADMA_SPI3_SDI | Available in SOM without TP | G33 |
| 187 | No TP | ADMA_SPI3_SDO | Available in SOM without TP | F34 |

## 8.14 QSPI

The VAR-SOM-MX8X exports one QSPI channel for connection of up to 4 external devices supporting Single/Dual/Quad/ mode data transfer (1/2/4 bidirectional data lines).
The QSPI is available only in SOMs with the “No ADC” assembly option

Key features of QSPI are:

- Flexible sequence engine to support various flash vendor devices.
- Support for FPGA interface
- Single, dual, quad, mode of operation.
- DDR/DTR mode wherein the data is generated on every edge of the serial flash clock.
- Support for flash data strobe signal for data sampling in DDR and SDR mode.
- Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.
- Multi-master accesses with priority
- Flexible and configurable buffer for each master
- Thirteen interrupt conditions
- Memory mapped read access to connected flash devices.
- Programmable sequence engine to cater to future command/protocol changes and able to support all existing vendor commands and operations.
- Supports 3-byte and 4-byte addressing.
- LUT size is 512B

*Table 46: QSPI0B Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 142 | No ADC | LSIO_QSPI0B_DATA0 | | AM10 |
| 141 | No ADC | LSIO_QSPI0B_DATA1 | | AL9 |
| 140 | No ADC | LSIO_QSPI0B_DATA2 | | AJ11 |
| 143 | No ADC | LSIO_QSPI0B_DATA3 | | AM8 |
| 145 | No ADC | LSIO_QSPI0B_DQS | | AK10 |
| 147 | No ADC | LSIO_QSPI0B_SCLK | | AR11 |
| 117 | | LSIO_QSPI0B_SS0_B | | AH10 |
| 86 | | LSIO_QSPI0B_SS1_B | | AJ9 |

## 8.15 Keypad

The VAR-SOM-MX8X exports a 4x4 Keypad matrix available on SOM with “No ADC” assembly option.

Keypad Key Features:

- Supports up to an 8 x 8 external key pad matrix
- Port pins can be used as general purpose I/O
- Open drain design
- Glitch suppression circuit design
- Multiple-key detection
- Long key-press detection
- Standby key-press detection
- Synchronizer chain clear
- Supports a 2-point and 3-point contact key matrix

*Table 47: Keypad Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 147 | No ADC | LSIO_KPP0_COL0 | | AR11 |
| 142 | No ADC | LSIO_KPP0_COL1 | | AM10 |
| 141 | No ADC | LSIO_KPP0_COL2 | | AL9 |
| 140 | No ADC | LSIO_KPP0_COL3 | | AJ11 |
| 143 | No ADC | LSIO_KPP0_ROW0 | | AM8 |
| 145 | No ADC | LSIO_KPP0_ROW1 | | AK10 |
| 117 | | LSIO_KPP0_ROW2 | | AH10 |
| 86 | | LSIO_KPP0_ROW3 | | AJ9 |

## 8.16 PWM

The VAR-SOM-MX8X exports 4 General purpose Pulse Width Modulators (PWM) signals.
In addition, there are 2 dedicated PWM signals for DSI0, DSI1, LCD interfaces.
PWM Features:

- 16-bit up-counter with clock source selection (bus clock, baud clock, or 32K)
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

***Table 48: PWM Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 124 | | LSIO_PWM0_OUT | | H34 |
| 175 | | LSIO_PWM1_OUT | | L31 |
| 69 | | LSIO_PWM2_OUT | | N29 |
| 68 | | LSIO_PWM3_OUT | | K32 |
| 22 | | ADMA_LCD_PWM0 | | R35 |
| 17 | | MIPI_DSI0_PWM0_OUT | | AD32 |
| 92 | | MIPI_DSI1_PWM0_OUT | | AD30 |

## 8.17 I2C

The SOM consists of 3 I2C Interface connectivity peripherals which provides serial interface for external devices. Data rates of up to 400 kbps are supported.
In addition, there are dedicated low-speed I2C non-DMA I2C busses for MIPI-CSI, CSI.

***Table 49: I2C1 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 17 | | ADMA_I2C1_SCL | | AD32 |
| 88 | | ADMA_I2C1_SCL | | F14 |
| 42 | | ADMA_I2C1_SCL | Pin Used for Boot mode setting,<br>Please see Boot Configuration section. | H14 |
| 87 | | ADMA_I2C1_SDA | | G15 |

***Table 50: I2C2 Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 92 | | ADMA_I2C2_SCL | | AD30 |
| 90 | | ADMA_I2C2_SDA | | AF34 |

*Table 51: I2C3 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 174 | | ADMA_I2C3_SCL | | K30 |
| 48 | | ADMA_I2C3_SCL | | AP28 |
| 74 | | ADMA_I2C3_SCL | Pin alternate function cannot be changed when using SOM with EC assembled | D30 |
| 176 | | ADMA_I2C3_SDA | | M28 |
| 79 | | ADMA_I2C3_SDA | | AR27 |
| 30 | | ADMA_I2C3_SDA | Pin alternate function cannot be changed when using SOM with EC assembled | B32 |

*Table 52: Parallel CSI I2C Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 48 | | CI_PI_CSI_I2C_SCL | | AP28 |
| 79 | | CI_PI_CSI_I2C_SDA | | AR27 |

*Table 53: MIPI CSI I2C Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 84 | | MIPI_CSI0_I2C0_SCL | | AK26 |
| 70 | | MIPI_CSI0_I2C0_SDA | | AM26 |

## 8.18 Analog to Digital Converter

The VAR-SOM-MX8X exports 6 channels of 12-bit successive approximation ADC interface. ADC SoC balls are exported only in SOM configurations with “ADC” assembly option ADC inputs are referenced to 1.8v.

*Table 54: Analog to Digital Converter Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 140 | ADC | ADMA_ADC_IN0 | Available in SOM with ADC (referenced to 1.8V) | U35 |
| 142 | ADC | ADMA_ADC_IN1 | Available in SOM with ADC (referenced to 1.8V) | U33 |
| 141 | ADC | ADMA_ADC_IN2 | Available in SOM with ADC (referenced to 1.8V) | V32 |
| 143 | ADC | ADMA_ADC_IN3 | Available in SOM with ADC (referenced to 1.8V) | V30 |
| 147 | ADC | ADMA_ADC_IN4 | Available in SOM with ADC (referenced to 1.8V) | W29 |
| 145 | ADC | ADMA_ADC_IN5 | Available in SOM with ADC (referenced to 1.8V) | V34 |

## 8.19 General Purpose Timer

Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

***Table 55: General Purpose Timer Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 124 | | LSIO_GPT0_CAPTURE | | H34 |
| 69 | | LSIO_GPT0_CLK | | N29 |
| 175 | | LSIO_GPT0_COMPARE | | L31 |
| 69 | | LSIO_GPT1_CAPTURE | | N29 |
| 175 | | LSIO_GPT1_CLK | | L31 |
| 68 | | LSIO_GPT1_COMPARE | | K32 |

## 8.20 Flex Timer (FTM)

The SOM exports a 3 channel Flex timer module (FTM) supporting input capture, output compare, and generation of PWM signals.

***Table 56: General Purpose Timer Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 115 | | ADMA_FTM_CH0 | | AD34 |
| 171 | | ADMA_FTM_CH1 | | AC35 |
| 18 | No AC | ADMA_FTM_CH2 | Available in SOM without AC | AA33 |

## 8.21 System Control Unit

The System Controller Unit (SCU) is made of a Cortex-M4 processor running at 266MHz with 256KB of TCM and a set of peripherals and interfaces to connect to external PMIC and to control internal subsystems. The SCU Cortex-M4 is the first processor to boot the chip (see System Boot). The SCU is responsible for:

- Booting the system
- Interfacing with the external PMIC through a dedicated I2C and dedicated pins
- Managing power, clocking, and reset of internal subsystems
- Controlling pin multiplexing and IO control (drive strength and pull up/down)
- Managing resource partitioning through isolation (see xRDC chapter)
- Managing thermal

***Table 57: System Control Unit Signals***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 146 | | SCU_DSC_BOOT_MODE1 | Pin Used for Boot mode setting,<br>Please see Boot Configuration section.<br>(referenced to 1.8V) | AK32 |
| 83 | | SCU_GPIO0_IO00 | Pin is routed via on SOM buffer, set as Input by default.<br>Pin direction can be controlled by GPIO1_26:<br>Low - Output from SoC<br>High - Input to SoC | AF28 |
| 85 | | SCU_GPIO0_IO01 | Pin is routed via on SOM buffer set as Output by default.<br>Pin direction can be controlled by GPIO1_25:<br>Low - Output from SoC<br>High - Input to SoC | AH30 |
| 53 | | SCU_UART0_RX | Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | AB32 |
| 83 | | SCU_UART0_RX | Pin is routed via on SOM buffer, set as Input by default.<br>Pin direction can be controlled by GPIO1_26:<br>Low - Output from SoC<br>High - Input to SoC | AF28 |
| 52 | | SCU_UART0_TX | Used internally in SOM with "WBD" Configuration.<br>Interface can be released by GPIO control. | AA29 |
| 85 | | SCU_UART0_TX | Pin is routed via on SOM buffer set as Output by default.<br>Pin direction can be controlled by GPIO1_25:<br>Low - Output from SoC<br>High - Input to SoC | AH30 |

## 8.22 JTAG

The SOM consists of the System JTAG Controller (SJC) which provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

***Table 58: JTAG signals 10-pin Header Connector***

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 1 | | JTAG_VTREF | JTAG reference voltage (3.3v) | |
| 2 | | JTAG_TMS | JTAG Test Mode select | AG35 |
| 3 | | GND | Digital Ground | |
| 4 | | JTAG_TCK | JTAG Test Clock | AE31 |
| 5 | | GND | Digital Ground | |
| 6 | | JTAG_TDO | JTAG Test Data Out | AF32 |
| 7 | | RTCK | JTAG Return clock | |
| 8 | | JTAG_TDI | JTAG Test Data In | AH34 |
| 9 | | JTAG_TRST_B_CONN | JTAG TAP reset | |
| 10 | | JTAG_SRST_B | JTAG System reset | |

## 8.23 Cortex M4

The SOM features one configurable Cortex-M4 subsystem and a dedicated Cortex-M4 subsystem within the SCU. The modular set of Cortex-M4 platform components offer a low-latency execution environment with real-time and low-power processing capability. Along with the processor components, the Cortex-M4 subsystem features several off platform components. These off-platform components and subsystem features include:

- WDOG (watchdog) timer
- LPIT (Low-power Periodic Interrupt Timer) for periodic timer services
- TPM (Timer PWM Module) for timer and PWM services
    - 32-bit counters
- LPCG (Low-Power Clock Gating) for local clock management
- TSTMR (Timestamp Timer) for global timer services
    - Receives system time bus driven by system counter
- Power mode control
    - Programming model for power mode request
    - Low-power bus connected to SC to support power mode transitions
- Reset control and status
- MU (Messaging Unit) for inter-processor communication
    - MU0 with 4 channels inside the GP CM4 domain
    - MU1 with 1 channel which is inside the DSC. The latter is talked to over an asynchronous bus.
- LPI2C (Low-Power I2C) for serial communication
    - Standard features (FEATURE_EN = 1)
    - Slave mode logic enabled (SLAVE_EN = 1)
    - TX FIFO size of 4 entries (TXFIFO_SZ = 2)
    - RX FIFO size of 4 entries (RXFIFO_SZ = 2)
- LPUART (Low-Power UART) for serial communication and debug
    - Standard functionality with MODEM/IrDA (FEATURE_EN = 2)
    - TX FIFO size of 32 entries (TXFIFO_SZ = 5)
    - RX FIFO size of 5(RXFIFO_SZ = 5)
- RGPIO (Rapid General-Purpose Input/Output) for fast pin I/O capability
    - Dual access (AIPS and AHB access from system peripheral address space)
- INTMUX (Interrupt Mux) to select local interrupts routed outside of the subsystem
- SEMA42 (hardware semaphore) for HMP synchronization to shared resources

*Table 59: Cortex M4 GPIO Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 25 | | M40_GPIO0_IO00 | | P30 |
| 140 | ADC | M40_GPIO0_IO00 | Available in SOM with ADC (referenced to 1.8V) | U35 |
| 24 | | M40_GPIO0_IO01 | | R31 |
| 142 | ADC | M40_GPIO0_IO01 | Available in SOM with ADC (referenced to 1.8V) | U33 |
| 26 | | M40_GPIO0_IO02 | | P34 |
| 141 | ADC | M40_GPIO0_IO02 | Available in SOM with ADC (referenced to 1.8V) | V32 |
| 21 | | M40_GPIO0_IO03 | | R33 |
| 143 | ADC | M40_GPIO0_IO03 | Available in SOM with ADC (referenced to 1.8V) | V30 |
| 147 | ADC | M40_GPIO0_IO04 | Available in SOM with ADC (referenced to 1.8V) | W29 |
| 145 | ADC | M40_GPIO0_IO05 | Available in SOM with ADC (referenced to 1.8V) | V34 |

*Table 60: Cortex M4 UART Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 141 | ADC | M40_UART0_RX | Available in SOM with ADC (referenced to 1.8V) | V32 |
| 83 | | M40_UART0_RX | Pin is routed via on SOM buffer, set as Input by default. Pin direction can be controlled by GPIO1_26:<br>Low - Output from SoC<br>High - Input to SoC | AF28 |
| 143 | ADC | M40_UART0_TX | Available in SOM with ADC (referenced to 1.8V) | V30 |
| 85 | | M40_UART0_TX | Pin is routed via on SOM buffer set as Output by default. Pin direction can be controlled by GPIO1_25:<br>Low - Output from SoC<br>High - Input to SoC | AH30 |

*Table 61: Cortex I2C0 M4 Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 25 | | M40_I2C0_SCL | | P30 |
| 140 | ADC | M40_I2C0_SCL | Available in SOM with ADC (referenced to 1.8V) | U35 |
| 24 | | M40_I2C0_SDA | | R31 |
| 142 | ADC | M40_I2C0_SDA | Available in SOM with ADC (referenced to 1.8V) | U33 |

*Table 62: Cortex M4 Timer and PWM Module Signals*

| Pin # | Assy | PIN Function | Notes | Ball |
|---|---|---|---|---|
| 26 | | M40_TPM0_CH0 | | P34 |
| 147 | ADC | M40_TPM0_CH0 | Available in SOM with ADC (referenced to 1.8V) | W29 |
| 21 | | M40_TPM0_CH1 | | R33 |
| 145 | ADC | M40_TPM0_CH1 | Available in SOM with ADC (referenced to 1.8V) | V34 |

## 8.24 General Purpose IO

The SOM provides IO pins which can be used as GPIOs. See Chapter 7 for a complete SOM connectors' signal list and GPIO multiplexing.

# 9. Power and control

## 9.1 Power

***Table 63: Power***

| Pin # | PIN Function | Notes |
|---|---|---|
| 32,34,103,105,107,109, 111 | VBAT | VARS-SOM-MX8X single 3.3V supply voltage input |
| 36 | LICELL | RTC back-up battery 1.8V/3.0V/3.3V supply voltage input |
| 38 | VDD_ENET1_1P8_2P5_3P3_IN | VAR-SOM-MX8X 1.8V/2.5V/3.3V supply voltage input.<br><br>The following SOM pins are referenced to this voltage:<br>40,54,55,56,57,71,73,81,96,113,120,122,177<br><br>When using the above pins for alternate functions of ENET1:<br>• For RMII - voltage supply should be 3.3V<br>• For RGMII - voltage supply should be 1.8V/2.5V |
| 104 | USB_OTG1_VBUS | USB Host VBUS (5V) input |
| 106 | USB_OTG2_VBUS | USB OTG VBUS (5V) input |

## 9.2 Ground

***Table 64: Digital Ground Pins***

| Pin # | PIN Function | Notes |
|---|---|---|
| 1,2,7,8,13,14,19,27,28, 37,47,58,59,66, 67,76, 78,89,95,101,112, 118,126,132,138,139, 144,149,158,159,169, 172,178,179,185 | GND | Digital ground |
| 195 | AGND | Audio Interface ground reference |

## 9.3 General System Control Signals

***Table 65: General System Control Signals***

| Pin # | PIN Function | Notes |
|---|---|---|
| 49 | SW_3P3 | SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply.<br>Connect to pin 38 in case of 3.3V supply. |
| 98 | POR_B_3V3 | System Reset Input. Active on falling edge. A logic low '0' on this pin will reset the system. |

## 9.4 Boot Configuration

***Table 66: SOM boot options***

| | Pin # 146 (SCU_BOOT_MODE1) | Pin # 42 (USB_SS3_TC1) | Notes |
|---|---|---|---|
| Fuse boot | 0 | 1 or float | 1) Pin 42 is pulled High internally on SOM, referenced to 3.3V.<br>2) Pin 146 is pulled high internally on SOM, referenced to 1.8V.<br>3) To set to logic '1' or '0' externally use strong pull - 1K Ohm or less. |
| Serial Boot | 0 | 0 | |
| eMMC Boot | 1 or float | 1 or float | |
| SD Boot | 1 or float | 0 | |

# 10. Assembly options

To make the solution as Flexible as possible the following assembly options were added. The assembly options help customers to order the SOM subversion that include only the needed interfaces with a lower cost.

## 10.1 ADC

The SOM can be ordered with ADC interface exposed, this allows connection to ADC inputs. In this special configuration SOM pins exported are referenced to 1.8V.

***Table 67: ADC assembly options***

| Pin # | Default SOM option | | Special SOM option | |
|---|---|---|---|---|
| | Pin name | Ball | Pin name | Ball |
| 140 | QSPI0B_DATA2 | AJ11 | ADC_IN0 | U35 |
| 141 | QSPI0B_DATA1 | AL9 | ADC_IN2 | V32 |
| 142 | QSPI0B_DATA0 | AM10 | ADC_IN1 | U33 |
| 143 | QSPI0B_DATA3 | AM8 | ADC_IN3 | V30 |
| 145 | QSPI0B_DQS | AK10 | ADC_IN5 | V34 |
| 147 | QSPI0B_SCLK | AR11 | ADC_IN4 | W29 |

## 10.2 Analog Audio Codec

The SOM can be ordered without Audio Codec chip assembled, it allows reducing the overall cost of the product in case the Analog Audio is not used.
When not assembled, the SoC balls which are normally connected to Codec are routed to SOM connector and exported on Analog codec interface pins.

***Table 68: AC assembly options***

| Pin # | Default SOM option | | Special SOM option | |
|---|---|---|---|---|
| | Pin name | Ball | Pin name | Ball |
| 18 | DMIC_CLK | WM8904CGEFL.1 | FLEXCAN1_RX | AA33 |
| 20 | DMIC_DATA | WM8904CGEFL.27 | MCLK_OUT0 | L29 |
| 196 | HPOUTFB | WM8904CGEFL.14 | SAI0_RXD | M34 |
| 197 | LINEIN1_LP | WM8904CGEFL.26 | SAI0_TXD | K34 |
| 198 | HPLOUT | WM8904CGEFL.13 | FLEXCAN1_TX | AA35 |
| 199 | LINEIN1_RP | WM8904CGEFL.24 | SAI1_RXFS | N35 |
| 200 | HPROUT | WM8904CGEFL.15 | SAI1_RXC | L35 |

## 10.3 Resistive Touch

The SOM can be ordered without Resistive Touch controller assembled, it allows reducing the overall cost of the product in case the Resistive Touch is not used.
When not assembled, the SoC balls which are normally connected to Resistive Touch are routed to SOM connector and exported on Resistive Touch interface pins.

***Table 69: TP assembly option***

| Pin # | Default SOM option | | Special SOM option | |
|---|---|---|---|---|
| | Pin name | Ball | Pin name | Ball |
| 187 | TS_X+ | TSC2046.6 | SPI3_SDO | F34 |
| 189 | TS_Y+ | TSC2046.7 | SPI3_SCK | H32 |
| 191 | TS_X- | TSC2046.8 | SPI3_CS0 | J31 |
| 193 | TS_Y- | TSC2046.9 | SPI3_SDI | G33 |

## 10.4 Ethernet PHY

The SOM can be ordered without Ethernet0 PHY chip assembled, it allows reducing the overall cost of the product in case the Ethernet Interfaces are not used.

## 10.5 Dual band Wi-Fi and BT/BLE combo

The SOM can be ordered without the Dual band Wi-Fi and BT/BLE combo chip assembled, it allows reducing the overall cost of the product in case the Wi-Fi and BT/BLE is not used.

## 10.6 Bluetooth

The SOM can be ordered with UART0 interface not connected to WiFi/Bluetooth module. In this case the Bluetooth interface will not be available. For testing purposes same operation can be achieved by pulling GPIO1_29 high. It will disable ON-SOM level translator and allow UART0 operation externally.

## 10.7 LPDDR4

The SOM can be ordered with different RAM size capacities, it allows reducing the overall cost of the product in case lower RAM size is sufficient.

## 10.8 eMMC

The SOM can be ordered with different eMMC size capacities, it allows reducing the overall cost of the product in case lower eMMC size is sufficient.

# 11. Electrical specifications

## 11.1 Absolute maximum ratings

***Table 70: Absolute Maximum Ratings***

| Pin # | Min | Max | Units | Comments |
|---|---|---|---|---|
| VBAT | -0.3 | 3.6 | V | |
| LICELL | -0.3 | 5.5 | V | |
| USB_OTG1_VBUS/ USB_OTG2_VBUS | -0.3 | 5.5 | V | |
| USB_OTG1_DP/USB_OTG1_DN<br>USB_OTG2_DP/USB_OTG2_DN | -0.3 | 3.63 | V | |
| VDD_ENET1_1P8_2P5_3P3_IN | -0.3 | 3.8 | V | |
| ADC_Inx I/O Voltage | -0.1 | 2.1 | V | |
| Vin/Vout input/output voltage range (GPIO Type Pins) | -0.3 | Refer to i.MX8X Datasheet section 4.6.1 | V | OVDD is the I/O supply voltage |
| ESD damage immunity<br>Human Body Model (HBM) | — | 2000 | V | PCIe differential pairs and USB3 (including OTG2) interfaces are 1000V HBM instead of 2000V |
| ESD damage immunity<br>Charge Device Model (CDM) | — | 500 | V | PCIe differential pairs and USB3 (including OTG2) interfaces are 250V HBM instead of 500V |

## 11.2 Operating conditions

***Table 71: Operating Ranges***

| Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VBAT | | 3.25 | 3.3 | 3.45 | V |
| LICELL | | - | - | 4.2 | V |
| VDD_ENET1_1P8_2P5_3P3_IN | 1.8 | 1.65 | 1.8 | 1.95 | V |
| | 2.5 | 2.4 | 2.5 | 2.6 | |
| | 3.3 | 3 | 3.3 | 3.6 | |

## 11.3 Power consumption

***Table 72: VAR-SOM-MX8X Power Consumption***

| Mode | Voltage | Current | Power | Conditions |
|---|---|---|---|---|
| Run | 3.3V | 0.77A | 2.54W | Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz |
| Run | 3.3V | 0.64A | 2.11W | Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz |
| Run | 3.3V | 0.44A | 1.45W | Linux up |
| Standby | 3.3V | TBD | TBD | Memory retention mode |
| Off (RTC) | 3V | 0.12mA | 0.36mW | All power rails are Off, only Internal SOC RTC is powered |

***NOTE***

Setup:
HW: VAR-SOM-MX8XQP_1200C_2048R_16G_AC_EC_TP_WBD_ET_REV1.11
SW: imx8x-var-som-emmc-wifi.dtb

**DISCLAIMER:**
**The power consumption measurements apply only to limited operation scenarios. Actual power consumption may vary depending on the interfacing peripherals and user application modes; Users must conduct testing per their specific operation scenarios.**

# 12. Environmental Specifications

***Table 73: Environmental Specifications***

| Parameter | Min | Max |
|---|---|---|
| Extended Operating Temperature Range | -25°C | 85°C |
| Industrial Operating Temperature Range | -40°C | 85°C |
| Storage temperature | -40°C | 85°C |
| Relative humidity (operation) | 10% | 90% |
| Relative humidity (storage) | 05% | 95% |
| Referring Telcordia Technologies Special Report SR-332, Issue 4 Reliability Prediction Method Model:<br>25Deg Celsius, Class B-1, GM | TBD | |

Note: Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

# 13. Mechanical Drawings

## 13.1 Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-2.5-M2-B**

## 13.2 Thermal Management

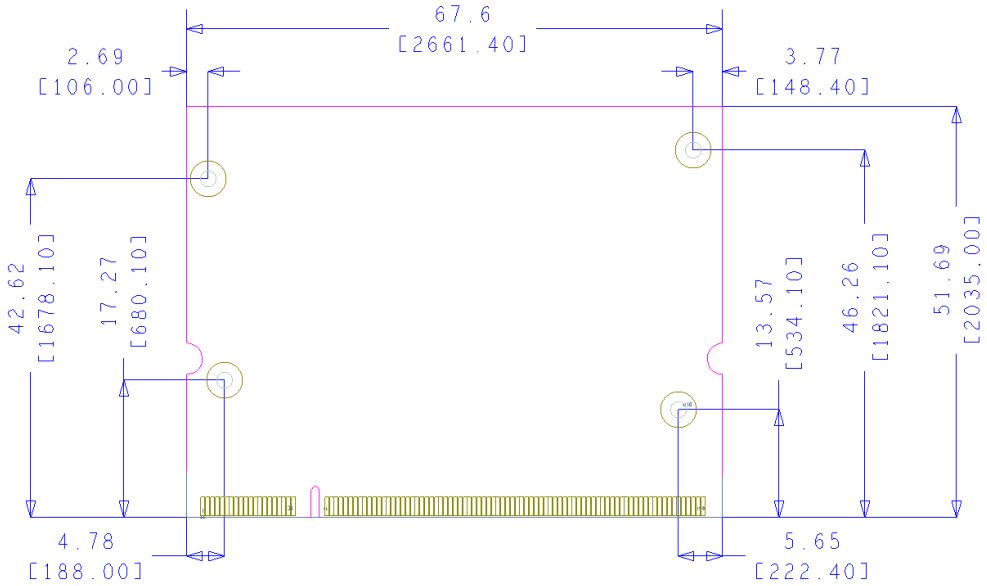
Certain operation scenarios may prompt the use of an external heat dissipation solution.
To handle intensive applications where thermal management is required, Variscite offers a heat sink designed for the VAR-SOM-MX8/X:

Variscite PN: VHP-MX8

**DISCLAIMER:**
**Implemented solution may vary depending on the device operation scenario as well as its mechanical design. Thermal solution must be evaluated.**

## 13.3 SOM Dimensions

**Figure 5: VAR-SOM-MX8X Mechanics in millimeters [mils]**



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