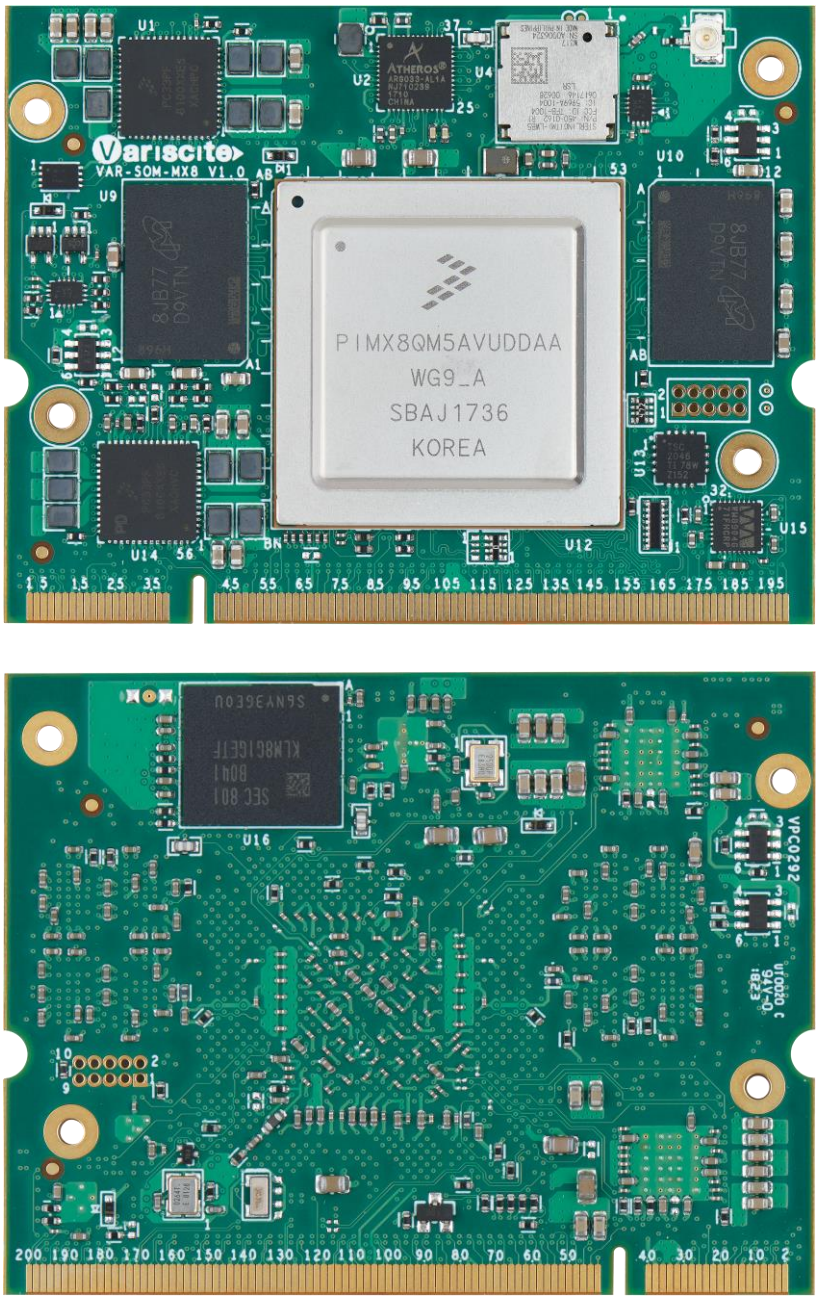
VARISCITE LTD.

VAR-SOM-MX8 V1.x Datasheet

NXP i.MX 8QM/QP™ - based System-on-Module



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VAR-SOM-MX8 Datasheet

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1. Document Revision History

Revision	Date	Notes
1.0	Apr 2, 2019	Initial - Preliminary
1.01	May 15, 2019	Updated pins 67,76,78,174,176 sections 7.4,7.5,8.15 ,9 Updated SOM assembly options sections 6,10
1.02	May 26, 2019	Updated sections 4.3, 9.4
1.03	Jul 18, 2019	Updated block diagram section 4.3
1.04	Oct 24, 2019	Updated section 11.3 Updated note section 8.1.1 Renamed “AUX” to “DP” in pinmux tables
1.05	Feb 9, 2020	Updated notes for pins 39,41,43,45 Tables 2,35,37
1.06	June 18, 2020	Updated tables 3,60 removed ADC
1.07	Aug 23, 2020	Updated RAM max capacity to 8GB sections 4.2,5.2
1.08	Oct 21, 2020	Added note for SOM pin 29 – Tables 2, 7
1.09	Nov 4, 2021	Updated block Diagram Added EEPROM section 5.8 Updated section 12 Table 63 Added support for i.MX 8QuadPlus
1.10	Jan 3, 2022	Added section 8.1.3
1.11	May 1, 2022	Updated sections: 4.2, 5.4
1.12	June 7, 2022	Added Ethernet PHY ADIN1300 – Updated sections 5.6, 7.4, 8.3 Updated section 5.3 Corrected note for pin 98 Updated note on PCIE pins 100,102 sections 7.4, 8.9 Updated section 13 SMT spacer P/N
1.13	Sep 14, 2022	Updated section 13.2
1.14	Jan 3, 2023	Updated Key Features section 5.4
1.15	Feb 26, 2023	Updated section 12 Updated the eMMC on sections 4.2, 5.2

2. Table of Contents

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4. Overview

4.1 General Information

The VAR-SOM-MX8 offers a high-performance processing for a low-power System-on-Module. The product is based on the NXP i.MX 8QuadMax/QuadPlus comprehensive multimedia device targeting high-end automotive and industrial market segments. The chip is built using a leading edge process to achieve both high performances and low-power consumption. The chip relies on a powerful fully-coherent core complex based on a dual (2x) /single (1x) Cortex-A72 cluster for use-cases requiring high computing performances and a quad (4x) Cortex-A53 cluster running most of the use cases at a lower-power consumption.

Graphics processing is handled by two (2x) Graphics Processing Units (GPU) supporting the latest graphic APIs including OpenVX for computer vision. Video is managed by a dedicated video engine decoding formats including HEVC (H.265) up to 4K60, and encoding in H.264 up to 1080p60. The chip provides various display interfaces that supports up to four displays.

This heterogeneous multicore processing architecture enables the device to run an open operating system like Linux and an RTOS like FreeRTOS™ on the Cortex-M4 core for time and security critical tasks.

The VAR-SOM-MX8 provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

- Symphony-Board – evaluation board
  - ✓ Carrier Board, compatible with VAR-SOM-MX8
  - ✓ Schematics
- VAR-DVK-MX8 full development kit, including:
  - ✓ Symphony-Board
  - ✓ VAR-SOM-MX8
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

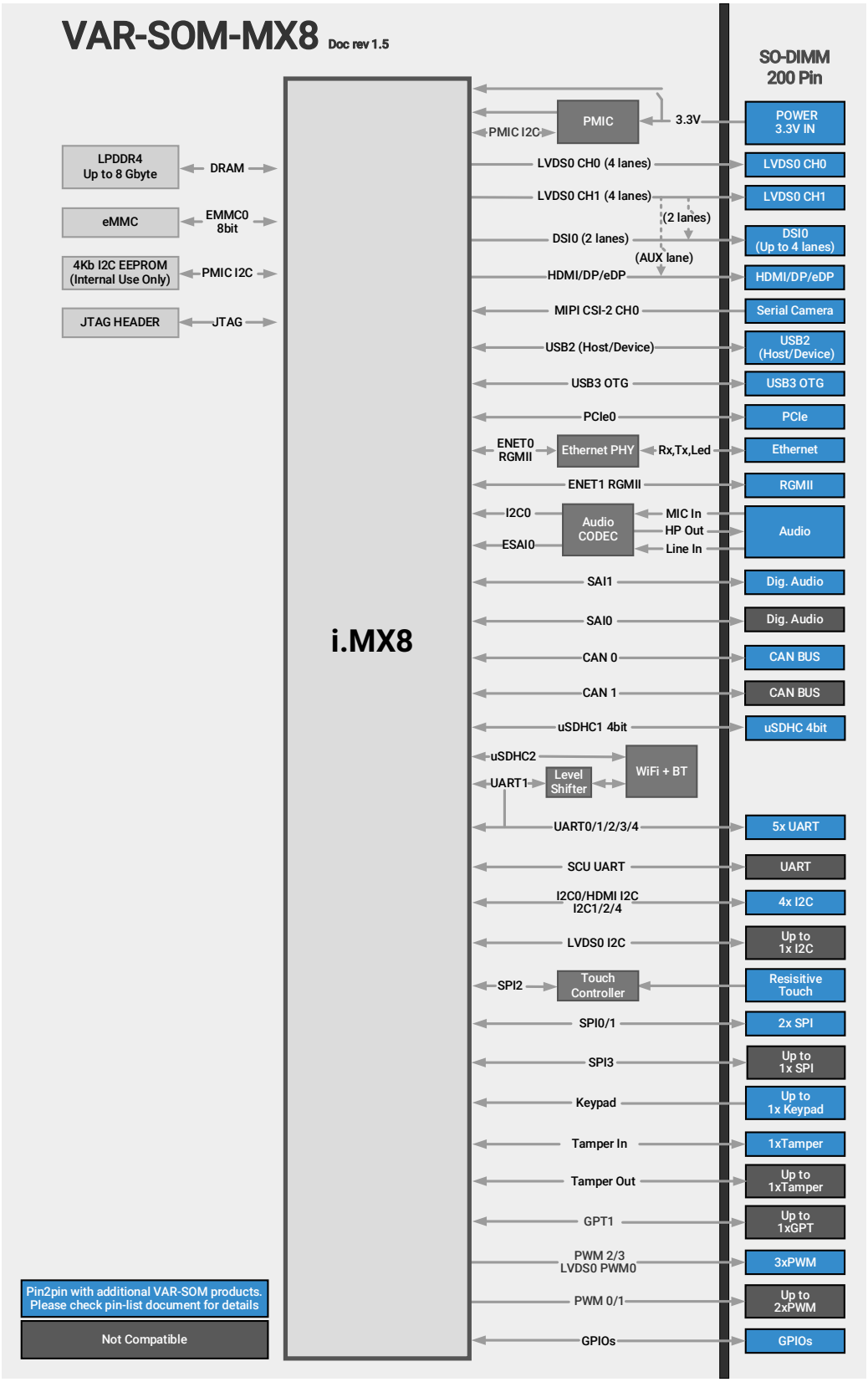
Contact Variscite support services for further information: mailto:support@variscite.com.

4.2 Feature Summary

- NXP i.MX 8QuadMax/QuadPlus series SOC
  - QuadMax: 4x Cortex A53 up to @ 1.2 GHz + 2x Cortex A72 up to @ 1.6 GHz
    QuadPlus: 4x Cortex A53 up to @ 1.26 GHz + 1x Cortex A72 up to @ 1.6 GHz
  - 2x Cortex M4 @ 264 MHz
  - Up to 8GB LPDDR4 RAM @ 1600Mhz
  - 8-bit up to 128GB eMMC boot and storage
- Display Support
  - 2x LVDS interface 4-lane each, up to 1080p60
  - HDMI/eDP/DP
  - 1x MIPI DSI with up to 4 data lanes
- Networking
  - 2x 10/100/1000 Mbit/s Ethernet Interface
  - Certified Wi-Fi 802.11 ac/a/b/g/n
  - Bluetooth: 5.2/BLE
- Camera
  - 1x MIPI CSI – CMOS Serial camera Interface 4 lanes.
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - 2x Digital audio (SAI)
- USB
  - 1x USB 3.0/2.0 OTG
  - 1x USB 2.0 Host/Device
- Other Interfaces
  - SDIO/MMC
  - 1x PCIe v3.0
  - Resistive touch controller
  - Serial interfaces (FlexSPI, I2C, UART, CAN, JTAG)
  - GPIOs
- Single power supply: 3.3V
- Dimensions (W x L x H): 67 mm x 51.6 mm x 4.97mm
- Industrial temperature range -40°C to 85°C

4.3 Block Diagram

Figure 1 : VAR-SOM-MX8 Block Diagram



5. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-MX8.

5.1 NXP i.MX 8QuadMax/QuadPlus

5.1.1 Overview

The i.MX 8QuadMax/QuadPlus is a fully comprehensive multimedia device targeting high-end automotive and industrial market segments. The chip is built using a leading-edge process to achieve both high performances and low-power consumption. The chip relies on a powerful fully-coherent core complex based on a dual (2x) / single (1x) Cortex-A72 cluster for use-cases requiring high computing performances and a quad (4x) Cortex-A53 cluster running most of the use cases at a lower-power consumption.
Graphics processing is handled by two (2x) Graphics Processing Units (GPU) supporting the latest graphic APIs including OpenVX for computer vision. Video is managed by a dedicated video engine decoding formats including HEVC (H.265) up to 4K60 and encoding in H.264 up to 1080p60. The chip provides various display interfaces that supports up to four displays.
To feed data to those high demanding blocks, i.MX 8QuadMax/QuadPlus has two DRAM controllers supporting DDR4 and LPDDR4 memory types.

The i.MX 8QuadMax/QuadPlus provides additional computing resources and peripherals:

- A dedicated system control unit and a dedicated security subsystem which provides High Assurance Boot (HAB) features and cryptographic acceleration
- An audio sub-system with a wide range of audio interfaces
- Two general purpose Cortex-M4 with their own off-platform peripherals
- A large set of peripherals that are commonly used in automotive and industrial markets

5.1.2 i.MX 8QuadMax/QuadPlus Block Diagram

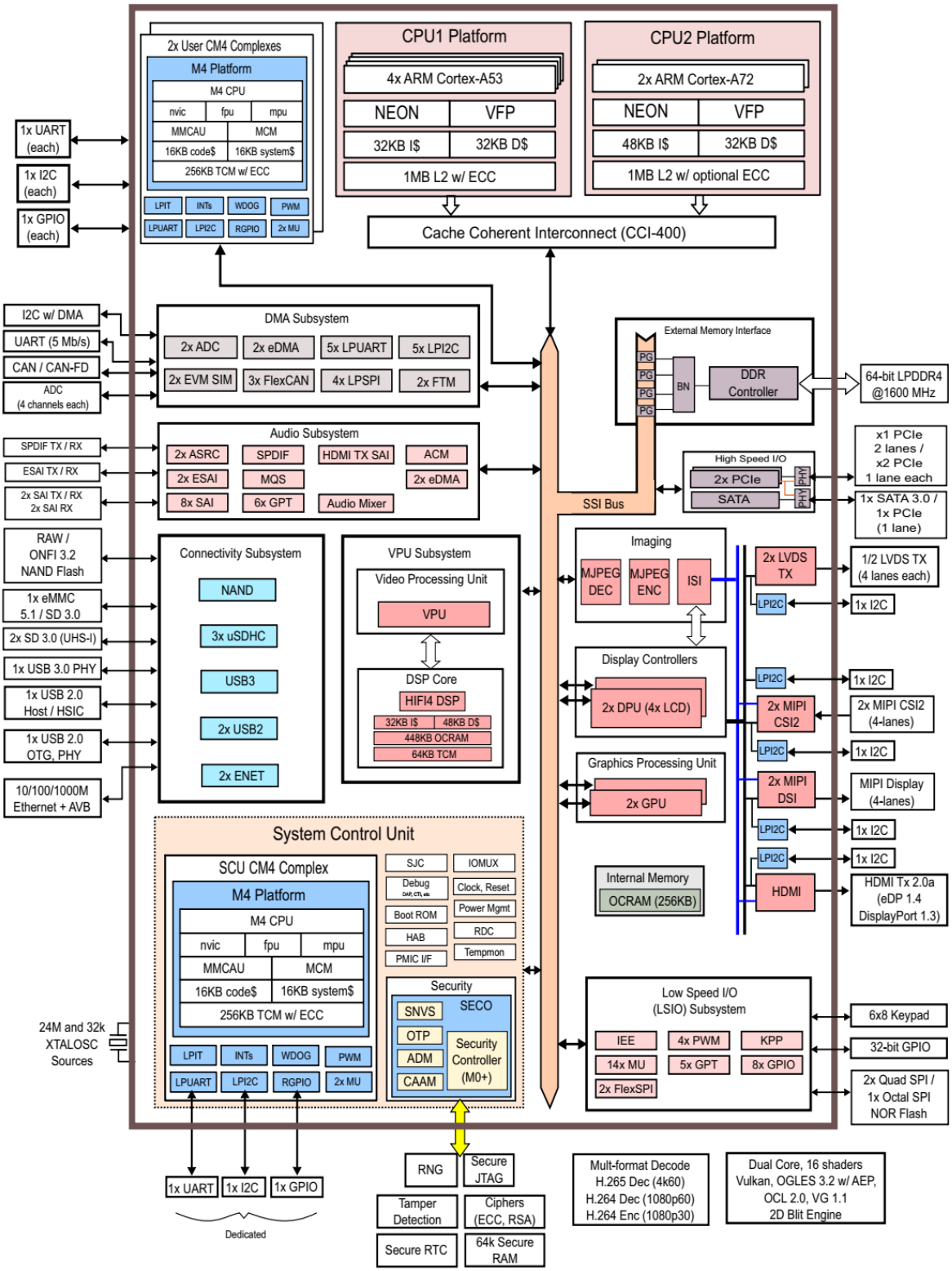


Figure 2 : i.MX8QuadMax Block Diagram

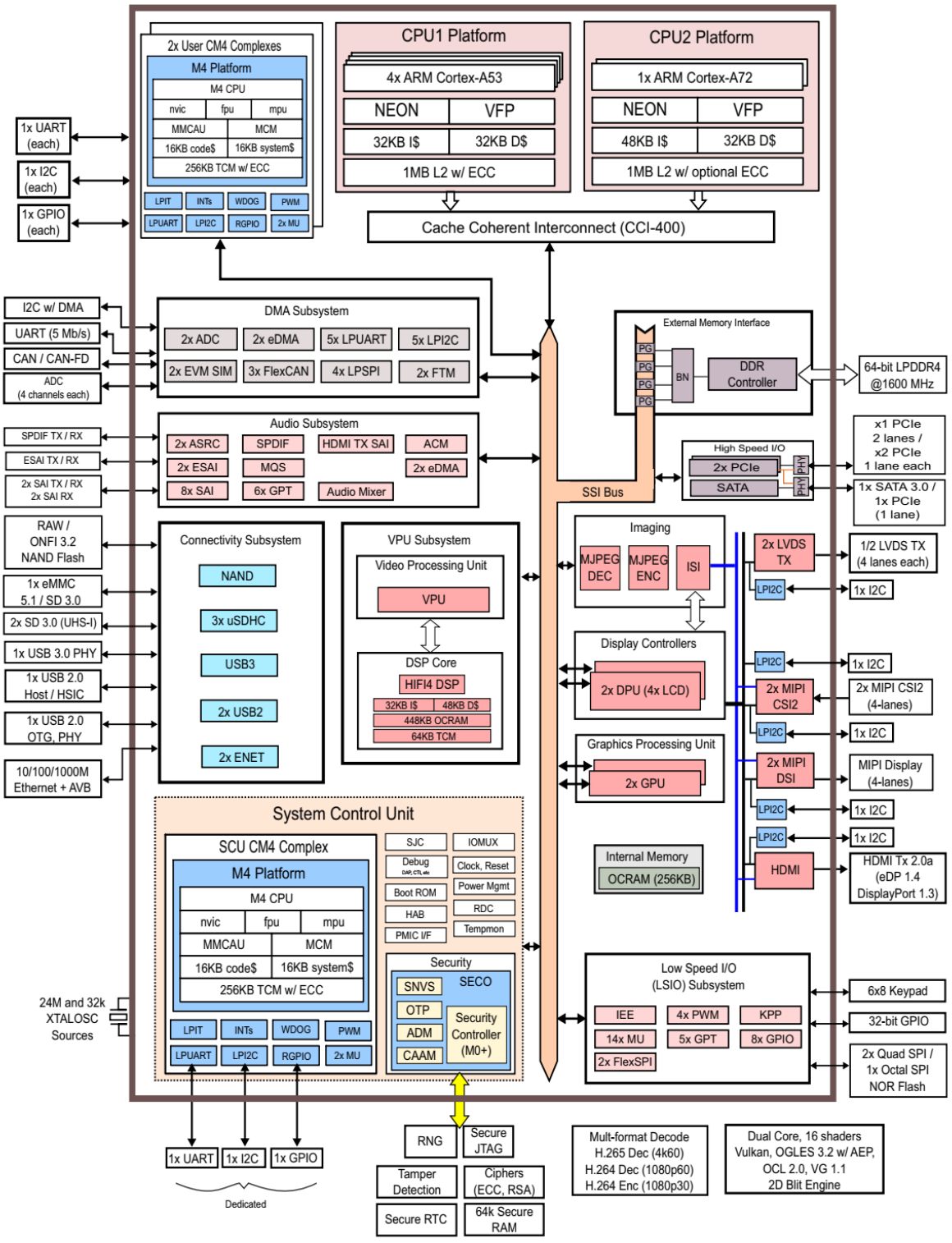


Figure 3 : i.MX8QuadPlus Block Diagram

5.1.3 ARM Cortex-A53 MPCore™ Platform

The i.MX 8QuadMax/QuadPlus family Applications Processors are based on the ARM Cortex-A53 MPCore™ platform, which has the following features:

- 4x cores
- L1 instruction cache 32K with parity
- L1 data cache 32K with SECDED
- Advanced SIMD (NEON) per core
- Crypto extension per core
- CPU cache protection per core
- AMBA 4 ACE interface
- 1MB of L2 Cache
  - 1M with SECDED
  - Input latency 2 cycles
  - Output latency 2 cycles
  - SCU-L2 cache protection

5.1.4 Arm Cortex A72 Platform

Cortex-A72 core platform includes the following features:

- 2x / 1x cores
- L1 instruction cache 48K with parity
- L1 data cache 32K
- Advanced SIMD (NEON) per core
- Crypto extension per core
- CPU cache protection per core
- AMBA 4 ACE interface
- 1MB of L2 Cache
- 1MB with ECC protection

5.1.5 Arm Cortex-M4 Platform

The Cortex-M4 implements the ARMv7- ME instruction set architecture (ISA) and adds significant capabilities with DSP and SIMD extensions. The ARM Cortex-M4 core provides additional general processing capability to the SoC with lower power and fast interrupt response time. The Cortex-M4 also includes a single-precision floating-point unit (FPU) and two 32-bit system bus interfaces.
The Cortex-M4 implementation includes two tightly coupled local memories, two cache memories connected to bus interfaces, 64-bit system bus interconnect, and supports a 32-byte cache line size.

ARM Cortex M4 CPU processor includes the following features:

- AHB LMEM (Local Memory Controller) including controllers for TCM and cache memories
- 256 KB TCM (128 KB TCMU, 128 KB TCML)
- 16 KB Code Bus Cache
- 16 KB System Bus Cache
- ECC for TCM memories and parity for code and system caches
- Integrated Nested Vector Interrupt Controller (NVIC)
- Wakeup Interrupt Controller (WIC)
- FPU (Floating Point Unit)
- Core MPU (Memory Protection Unit)
- Support for exclusive access on the system bus
- MMCAU (Crypto Acceleration Unit)
- MCM (Miscellaneous Control Module)16 KB L1 Instruction Cache

5.2 Memory

5.2.1 RAM

The VAR-SOM-MX8 is available with up to 8GB of LPDDR4 memory capable of running up to 3200MTS.

5.2.2 Non-volatile Storage Memory

The VAR-SOM-MX8 is available with a non-volatile storage memory with optional densities.
It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.
The VAR-SOM-MX8 can arrive with up to 128GB MLC eMMC

5.3 Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4 Wi-Fi + BT (LWB5™)

The VAR-SOM-MX8 contains LSR's pre-certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 5.2 wireless connectivity.

The VAR-SOM-MX8 module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

Key Features:

- IEEE 802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, and BLE 5.2
- U.F.L connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- Industrial operating Temperature Range: -40 to +85
- Tristate buffer on the BT link based on UART interface will allow isolation from the LWB5 module and the use by external circuity via the SPEAR-MX8 connector. The tristate buffer controlled by QSPI1A_DATA0 line (alternate function GPIO4_IO26)

5.5 PMIC

The VAR-SOM-MX8 features Dual Freescale/NXP's PF8200 chips as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX 8QuadMax/QuadPlus series of application processors. The PF8200 regulates power rails required on SOM from a single 3.3V power supply.
The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

5.6 Dual Ethernet MAC and on-board 10/100/1000 Mbps Ethernet Transceiver

The SOM can be ordered with an Integrated Ethernet Transceiver connected to ENET0 RGMII signals, Qualcomm Atheros AR8033 or Analog Devices ADIN1300.
Please contact sales@variscite.com for inquiries about P/N assembled on your SOM.

An additional Ethernet Transceiver can be connected to ENET1 signals exported from SOM connector pins. Connecting an external Ethernet Transceiver requires a single 1.8/2.5V power supply for RGMII interfaces or 3.3V for RMII interface.

5.6.1 Qualcomm Atheros AR8033 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- 1000BASE-T PCS and auto-negotiation with next page support
- Green ETHOS power saving modes with internal automatic DSP power saving scheme
- IEEE 802.3az EEE
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Robust operation over up to 140 meters of CAT5 cable
- Automatic Channel Swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction ν IEEE 802.3u compliant auto-negotiation
- Jumbo frame supports up to 10 KB (full-duplex)
- Integrated termination circuitry at the line side

5.6.2 Analog Devices ADIN1300 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.
- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover

- Autonegotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

5.7 Resistive Touch Controller (TSC2046)

The VAR-SOM-MX8 features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

The SOM uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters.
This EEPROM is connected to I2C1 bus and intended only for holding the above information.
The SOM may not boot if the contents of EEPROM device are corrupted.

5.8 EEPROM

The SOM uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters.
This EEPROM is connected to SCU I2C bus and intended only for holding the above information.
The SOM may not boot if the contents of EEPROM device are corrupted.

6. VAR-SOM-MX8 Hardware Configuration

The table below lists the Hardware configurations options orderable for the VAR-SOM-MX8.

Table 1 Hardware Configuration Options

Option	Description
EC	Ethernet PHY assembled on SOM
AC	Audio Codec assembled on SOM
WBD	Dual band Wi-Fi and BT/BLE combo assembled on SOM
TP	Resistive Touch controller assembled on SOM
LD/ DSI/ DP	LD (default) - LVDS0 CH1 Upper 2x data lanes exported via SOM connector pins DSI - DSI Upper 2x data lanes exported via SOM connector pins HDMI/DP/eDP 1x Auxiliary lane exported via SOM connector pins
1588	IEEE 1588 time synchronization signals exported via SOM connector pins
TM	Tamper signals exported via SOM connector pins
CMP	Pins 31,33,35 are disconnected from VBAT on SOM

Note: Other orderable options are available and are not part of this datasheet.
Please refer to Variscite official website for full list of configuration options.

7. External Connectors

7.1 Board to Board Connector

The VAR-SOM-MX8 exposes a 200-pin SO-DIMM connector.

- The recommended mating connectors for baseboard interfacing are:
  1. Concraft - 0701A0BE52E
  2. Tyco Electronics -1565917-4

7.2 Wi-Fi & BT Connector

In Modules with Wi-Fi "WBD" Configuration - a combined Wi-Fi + BT antenna connector is assembled.

- Connector type: U.FL JACK connector
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 JTAG Header

In addition to the 200-pin SO-DIMM interface, the SOM exposes JTAG interface via an optional 10-pin header.

7.4 VAR-SOM-MX8 Connector Pin-out

Table 2: VAR-SOM-MX8 J1 Pinout

Pin#	Assembly	Pin Name	Notes	GPIO	Ball
1	No 1588	GND			
1	1588	ENET1_REFCLK_125M_25M		GPIO4_IO16	A11
2		GND			
3	EC	ETH0_MDI_A_P			AR8033.11/ ADIN1300.12
4	EC	ETH0_MDI_C_P			AR8033.17/ ADIN1300.16
5	EC	ETH0_MDI_A_M			AR8033.12/ ADIN1300.13
6	EC	ETH0_MDI_C_M			AR8033.18/ ADIN1300.17
7		GND			
8		GND			
9	EC	ETH0_MDI_B_P			AR8033.14/ ADIN1300.14
10	EC	ETH0_MDI_D_P			AR8033.20/ ADIN1300.18
11	EC	ETH0_MDI_B_M			AR8033.15/ ADIN1300.15
12	EC	ETH0_MDI_D_M			AR8033.21/ ADIN1300.19

Pin#	Assembly	Pin Name	Notes	GPIO	Ball
13		GND			
14		GND			
15	EC	ETH_LED_ACT	Ethernet PHY Activity LED, active low		AR8033.23/ ADIN1300.21
16	EC	ETH0_LED_LINK_10_100_1000	Ethernet PHY Link LED, active low		AR8033.24_26/ ADIN1300.26 via inverting FET
17		LVDS0_GPIO00		GPIO1_IO04	BE39
18	AC	DMIC_CLK	Digital microphone clock output		WM8904.1
19		GND			
20	AC	DMIC_DATA	Digital microphone data input		WM8904.27
21		SAI1_RXD		GPIO3_IO13	AV4
22		SAI1_RXC		GPIO3_IO12	AV6
23		SAI1_RXFS		GPIO3_IO14	AU3
24		SAI1_TXFS		GPIO3_IO17	AV2
25		SAI1_TXC		GPIO3_IO15	AU5
26		SAI1_TXD		GPIO3_IO16	AU1
27		GND			
28		GND			
29		MIPI_CSI0_MCLK_OUT	Pin is referenced to 1.8V. When using pin as an input pin driven by higher input voltage, use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.	GPIO1_IO24	BJ23
30		ENET0_MDIO	Pin alternate function cannot be changed when using SOM with EC assembled	GPIO4_IO13	D10
31	No CMP	VBAT			
31	CMP	NC			
32		VBAT			
33	No CMP	VBAT			
33	CMP	NC			
34		VBAT			
35	No CMP	VBAT			
35	CMP	NC			
36	No TM	VBAT			
36	TM	LICELL	RTC back-up battery 1.8V/3.0V/3.3V supply voltage input		PF8100.46
37		GND			

Pin#	Assembly	Pin Name	Notes	GPIO	Ball
38		VDD_ENET1_1P8_2P5_3P3_IN	VAR-SOM-MX8 1.8V/2.5V/3.3V supply voltage input. The following SOM pins are referenced to this voltage: 54,55,56,57,71,73,81,96,113,120,122,177 When using the above pins for alternate functions of ENET1: • For RMII - connect to 3.3V • For RGMII - connect to 1.8V/2.5V		
39		ADC_IN6	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_7: Low - Output from SoC High - Input to SoC	GPIO3_IO24	AL9
40		SPI0_CS1		GPIO3_IO06	BA3
41		ADC_IN5	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_6: Low - Output from SoC High - Input to SoC	GPIO3_IO23	AR7
42		LVDS0_GPIO01	Pin Used for Boot mode setting, Please see Boot Configuration section.	GPIO1_IO05	BD40
43		ADC_IN3	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_4: Low - Output from SoC High - Input to SoC	GPIO3_IO21	AR9
44		FLEXCAN0_TX		GPIO3_IO30	H6
45		ADC_IN4	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_5: Low - Output from SoC High - Input to SoC	GPIO3_IO22	AN9
46		FLEXCAN0_RX		GPIO3_IO29	C5
47		GND			
48		GPT1_CLK		GPIO0_IO17	BA53
49		SW_3P3	SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Connect to pin 38 in case of 3.3V supply.		
50		UART1_CTS_B	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	GPIO0_IO27	AV46
51		UART1_RTS_B	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	GPIO0_IO26	AR43
52		UART1_TX	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	GPIO0_IO24	AY48

Pin#	Assembly	Pin Name	Notes	GPIO	Ball
53		UART1_RX	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	GPIO0_IO25	AT44
54		ENET1_RGMII_RXD3	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO21	E53
55		ENET1_RGMII_TXD3	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO15	D48
56		ENET1_RGMII_TXD2	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO14	G47
57		ENET1_RGMII_RXC	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO16	B50
58	No 1588	GND			
58	1588	ENET0_REFCLK_125M_25M		GPIO4_IO15	B10
59		GND			
60		USDHC1_CLK			J39
61		USDHC1_DATA2		GPIO5_IO17	E39
62		USDHC1_DATA0		GPIO5_IO15	E37
63		USDHC1_DATA1		GPIO5_IO16	F38
64		USDHC1_CMD		GPIO5_IO14	G41
65		USDHC1_DATA3		GPIO5_IO18	F40
66	No TM	GND			
66	TM	SNVS_TAMPER_OUT0			BD46
67		GND			
68		GPT1_COMPARE		GPIO0_IO19	BA51
69		GPT0_COMPARE		GPIO0_IO16	AW53
70		SPI0_SDO		GPIO3_IO03	AY6
71		ENET1_RGMII_RXD2	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO20	D52
72		SPI2_CS1		GPIO3_IO11	AY2
73		ENET1_RGMII_TXD0	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO12	A49
74		ENET0_MDC	Pin alternate function cannot be changed when using SOM with EC assembled	GPIO4_IO14	A9
75		SPI0_SCK		GPIO3_IO02	BB4
76		GND			
77		SPI0_SDI		GPIO3_IO04	BA5
78		GND			
79		SPI0_CS0		GPIO3_IO05	BC1
80		GPT0_CLK		GPIO0_IO14	AY52
81		ENET1_RGMII_RXD1	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO19	C51
82		GPT1_CAPTURE		GPIO0_IO18	AY50
83		UART0_RX		GPIO0_IO20	AV50
84		UART0_CTS_B		GPIO0_IO23	AW49
85		UART0_TX		GPIO0_IO21	AV48
86		UART0_RTS_B		GPIO0_IO22	AU45
87		USB_SS3_TC3		GPIO4_IO06	H10
88		USB_SS3_TC1		GPIO4_IO04	L9
89		GND			
90		ENET1_MDIO		GPIO4_IO17	C13
91		USB_SS3_RX_N			B34

Pin#	Assembly	Pin Name	Notes	GPIO	Ball
92		ENET1_MDC		GPIO4_IO18	A13
93		USB_SS3_RX_P			C35
94		USB_OTG2_ID			F30
95		GND			
96		ENET1_RGMII_TXC	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO10	D46
97		USB_SS3_TX_P			A33
98		POR_B_3V3	System Reset Input. Active on falling edge. A logic low '0' on this pin will reset the system.		
99		USB_SS3_TX_N			B32
100		PCIE_SATA_REFCLK100M_N	PCIe compliant 100MHz reference clock. Can be exported from SOM or input to the SOM. The internal PCIe reference clock is not spread spectrum capable. For PCIe Gen 3.0 or EMC/EMI sensitive applications, it is recommended to connect to an external HCSL-compatible clock source.		E25
101		GND			
102		PCIE_SATA_REFCLK100M_P	PCIe compliant 100MHz reference clock. Can be exported from SOM or input to the SOM. The internal PCIe reference clock is not spread spectrum capable. For PCIe Gen 3.0 or EMC/EMI sensitive applications, it is recommended to connect to an external HCSL-compatible clock source.		F26
103		VBAT			
104		USB_OTG1_VBUS	USB Host VBUS (5V) input		A39
105		VBAT			
106		USB_OTG2_VBUS	USB OTG VBUS (5V) input		A35
107		VBAT			
108		USB_OTG1_DN			C39
109		VBAT			
110		USB_OTG1_DP			B40
111		VBAT			
112		GND			
113		ENET1_RGMII_TX_CTL	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO11	B48
114		USB_OTG2_DN			C37
115		M40_GPIO0_00		GPIO0_IO08	AR47
116		USB_OTG2_DP			B38
117		FLEXCAN1_TX		GPIO4_IO00	G7
118		GND			
119		MIPI_CSI0_DATA0_P			BF22
120		ENET1_RGMII_RX_CTL	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO17	E49
121		MIPI_CSI0_DATA0_N			BE23
122		ENET1_RGMII_RXD0	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO18	E51

Pin#	Assembly	Pin Name	Notes	GPIO	Ball
123		MIPI_CSI0_DATA1_N			BE19
124		LVDS0_I2C1_SCL		GPIO1_IO08	BE37
125		MIPI_CSI0_DATA1_P			BF18
126		GND			
127		MIPI_CSI0_DATA2_P			BF24
128		PCIE0_TX0_N			C27
129		MIPI_CSI0_DATA2_N			BE25
130		PCIE0_TX0_P			B26
131		MIPI_CSI0_DATA3_N			BE17
132		GND			
133		MIPI_CSI0_DATA3_P			BF16
134		PCIE0_RX0_P			A29
135		MIPI_CSI0_CLK_P			BF20
136		PCIE0_RX0_N			B30
137		MIPI_CSI0_CLK_N			BE21
138		GND			
139		GND			
140		MIPI_DSI0_CLK_P			BL27
141		MIPI_DSI0_DATA0_N			BM28
142		MIPI_DSI0_CLK_N			BN27
143		MIPI_DSI0_DATA0_P			BK28
144		GND			
145		MIPI_DSI0_DATA1_N			BM26
146		HDMI_TX0_DATA1_EDP1_P			BL7
147		MIPI_DSI0_DATA1_P			BK26
148		HDMI_TX0_DATA1_EDP1_N			BM6
149		GND			
150		HDMI_TX0_CLK_EDP3_N			BK2
151		HDMI_TX0_DATA2_EDP0_P			BL9
152		HDMI_TX0_CLK_EDP3_P			BL3
153		HDMI_TX0_DATA2_EDP0_N			BM8
154		HDMI_TX0_HPD			BH8
155		HDMI_TX0_DATA0_EDP2_P			BL5
156	No TM	HDMI_TX0_CEC			BJ1
156	TM	SNVS_TAMPER_IN0			BE41
157		HDMI_TX0_DATA0_EDP2_N			BM4
158		GND			
159		GND			
160		LVDS0_CH0_TX1_N			BL43
161		LVDS0_CH0_TX0_N			BK42
162		LVDS0_CH0_TX1_P			BN43
163		LVDS0_CH0_TX0_P			BM42
164		LVDS0_CH0_TX2_N			BK44

Pin#	Assembly	Pin Name	Notes	GPIO	Ball
165		LVDS0_CH0_TX3_N			BL45
166		LVDS0_CH0_TX2_P			BM44
167		LVDS0_CH0_TX3_P			BN45
168		LVDS0_CH0_CLK_N			BL41
169		GND			
170		LVDS0_CH0_CLK_P			BN41
171		M40_GPIO0_01		GPIO0_IO09	AU53
172		GND			
173		FLEXCAN1_RX		GPIO3_IO31	E5
174		HDMI_TX0_TS_SCL	SoC ball is exported via on SOM switch controlled by GPIO1_22: Low (default) - SoC Ball BN9 ball is exported High - SoC Ball BG1 is exported	GPIO2_IO02	BN9
174		HDMI_TX0_DDC_SCL	SoC ball is exported via on SOM switch controlled by GPIO1_22: Low (default) - SoC Ball BN9 ball is exported High - SoC Ball BG1 is exported		BG1
175		LVDS0_I2C1_SDA		GPIO1_IO09	BE35
176		HDMI_TX0_TS_SDA	SoC ball is exported via on SOM switch controlled by GPIO1_22: Low (default) - SoC Ball BN7 ball is exported High - SoC Ball BN5 is exported	GPIO2_IO03	BN7
176		HDMI_TX0_DDC_SDA	SoC ball is exported via on SOM switch controlled by GPIO1_22: Low (default) - SoC Ball BN7 ball is exported High - SoC Ball BN5 is exported		BN5
177		ENET1_RGMII_TXD1	Referenced to pin 38 supply (1.8V/2.5/3.3V)	GPIO6_IO13	C47
178		GND			
179		GND			
180		LVDS0_CH1_CLK_N			BG45
181	LD	LVDS0_CH1_TX3_P			BH38
181	DSI	MIPI_DSI0_DATA3_P			BL25
181	DP	HDMI_TX0_AUX_P			BH2
182		LVDS0_CH1_CLK_P			BH46
183	LD	LVDS0_CH1_TX3_N			BG37
183	DSI	MIPI_DSI0_DATA3_N			BN25
183	DP	HDMI_TX0_AUX_N			BG3
184		LVDS0_CH1_TX0_N			BG43
185		GND			
186		LVDS0_CH1_TX0_P			BH44
187	TP	TS_X-			TSC2046.8
188		LVDS0_CH1_TX1_N			BG41
189	TP	TS_X+			TSC2046.6
190		LVDS0_CH1_TX1_P			BH42
191	TP	TS_Y+			TSC2046.7
192	LD	LVDS0_CH1_TX2_N			BG39
192	DSI	MIPI_DSI0_DATA2_N			BN29

Pin#	Assembly	Pin Name	Notes	GPIO	Ball
193	TP	TS_Y-			TSC2046.9
194	LD	LVDS0_CH1_TX2_P			BH40
194	DSI	MIPI_DSI0_DATA2_P			BL29
195		AGND	Audio interface ground reference		
196	AC	HPOUTFB	Headphone output ground loop noise rejection feedback		WM8904.14
197	AC	LINEIN1_LP	Left channel input		WM8904.26
198	AC	HPLOUT	Left headphone output (line or headphone output)		WM8904.13
199	AC	LINEIN1_RP	Right channel input		WM8904.24
200	AC	HPROUT	Right headphone output (line or headphone output)		WM8904.15

7.5 VAR-SOM-MX8 Connector Pin Mux

Table 3: VAR-SOM-MX8 PINMUX

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3
1	1588	A11	CONN.ENET1.REFCLK_125M_25M	CONN.ENET1.PPS		LSIO.GPIO4.IO16
17		BE39	LVDS0.GPIO0.IO00	LVDS0.PWM0.OUT		LSIO.GPIO1.IO04
21		AV4	AUD.SAI1.RXD	AUD.SAI0.TXFS		LSIO.GPIO3.IO13
22		AV6	AUD.SAI1.RXC	AUD.SAI0.TXD		LSIO.GPIO3.IO12
23		AU3	AUD.SAI1.RXFS	AUD.SAI0.RXD		LSIO.GPIO3.IO14
24		AV2	AUD.SAI1.TXFS	AUD.SAI1.RXFS		LSIO.GPIO3.IO17
25		AU5	AUD.SAI1.TXC	AUD.SAI0.TXC		LSIO.GPIO3.IO15
26		AU1	AUD.SAI1.TXD	AUD.SAI1.RXC		LSIO.GPIO3.IO16
29		BJ23	MIPI_CSI0.ACM.MCLK_OUT			LSIO.GPIO1.IO24
30		D10	CONN.ENET0.MDIO	DMA.I2C4.SDA		LSIO.GPIO4.IO13
39		AL9		DMA.SPI1.CS0	LSIO.KPP0.ROW2	LSIO.GPIO3.IO24
40		BA3	DMA.SPI0.CS1	AUD.SAI0.TXC		LSIO.GPIO3.IO06
41		AR7		DMA.SPI1.SDI	LSIO.KPP0.ROW1	LSIO.GPIO3.IO23
42		BD40	LVDS0.GPIO0.IO01			LSIO.GPIO1.IO05
43		AR9		DMA.SPI1.SCK	LSIO.KPP0.COL3	LSIO.GPIO3.IO21
44		H6	DMA.FLEXCAN0.TX			LSIO.GPIO3.IO30
45		AN9		DMA.SPI1.SDO	LSIO.KPP0.ROW0	LSIO.GPIO3.IO22
46		C5	DMA.FLEXCAN0.RX			LSIO.GPIO3.IO29
48		BA53	LSIO.GPT1.CLK	DMA.I2C2.SCL	LSIO.KPP0.COL7	LSIO.GPIO0.IO17
50		AV46	DMA.UART1.CTS_B	DMA.SPI3.CS0	DMA.UART1.RTS_B	LSIO.GPIO0.IO27
51		AR43	DMA.UART1.RTS_B	DMA.SPI3.SDI	DMA.UART1.CTS_B	LSIO.GPIO0.IO26
52		AY48	DMA.UART1.TX	DMA.SPI3.SCK		LSIO.GPIO0.IO24
53		AT44	DMA.UART1.RX	DMA.SPI3.SDO		LSIO.GPIO0.IO25
54		E53	CONN.ENET1.RGMII_RXD3	DMA.UART3.RX	VPU.TSI_S1.CLK	LSIO.GPIO6.IO21
55		D48	CONN.ENET1.RGMII_TXD3	DMA.UART3.RTS_B	VPU.TSI_S1.SYNC	LSIO.GPIO6.IO15
56		G47	CONN.ENET1.RGMII_TXD2	DMA.UART3.TX	VPU.TSI_S1.VID	LSIO.GPIO6.IO14

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3
57		B50	CONN.ENET1.RGMII_RXC	DMA.UART3.CTS_B	VPU.TSI_S1.DATA	LSIO.GPIO6.IO16
58	1588	B10	CONN.ENET0.REFCLK_125M_25M	CONN.ENET0.PPS		LSIO.GPIO4.IO15
60		J39	CONN.USDHC1.CLK			
61		E39	CONN.USDHC1.DATA2	CONN.NAND.DQS_N		LSIO.GPIO5.IO17
62		E37	CONN.USDHC1.DATA0	CONN.NAND.RE_N		LSIO.GPIO5.IO15
63		F38	CONN.USDHC1.DATA1	CONN.NAND.RE_P		LSIO.GPIO5.IO16
64		G41	CONN.USDHC1.CMD			LSIO.GPIO5.IO14
65		F40	CONN.USDHC1.DATA3	CONN.NAND.DQS_P		LSIO.GPIO5.IO18
66	TM	BD46	SNVS.TAMPER_OUT0			
68		BA51	LSIO.GPT1.COMPARE	LSIO.PWM2.OUT	LSIO.KPP0.ROW5	LSIO.GPIO0.IO19
69		AW53	LSIO.GPT0.COMPARE	LSIO.PWM3.OUT	LSIO.KPP0.COL6	LSIO.GPIO0.IO16
70		AY6	DMA.SPI0.SDO	AUD.SAI0.TXD		LSIO.GPIO3.IO03
71		D52	CONN.ENET1.RGMII_RXD2	CONN.ENET1.RMII_RX_ER	VPU.TSI_S0.CLK	LSIO.GPIO6.IO20
72		AY2	DMA.SPI2.CS1	AUD.SAI0.TXFS		LSIO.GPIO3.IO11
73		A49	CONN.ENET1.RGMII_TXD0			LSIO.GPIO6.IO12
74		A9	CONN.ENET0.MDC	DMA.I2C4.SCL		LSIO.GPIO4.IO14
75		BB4	DMA.SPI0.SCK	AUD.SAI0.RXC		LSIO.GPIO3.IO02
77		BA5	DMA.SPI0.SDI	AUD.SAI0.RXD		LSIO.GPIO3.IO04
79		BC1	DMA.SPI0.CS0	AUD.SAI0.RXFS		LSIO.GPIO3.IO05
80		AY52	LSIO.GPT0.CLK	DMA.I2C1.SCL	LSIO.KPP0.COL4	LSIO.GPIO0.IO14
81		C51	CONN.ENET1.RGMII_RXD1		VPU.TSI_S0.DATA	LSIO.GPIO6.IO19
82		AY50	LSIO.GPT1.CAPTURE	DMA.I2C2.SDA	LSIO.KPP0.ROW4	LSIO.GPIO0.IO18
83		AV50	DMA.UART0.RX			LSIO.GPIO0.IO20
84		AW49	DMA.UART0.CTS_B	LSIO.PWM1.OUT	DMA.UART2.TX	LSIO.GPIO0.IO23
85		AV48	DMA.UART0.TX			LSIO.GPIO0.IO21
86		AU45	DMA.UART0.RTS_B	LSIO.PWM0.OUT	DMA.UART2.RX	LSIO.GPIO0.IO22
87		H10	DMA.I2C1.SDA	CONN.USB_OTG2.OC		LSIO.GPIO4.IO06
88		L9	DMA.I2C1.SCL	CONN.USB_OTG2.PWR		LSIO.GPIO4.IO04
90		C13	CONN.ENET1.MDIO	DMA.I2C4.SDA		LSIO.GPIO4.IO17
91		B34	CONN.USB_SS3.RX_M_LN_0			
92		A13	CONN.ENET1.MDC	DMA.I2C4.SCL		LSIO.GPIO4.IO18
93		C35	CONN.USB_SS3.RX_P_LN_0			
94		F30	CONN.USB_OTG2.ID			
96		D46	CONN.ENET1.RGMII_TXC	CONN.ENET1.RCLK50M_OUT	CONN.ENET1.RCLK50M_IN	LSIO.GPIO6.IO10

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3
97		A33	CONN.USB_SS3.TX_P_LN_0			
99		B32	CONN.USB_SS3.TX_M_LN_0			
100		E25	HSIO.PCIE_IOB.EXT_REFCLK100M_N			
102		F26	HSIO.PCIE_IOB.EXT_REFCLK100M_P			
104		A39	CONN.USB_OTG1.VBUS			
106		A35	CONN.USB_OTG2.VBUS			
108		C39	CONN.USB_OTG1.DN			
110		B40	CONN.USB_OTG1.DP			
113		B48	CONN.ENET1.RGMII_TX_CTL			LSIO.GPIO6.IO11
114		C37	CONN.USB_OTG2.DM			
115		AR47	M40.GPIO0.IO00	M40.TPM0.CH0	DMA.UART4.RX	LSIO.GPIO0.IO08
116		B38	CONN.USB_OTG2.DP			
117		G7	DMA.FLEXCAN1.TX			LSIO.GPIO4.IO00
119		BF22	MIPI_CSI0.DP0			
120		E49	CONN.ENET1.RGMII_RX_CTL		VPU.TSI_S0.VID	LSIO.GPIO6.IO17
121		BE23	MIPI_CSI0.DN0			
122		E51	CONN.ENET1.RGMII_RXD0		VPU.TSI_S0.SYNC	LSIO.GPIO6.IO18
123		BE19	MIPI_CSI0.DN1			
124		BE37	LVDS0.I2C1.SCL	DMA.UART2.TX		LSIO.GPIO1.IO08
125		BF18	MIPI_CSI0.DP1			
127		BF24	MIPI_CSI0.DP2			
128		C27	HSIO.PCIE0.TX0_N			
129		BE25	MIPI_CSI0.DN2			
130		B26	HSIO.PCIE0.TX0_P			
131		BE17	MIPI_CSI0.DN3			
133		BF16	MIPI_CSI0.DP3			
134		A29	HSIO.PCIE0.RX0_P			
135		BF20	MIPI_CSI0.CKP			
136		B30	HSIO.PCIE0.RX0_N			
137		BE21	MIPI_CSI0.CKN			
140		BL27	MIPI_DSI0.CKP			
141		BM28	MIPI_DSI0.DN0			
142		BN27	MIPI_DSI0.CKN			
143		BK28	MIPI_DSI0.DP0			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3
145		BM26	MIPI_DSI0.DN1			
146		BL7	HDMI_TX0.TX_P_LN_1			
147		BK26	MIPI_DSI0.DP1			
148		BM6	HDMI_TX0.TX_M_LN_1			
150		BK2	HDMI_TX0.TX_M_LN_3			
151		BL9	HDMI_TX0.TX_P_LN_0			
152		BL3	HDMI_TX0.TX_P_LN_3			
153		BM8	HDMI_TX0.TX_M_LN_0			
154		BH8	HDMI_TX0.HPD			
155		BL5	HDMI_TX0.TX_P_LN_2			
156	No TM	BJ1	HDMI_TX0.CEC			
156	TM	BE41	SNVS.TAMPER_IN0			
157		BM4	HDMI_TX0.TX_M_LN_2			
160		BL43	LVDS0.T0BN			
161		BK42	LVDS0.T0AN			
162		BN43	LVDS0.T0BP			
163		BM42	LVDS0.T0AP			
164		BK44	LVDS0.T0CN			
165		BL45	LVDS0.T0DN			
166		BM44	LVDS0.T0CP			
167		BN45	LVDS0.T0DP			
168		BL41	LVDS0.T0CLKN			
170		BN41	LVDS0.T0CLKP			
171		AU53	M40.GPIO0.IO01	M40.TPM0.CH1	DMA.UART4.TX	LSIO.GPIO0.IO09
173		E5	DMA.FLEXCAN1.RX			LSIO.GPIO3.IO31
174		BN9	HDMI_TX0.I2C0.SCL	DMA.I2C0.SCL		LSIO.GPIO2.IO02
174		BG1	HDMI_TX0.DDC_SCL			
175		BE35	LVDS0.I2C1.SDA	DMA.UART2.RX		LSIO.GPIO1.IO09
176		BN7	HDMI_TX0.I2C0.SDA	DMA.I2C0.SDA		LSIO.GPIO2.IO03
176		BN5	HDMI_TX0.DDC_SDA			
177		C47	CONN.ENET1.RGMII_TXD1			LSIO.GPIO6.IO13
180		BG45	LVDS0.T1CLKN			
181	LD	BH38	LVDS0.T1DP			
181	DSI	BL25	MIPI_DSI0.DP3			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3
181	DP	BH2	HDMI_TX0.AUX_P			
182		BH46	LVDS0.T1CLKP			
183	LD	BG37	LVDS0.T1DN			
183	DSI	BN25	MIPI_DSI0.DN3			
183	DP	BG3	HDMI_TX0.AUX_M			
184		BG43	LVDS0.T1AN			
186		BH44	LVDS0.T1AP			
188		BG41	LVDS0.T1BN			
190		BH42	LVDS0.T1BP			
192	LD	BG39	LVDS0.T1CN			
192	DSI	BN29	MIPI_DSI0.DN2			
194	LD	BH40	LVDS0.T1CP			
194	DSI	BL29	MIPI_DSI0.DP2			

8. SOM's Interfaces

Trace Impedance
SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 4: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
PCIe TX/RX data pairs	85 Ω Differential
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, PCIe clocks, MIPI (CSI and DSI), LVDS, HDMI lines	100 Ω Differential

8.1 Display Interfaces

The VAR-SOM-MX8 supports HDMI/DP/eDP, MIPI DSI and LVDS display interfaces.

8.1.1 HDMI/DP/eDP

The i.MX 8QuadMax/QuadPlus HD Display Transmitter Controller IP offers multi-protocol support of standards such as HDMI, DisplayPort, eDP.

The following features are supported:

- HDMI/DP/eDP
  - HDMI 1.4, HDMI 2.0a support for resolution up to 4096x2160p60
  - HDCP 2.2 and HDCP 1.4
  - Pixel clock up to 600 MHz
  - DisplayPort 1.3(VESA.org):
    - DP supports 1.6 GHz (RBR), 2.7 GHz (HBR), and 5.4 GHz (HBR2) rates. Those rates are managed in API (Host).
    - RBR supports 1080p60 (RGB 8b), HBR supports 4kp30 (RGB 8b) and HBR2 supports 4kp60 (RGB 8b).
  - eDP 1.4 (VESA.org):
    - eDP link rates: R216 (2.16 Gbps), R243 (2.43 Gbps), R324 (3.24 Gbps), and R432 (4.32 Gbps)
    - Fast Link Training is also supported

Note: The HDMI, Display port and Embedded Display port signals share the same pins. Only one standard is supported at a time depending on SW configuration. In addition, eDP/DP requires the “DP” assembly option.

Table 5: HDMI/DP/eDP Signals

Pin#	Assy	Pin Function	Notes	Ball
183	DP	HDMI_TX0_AUX_M	HDMI/DP/eDP- AUX_N	BG3
181	DP	HDMI_TX0_AUX_P	HDMI/DP/eDP: AUX_P	BH2
156	No TM	HDMI_TX0_CEC	HDMI: HDMI_TX0_CEC	BJ1
154		HDMI_TX0_HPD	HDMI/DP/eDP: Hot Plug Detect	BH8
153		HDMI_TX0_TX_M_LN_0	HDMI: HDMI_TX0_DATA2_N DP/eDP: EDP0_N	BM8
148		HDMI_TX0_TX_M_LN_1	HDMI: HDMI_TX0_DATA1_N DP/eDP: EDP1_N	BM6
157		HDMI_TX0_TX_M_LN_2	HDMI: HDMI_TX0_DATA0_N DP/eDP: EDP2_N	BM4
150		HDMI_TX0_TX_M_LN_3	HDMI: HDMI_TX0_CLK_N DP/eDP: EDP3_N	BK2
151		HDMI_TX0_TX_P_LN_0	HDMI: HDMI_TX0_DATA2_P DP/eDP: EDP0_P	BL9
146		HDMI_TX0_TX_P_LN_1	HDMI: HDMI_TX0_DATA1_P DP/eDP: EDP1_P	BL7
155		HDMI_TX0_TX_P_LN_2	HDMI: HDMI_TX0_DATA0_P DP/eDP: EDP2_P	BL5
152		HDMI_TX0_TX_P_LN_3	HDMI: HDMI_TX0_CLK_P DP/eDP: EDP3_P	BL3

8.1.2 DSI

The i.MX 8QuadMax/QuadPlus incorporates the MIPI DSI Host Controller.
The VAR-SOM-MX8 exposes by default, a 2 data lane + clock interface.
Additional 2 data lanes are exposed only on SOM with “DSI” assembly option.

The following are the key features of the MIPI DSI D-PHY:

- 1 Clock lane
- 4 data lanes
- Supports MIPI Standard for D-PHY
- Supports both high speed and low power modes
- High Speed Serializers and Deserializers

Table 6: MIPI DSI Signals

Pin#	Assy	Pin Function	Notes	Ball
141		MIPI_DSI0_DN0		BM28
143		MIPI_DSI0_DP0		BK28
145		MIPI_DSI0_DN1		BM26
147		MIPI_DSI0_DP1		BK26
192	DSI	MIPI_DSI0_DN2		BN29
194	DSI	MIPI_DSI0_DP2		BL29
183	DSI	MIPI_DSI0_DN3		BN25
181	DSI	MIPI_DSI0_DP3		BL25
142		MIPI_DSI0_CKN		BN27
140		MIPI_DSI0_CKP		BL27

8.1.3 LVDS

The SOM exports a Dual channel LVDS interface.
The interface is used to communicate RGB data and controls to external LCD displays.
By default, LVDS0 CH1 upper 2x data lanes are exported via SOM connector pins.
For other assembly options refer to Table 1, Table 57 of datasheet.

Table 7: LVDS Signals

Pin#	Assy	Pin Function	Notes	Ball
17		LVDS0_GPIO0_IO00		BE39
42		LVDS0_GPIO0_IO01	Pin Used for Boot mode setting, Please see Boot Configuration section.	BD40
124		LVDS0_I2C1_SCL		BE37
175		LVDS0_I2C1_SDA		BE35
17		LVDS0_PWM0_OUT		BE39
161		LVDS0_CH0_TX0_N		BK42
163		LVDS0_CH0_TX0_P		BM42
160		LVDS0_CH0_TX1_N		BL43
162		LVDS0_CH0_TX1_P		BN43
164		LVDS0_CH0_TX2_N		BK44
166		LVDS0_CH0_TX2_P		BM44
165		LVDS0_CH0_TX3_N		BL45
167		LVDS0_CH0_TX3_P		BN45
168		LVDS0_CH0_CLK_N		BL41
170		LVDS0_CH0_CLK_P		BN41
184		LVDS0_CH1_TX0_N		BG43
186		LVDS0_CH1_TX0_P		BH44
188		LVDS0_CH1_TX1_N		BG41
190		LVDS0_CH1_TX1_P		BH42
192	LD	LVDS0_CH1_TX2_N		BG39
194	LD	LVDS0_CH1_TX2_P		BH40
183	LD	MIPI_DSI0_DATA3_N		BG37
181	LD	MIPI_DSI0_DATA3_P		BH38
180		LVDS0_CH1_CLK_N		BG45
182		LVDS0_CH1_CLK_P		BH46

8.2 Camera Interface

8.2.1 MIPI CSI-2

The SOM consist of a CSI-2 Host Controller which implements all protocol functions defined in the MIPI CSI-2 specification, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 controller supports the following features:

- Implements all three CSI-2 MIPI layers (Pixel to byte packing, low level protocol, Lane management)
- Supports unidirectional Master operation
- Transmitter and receiver versions
- Scalable data lane support, 1 to 4 Data Lanes
- Supports high speed mode(80Mbps - 1.5Gbps) per lane, providing 4K@30fps capability for the 4 lanes
- Supports 10Mbps data rate in low power mode
- Includes high speed deserializers
- Loopback testability support
- Support for all CSI-2 data types
- Virtual Channel support
- Support for DPHY Ultra Low Power State (ULPS)
- Error collection support (Rx Only)
- Flexible pixel-based user interface
    - Supports user generated packets
    - Supports single, double, or quad pixel interface
- Supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs
    - Delivered fully integrate and verified with target MIPI D-PHY
- RX Video Interface
- APB Control and Status Register (CSR) interface with IRQ support
- Easy configuration and control via core ports
- Optimized for use in FPGAs and ASICs
- Provided with full-featured MIPI Test bench
    - Provides scripting, stimulus and data logging capabilities
    - Can be used for basic verification of user's design
- Source code option
- Provided with expert technical support
- Customization and integration services available

Table 8: MIPI-CSI2 Signals

Pin#	Assy	Pin Function	Notes	Ball
121		MIPI_CSI0_DN0		BE23
119		MIPI_CSI0_DP0		BF22
123		MIPI_CSI0_DN1		BE19
125		MIPI_CSI0_DP1		BF18
129		MIPI_CSI0_DN2		BE25
127		MIPI_CSI0_DP2		BF24
131		MIPI_CSI0_DN3		BE17
133		MIPI_CSI0_DP3		BF16
137		MIPI_CSI0_CKN		BE21
135		MIPI_CSI0_CKP		BF20
29		MIPI_CSI0_ACM_MCLK_OUT	Pin is referenced to 1.8V. When using pin as an input pin driven by higher input voltage, use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.	BJ23

8.3 Ethernet Interface

The iMX 8QuadMax/QuadPlus core implements a triple-speed 10/100/1000-Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full duplex 10/100-Mbit/s and full-duplex gigabit Ethernet LANs.
The core consists of the IEEE1588 time-stamping module. The IEEE 1588 standard provides accurate clock synchronization for distributed control nodes for industrial automation applications. The MAC interface supports also AVB (Audio Video Bridging, IEEE 802.1Qav)

The VAR-SOM-MX8 features on SOM a Gigabit PHY (Atheros AR8033 or ADIN1300) connected to ENET0 RGMII interface signals. External connector and magnetics should be implemented on carrier board complete the interface to the media.

ENET1 RGMII/RMII interface signals are exported through SO-DIMM connector.
Signals, in conjunction to MDIO signals exported from SO-DIMM connector, can be used to interface an external Ethernet PHY.

ENET1 pins are referenced to SOM pin 38 VDD_ENET1_1P8_2P5_3P3_IN.
Reference voltage should be supplied to SOM pin 38.
For RMII - 3.3 V
For RGMII - 1.8V or 2.5V

The Following External Gigabit magnetics are required to complete the ETH0 interface to the media.

Table 9: Gigabit Ethernet Magnetics

Vendor	P/N	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

Table 10: Ethernet0 PHY Signals

Pin#	Assy	Pin Function	Notes	Ball
15	EC	ETH_LED_ACT	Ethernet PHY Activity LED, active low	AR8033.23/ ADIN1300.21
16	EC	ETH0_LED_LINK_10_100_1000	Ethernet PHY Link LED, active low	AR8033.24_26/ ADIN1300.26 via inv. FET
5	EC	ETH0_MDI_A_M		AR8033.12/ ADIN1300.13
3	EC	ETH0_MDI_A_P		AR8033.11/ ADIN1300.12
11	EC	ETH0_MDI_B_M		AR8033.15/ ADIN1300.15
9	EC	ETH0_MDI_B_P		AR8033.14/ ADIN1300.14
6	EC	ETH0_MDI_C_M		AR8033.18/ ADIN1300.17
4	EC	ETH0_MDI_C_P		AR8033.17/ ADIN1300.16
12	EC	ETH0_MDI_D_M		AR8033.21/ ADIN1300.19
10	EC	ETH0_MDI_D_P		AR8033.20/ ADIN1300.18

Table 11: ENET1 Supply voltage input Signal

Pin#	Assy	Pin Function	Notes	Ball
38		VDD_ENET1_1P8_2P5_3P3_IN	VAR-SOM-MX8 1.8V/2.5V/3.3V supply voltage input. The following SOM pins are referenced to this voltage: 54,55,56,57,71,73,81,96,113,120,122,177 When using the above pins for alternate functions of ENET1: • For RMII - connect to 3.3V • For RGMII - connect to 1.8V/2.5V	

Table 12: ENET1 RGMII Signals

Pin#	Assy	Pin Function	Notes	Ball
1	1588	CONN_ENET1_REFCLK_125M_25M		A11
120		CONN_ENET1_RGMII_RX_CTL	Referenced to pin 38 supply (1.8V/2.5/3.3V)	E49
57		CONN_ENET1_RGMII_RXC	Referenced to pin 38 supply (1.8V/2.5/3.3V)	B50
122		CONN_ENET1_RGMII_RXD0	Referenced to pin 38 supply (1.8V/2.5/3.3V)	E51
81		CONN_ENET1_RGMII_RXD1	Referenced to pin 38 supply (1.8V/2.5/3.3V)	C51
71		CONN_ENET1_RGMII_RXD2	Referenced to pin 38 supply (1.8V/2.5/3.3V)	D52
54		CONN_ENET1_RGMII_RXD3	Referenced to pin 38 supply (1.8V/2.5/3.3V)	E53
113		CONN_ENET1_RGMII_TX_CTL	Referenced to pin 38 supply (1.8V/2.5/3.3V)	B48
96		CONN_ENET1_RGMII_TXC	Referenced to pin 38 supply (1.8V/2.5/3.3V)	D46
73		CONN_ENET1_RGMII_TXD0	Referenced to pin 38 supply (1.8V/2.5/3.3V)	A49
177		CONN_ENET1_RGMII_TXD1	Referenced to pin 38 supply (1.8V/2.5/3.3V)	C47
56		CONN_ENET1_RGMII_TXD2	Referenced to pin 38 supply (1.8V/2.5/3.3V)	G47
55		CONN_ENET1_RGMII_TXD3	Referenced to pin 38 supply (1.8V/2.5/3.3V)	D48

Table 13: ENET1 RMII Signals

Pin#	Assy	Pin Function	Notes	Ball
96		CONN_ENET1_RCLK50M_IN	ENET1 RMII RCLK50M Input Clock (see note [1]). Referenced to pin 38 supply (1.8V/2.5/3.3V)	D46
96		CONN_ENET1_RCLK50M_OUT	ENET1 RMII RCLK50M Output Clock (see note [1]). Referenced to pin 38 supply (1.8V/2.5/3.3V)	D46
120		CONN_ENET1_RGMII_RX_CTL	ENET1 RMII_CRS_DV Referenced to pin 38 supply (1.8V/2.5/3.3V)	E49
122		CONN_ENET1_RGMII_RXD0	ENET1 RMII_RXD0 Referenced to pin 38 supply (1.8V/2.5/3.3V)	E51
81		CONN_ENET1_RGMII_RXD1	ENET1 RMII_RXD1 Referenced to pin 38 supply (1.8V/2.5/3.3V)	C51
71		CONN_ENET1_RMII_RX_ER	ENET1 RMII_RXER (see note [1]). Referenced to pin 38 supply (1.8V/2.5/3.3V)	D52
113		CONN_ENET1_RGMII_TX_CTL	ENET1 RMII_TXEN Referenced to pin 38 supply (1.8V/2.5/3.3V)	B48

Pin#	Assy	Pin Function	Notes	Ball
73		CONN_ENET1_RGMII_TXD0	ENET1 RMII_TXD0 Referenced to pin 38 supply (1.8V/2.5/3.3V)	A49
177		CONN_ENET1_RGMII_TXD1	ENET1 RMII_TXD1 Referenced to pin 38 supply (1.8V/2.5/3.3V)	C47

Note:

[1] Except for RCLK50M and RMII_RXER, all other RMII functions are using the same pin muxing mode of RGMII

Table 14: AR8033 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100_1000	OFF	OFF	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

Table 15: ADIN1300 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100_1000	ON	ON	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

Table 16: MDIO & 1588 Signals

Pin#	Assy	Pin Function	Notes	Ball
74		CONN_ENET0_MDC	Pin alternate function cannot be changed when using SOM with EC assembled	A9
30		CONN_ENET0_MDIO	Pin alternate function cannot be changed when using SOM with EC assembled	D10
58	1588	CONN_ENET0_PPS		B10
92		CONN_ENET1_MDC		A13
90		CONN_ENET1_MDIO		C13
1	1588	CONN_ENET1_PPS		A11

8.4 Ultra Secured Digital Host Controller uSDHC1

The SOM exposes uSDHC1 controller 4-bit interface for supporting interface between the host system and the SD/SDIO/MMC cards.
Key features of uSDHC1:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.0.
- 1.8 V and 3.3 V operation
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode
- Up to SDR104 rate

Another uSDHC controller, uSDHC0, capable of supporting up to an 8-bit interface is used internally for the eMMC interface on the SOM.

Table 17: uSDHC1 Signals

Pin#	Assy	Pin Function	Notes	Ball
60		CONN_USDHC1_CLK		J39
61		CONN_USDHC1_DATA2		E39
62		CONN_USDHC1_DATA0		E37
63		CONN_USDHC1_DATA1		F38
64		CONN_USDHC1_CMD		G41
65		CONN_USDHC1_DATA3		F40

8.5 USB 2.0

The SOM consists of a two USB controller blocks which provides 2 high-performance USB functionality USB ports that conform to the USB 2.0 specification.
Port 1 supports Host/Peripheral modes.
Port 2 supports OTG functionality as well as Host/Peripheral modes.

Table 18: USB 2.0 Port 1 Signals

Pin#	Assy	Pin Function	Notes	Ball
108		CONN_USB_OTG1_DN		C39
110		CONN_USB_OTG1_DP		B40
104		CONN_USB_OTG1_VBUS	USB Host VBUS (5V) input	A39

Table 19: USB 2.0 Port 2 Signals

Pin#	Assy	Pin Function	Notes	Ball
114		CONN_USB_OTG2_DM		C37
116		CONN_USB_OTG2_DP		B38
106		CONN_USB_OTG2_VBUS	USB OTG VBUS (5V) input	A35

8.5.1 USB OTG interface signals

The VAR-SOM-MX8 exposes pins, which can be optionally used to implement OTG functions.

Table 20: USB Port 2 OTG Interface signals

Pin#	Assy	Pin Function	Notes	Ball
94		CONN_USB_OTG2_ID		F30
87		CONN_USB_OTG2_OC		H10
88		CONN_USB_OTG2_PWR		L9

8.6 USB 3.0

The SOM includes a Super-speed USB 3.0 core consisting of:

- Super Speed (5 Gbps), High Speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps)
- Fully compatible with the USB 3.0 specification (backward compatible with USB 2.0)
- Fully compatible with the USB On-The-Go supplement to the USB 2.0 specification
- Hardware support for OTG signaling
- Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) implemented in hardware, which can also be controlled by software

Table 21: USB3 Signals

Pin#	Assy	Pin Function	Notes	Ball
91		CONN_USB_SS3_RX_M_LN_0		B34
93		CONN_USB_SS3_RX_P_LN_0		C35
97		CONN_USB_SS3_TX_P_LN_0		A33
99		CONN_USB_SS3_TX_M_LN_0		B32

8.7 Audio

The SOM features two audio interfaces

- WM8904CGEFL Audio codec interfaces:
  - Analog outputs & inputs: stereo line-in & Stereo HP out.
  - Digital microphone input
- Serial Audio Interface

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only. The codec interfaces the SoC via ESAI0 lines, when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

The following figure illustrates the connectivity for no large AC coupling capacitors implemented on SOM.

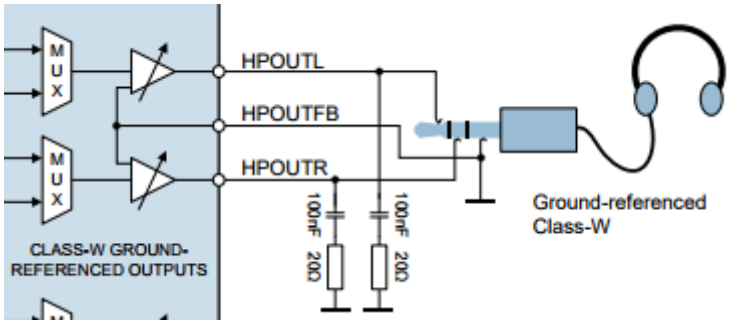


Figure 3: WM8904 Headphone connectivity

8.7.1 WM8904CGEFL Audio Codec

Table 22: Analog audio Signals

Pin #	Assy	Pin Function	Notes	Ball
195	AC	AGND	Audio interface ground reference	Audio AGND
18	AC	DMIC_CLK	Digital microphone clock output	WM8904CGEFL.1
20	AC	DMIC_DATA	Digital microphone data input	WM8904CGEFL.27
198	AC	HPLOUT	Left headphone output (line or headphone output)	WM8904CGEFL.13
196	AC	HPOUTFB	Headphone output ground loop noise rejection feedback	WM8904CGEFL.14
200	AC	HPROUT	Right headphone output (line or headphone output)	WM8904CGEFL.15
197	AC	LINEIN1_LP	Left channel input	WM8904CGEFL.26
199	AC	LINEIN1_RP	Right channel input	WM8904CGEFL.24

8.7.2 Serial Audio Interface

The SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Table 23: Serial Audio Interface 0 Signals

Pin#	Assy	Pin Function	Notes	Ball
75		AUD_SAI0_RXC		BB4
23		AUD_SAI0_RXD		AU3
77		AUD_SAI0_RXD		BA5
79		AUD_SAI0_RXFS		BC1
25		AUD_SAI0_TXC		AU5
40		AUD_SAI0_TXC		BA3
22		AUD_SAI0_TXD		AV6
70		AUD_SAI0_TXD		AY6
21		AUD_SAI0_TXFS		AV4
72		AUD_SAI0_TXFS		AY2

Table 24: Serial Audio Interface 1 Signals

Pin#	Assy	Pin Function	Notes	Ball
22		AUD_SAI1_RXC		AV6
26		AUD_SAI1_RXC		AU1
21		AUD_SAI1_RXD		AV4
23		AUD_SAI1_RXFS		AU3
24		AUD_SAI1_RXFS		AV2
25		AUD_SAI1_TXC		AU5
26		AUD_SAI1_TXD		AU1
24		AUD_SAI1_TXFS		AV2

The following table details the SAI interface signals definition.

Table 25: SAI interface signals definition

Name	Function	DIR
SAI_TXC	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_TXFS	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_TXD	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristate whenever not transmitting a word	O
SAI_RXC	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_RXFS	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_RXD	Receive Data. The receive data is sampled synchronously by the bit clock.	I

8.8 Resistive Touch

The VAR-SOM-MX8 features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

The Resistive Touch is available only in SOMs with the “TP” assembly option

Table 26: Serial Audio Interface 1 Signals

Pin#	Assy	Pin Function	Notes	Ball
187	TP	TS_X-		TSC2046.8
189	TP	TS_X+		TSC2046.6
191	TP	TS_Y+		TSC2046.7
193	TP	TS_Y-		TSC2046.9

8.9 PCIe

The VAR-SOM-MX8 exposes a single PCI Express Gen 3.0 single lane interface.

The following list the key features of the PCIe PHY:

- 1.5 / 2.5 / 3.0 / 5.0 / 6.0 Gbps Serializer / Deserializer
- 100 MHz Reference Clock
- K28.5 Detection for Word Alignment
- 8B/10B Encoding / Decoding
- Supports Spread Spectrum Clocking in Transmitter and Receiver

The PCIe controller implements the following standards:

- PCI Express Base Specification, Revision 4.0, Version 0.7
- PIPE Specification for PCI Express, Version 4.3, Intel Corporation
- PCI Local Bus Specification, Revision 3.0
- PCI Bus Power Management Specification, Revision 1.2
- PCI Express Card Electromechanical Specification, Revision 1.1

Note: Access to the above specification requires membership in PCI-SIG.

Table 27: PCIE Signals

Pin#	Assy	Pin Function	Notes	Ball
100		HSIO_PCIE_IOB_EXT_REFCLK100M_N	PCIe compliant 100MHz reference clock. Can be exported from SOM or input to the SOM. The internal PCIe reference clock is not spread spectrum capable. For PCIe Gen 3.0 or EMC/EMI sensitive applications, it is recommended to connect to an external HCSL-compatible clock source.	E25
102		HSIO_PCIE_IOB_EXT_REFCLK100M_P	PCIe compliant 100MHz reference clock. Can be exported from SOM or input to the SOM. The internal PCIe reference clock is not spread spectrum capable. For PCIe Gen 3.0 or EMC/EMI sensitive applications, it is recommended to connect to an external HCSL-compatible clock source.	F26
136		HSIO_PCIE0_RX0_N		B30
134		HSIO_PCIE0_RX0_P		A29
128		HSIO_PCIE0_TX0_N		C27
130		HSIO_PCIE0_TX0_P		B26

8.10 UART

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or multi drop mode (RS-485) support (automatic slave address detection)
- 7, 8, 9, or 10-bit data characters (7-bits only with parity), 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for RTS and CTS signals

Table 28: UART interface signals definition

Name	Function	DIR
UARTx_TXD	Transmit Bit Clock. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
UARTx_RXD	Receive data.	I
UARTx_CTS_B	Clear to send.	I
UARTx_RTS_B	Request to send.	O

Table 29: UART0 Signals

Pin#	Assy	Pin Function	Notes	Ball
84		DMA_UART0_CTS_B		AW49
86		DMA_UART0_RTS_B		AU45
83		DMA_UART0_RX		AV50
85		DMA_UART0_TX		AV48

Table 30: UART1 Signals

Pin#	Assy	Pin Function	Notes	Ball
51		DMA_UART1_CTS_B	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	AR43
50		DMA_UART1_CTS_B	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	AV46
51		DMA_UART1_RTS_B	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	AR43
50		DMA_UART1_RTS_B	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	AV46
53		DMA_UART1_RX	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	AT44

Pin#	Assy	Pin Function	Notes	Ball
52		DMA_UART1_TX	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	AY48

Table 31: UART2 Signals

Pin#	Assy	Pin Function	Notes	Ball
86		DMA_UART2_RX		AU45
175		DMA_UART2_RX		BE35
84		DMA_UART2_TX		AW49
124		DMA_UART2_TX		BE37

Table 32: UART3 Signals

Pin#	Assy	Pin Function	Notes	Ball
57		DMA_UART3_CTS_B	Referenced to pin 38 supply (1.8V/2.5/3.3V)	B50
55		DMA_UART3_RTS_B	Referenced to pin 38 supply (1.8V/2.5/3.3V)	D48
54		DMA_UART3_RX	Referenced to pin 38 supply (1.8V/2.5/3.3V)	E53
56		DMA_UART3_TX	Referenced to pin 38 supply (1.8V/2.5/3.3V)	G47

Table 33: UART4 Signals

Pin#	Assy	Pin Function	Notes	Ball
115		DMA_UART4_RX		AR47
171		DMA_UART4_TX		AU53

8.11 Flexible Controller Area Network

The Flexible Controller Area Network (FLEXCAN) module is a communication controller supporting CAN-FD (CAN Flexible Data Rate) and CAN2.0B specification.
Signal Description:

- CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
- CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

Table 34: FLEXCAN0 Signals

Pin#	Assy	Pin Function	Notes	Ball
46		DMA_FLEXCAN0_RX		C5
44		DMA_FLEXCAN0_TX		H6

Table 35: FLEXCAN1 Signals

Pin#	Assy	Pin Function	Notes	Ball
173		DMA_FLEXCAN1_RX		E5
117		DMA_FLEXCAN1_TX		G7

8.12 LPSPI

The LPSPI is a low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus, either as a master and/or as a slave.
The LPSPI supports:

- Word size = 32 bits
- Configurable clock polarity and clock phase
- Master operation supporting up to 4 peripheral chip select
- Slave operation
- Command/transmit FIFO of 64 words
- Receive FIFO of 64 words
- Flexible timing parameters in master mode, including SCK frequency and delays between PCS and SCK edges
- Support for full duplex transfers supporting 1-bit transmit and receive on each clock edge
- Support for half duplex transfers supporting 1-bit transmit or receive on each clock edge
- Support for half duplex transfers supporting 2-bit or 4-bit transmit or receive on each clock edge (master only)
- Host request input can be used to control the start time of an SPI bus transfer (master only)
- Receive data match logic supporting wakeup on data match

Table 36: SPI0 Signals

Pin#	Assy	Pin Function	Notes	Ball
79		DMA_SPI0_CS0		BC1
40		DMA_SPI0_CS1		BA3
75		DMA_SPI0_SCK		BB4
77		DMA_SPI0_SDI		BA5
70		DMA_SPI0_SDO		AY6

Table 37: SPI1 Signals

Pin#	Assy	Pin Function	Notes	Ball
39		DMA_SPI1_CS0	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_7: Low - Output from SoC High - Input to SoC	AL9
43		DMA_SPI1_SCK	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_4: Low - Output from SoC High - Input to SoC	AR9
41		DMA_SPI1_SDI	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_6: Low - Output from SoC High - Input to SoC	AR7
45		DMA_SPI1_SDO	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_5: Low - Output from SoC High - Input to SoC	AN9

Table 38: SPI3 Signals

Pin#	Assy	Pin Function	Notes	Ball
51		DMA_SPI3_SDI	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	AR43
50		DMA_SPI3_CS0	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	AV46
52		DMA_SPI3_SCK	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	AY48
53		DMA_SPI3_SDO	Used internally in SOM with "WBD" Configuration. Interface can be released by GPIO control.	AT44

8.13 Keypad

The VAR-SOM-MX8 exports a 5x3 Keypad matrix.

Keypad Key Features:

- Supports up to an 8 x 8 external key pad matrix
- Port pins can be used as general purpose I/O
- Open drain design
- Glitch suppression circuit design
- Multiple-key detection
- Long key-press detection
- Standby key-press detection
- Synchronizer chain clear
- Supports a 2-point and 3-point contact key matrix

Table 39: Keypad Signals

Pin#	Assy	Pin Function	Notes	Ball
43		LSIO_KPP0_COL3	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_4: Low - Output from SoC High - Input to SoC	AR9
80		LSIO_KPP0_COL4		AY52
69		LSIO_KPP0_COL6		AW53
48		LSIO_KPP0_COL7		BA53
45		LSIO_KPP0_ROW0	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_5: Low - Output from SoC High - Input to SoC	AN9
41		LSIO_KPP0_ROW1	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_6: Low - Output from SoC High - Input to SoC	AR7
39		LSIO_KPP0_ROW2	Pin is routed via on SOM buffer, set as Input by default. To enable buffer set GPIO2_16 Low. Pin direction can be controlled by GPIO2_7: Low - Output from SoC High - Input to SoC	AL9
82		LSIO_KPP0_ROW4		AY50
68		LSIO_KPP0_ROW5		BA51

8.14 PWM

The VAR-SOM-MX8 exports 4 General purpose Pulse Width Modulators (PWM) signals.
In addition, there is 1 dedicated PWM signals for LVDS0 interface.

PWM Features:

- 16-bit up-counter with clock source selection (bus clock, baud clock, or 32K)
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

Table 40: PWM Signals

Pin#	Assy	Pin Function	Notes	Ball
86		LSIO_PWM0_OUT		AU45
84		LSIO_PWM1_OUT		AW49
68		LSIO_PWM2_OUT		BA51
69		LSIO_PWM3_OUT		AW53
17		LVDS0_PWM0_OUT		BE39

8.15 I2C

The SOM consists of 3 I2C Interface connectivity peripherals which provides serial interface for external devices. Data rates of up to 400 kbps are supported.
In addition, there are dedicated low-speed I2C non-DMA I2C busses for HDMI, LVDS0.

Table 41: I2C0 Signals

Pin#	Assy	Pin Function	Notes	Ball
174		DMA_I2C0_SCL	SoC ball is exported via on SOM switch controlled by GPIO1_22: Low (default) - SoC Ball BN9 ball is exported High - SoC Ball BG1 is exported	BN9
176		DMA_I2C0_SDA	SoC ball is exported via on SOM switch controlled by GPIO1_22: Low (default) - SoC Ball BN7 ball is exported High - SoC Ball BN5 is exported	BN7

Table 42: I2C1 Signals

Pin#	Assy	Pin Function	Notes	Ball
80		DMA_I2C1_SCL		AY52
88		DMA_I2C1_SCL		L9
87		DMA_I2C1_SDA		H10

Table 43: I2C2 Signals

Pin#	Assy	Pin Function	Notes	Ball
48		DMA_I2C2_SCL		BA53
82		DMA_I2C2_SDA		AY50

Table 44: I2C4 Signals

Pin#	Assy	Pin Function	Notes	Ball
74		DMA_I2C4_SCL	Pin alternate function cannot be changed when using SOM with EC assembled	A9
92		DMA_I2C4_SCL		A13
30		DMA_I2C4_SDA	Pin alternate function cannot be changed when using SOM with EC assembled	D10
90		DMA_I2C4_SDA		C13

Table 45: HDMI I2C Signals

Pin#	Assy	Pin Function	Notes	Ball
174		HDMI_TX0_I2C0_SCL	SoC ball is exported via on SOM switch controlled by GPIO1_22: Low (default) - SoC Ball BN9 ball is exported High - SoC Ball BG1 is exported	BN9
176		HDMI_TX0_I2C0_SDA	SoC ball is exported via on SOM switch controlled by GPIO1_22: Low (default) - SoC Ball BN7 ball is exported High - SoC Ball BN5 is exported	BN7

Table 46: HDMI DDC Signals

Pin#	Assy	Pin Function	Notes	Ball
174		HDMI_TX0_DDC_SCL	SoC ball is exported via on SOM switch controlled by GPIO1_22: Low (default) - SoC Ball BN9 ball is exported High - SoC Ball BG1 is exported	BG1
176		HDMI_TX0_DDC_SDA	SoC ball is exported via on SOM switch controlled by GPIO1_22: Low (default) - SoC Ball BN7 ball is exported High - SoC Ball BN5 is exported	BN5

Table 47: LVDS0 I2C Signals

Pin#	Assy	Pin Function	Notes	Ball
124		LVDS0_I2C1_SCL		BE37
175		LVDS0_I2C1_SDA		BE35

8.16 General Purpose Timer

Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 48: General Purpose Timer Signals

Pin#	Assy	Pin Function	Notes	Ball
82		LSIO_GPT1_CAPTURE		AY50
48		LSIO_GPT1_CLK		BA53
68		LSIO_GPT1_COMPARE		BA51

8.17 System Control Unit

The System Controller Unit (SCU) is made of a Cortex-M4 processor running at 266MHz with 256KB of TCM and a set of peripherals and interfaces to connect to external PMIC and to control internal subsystems. The SCU Cortex-M4 is the first processor to boot the chip (see System Boot). The SCU is responsible for:

- Booting the system
- Interfacing with the external PMIC through a dedicated I2C and dedicated pins
- Managing power, clocking, and reset of internal subsystems
- Controlling pin multiplexing and IO control (drive strength and pull up/down)
- Managing resource partitioning through isolation (see xRDC chapter)
- Managing thermal

SCU UART pins are accessible via SOM test points:

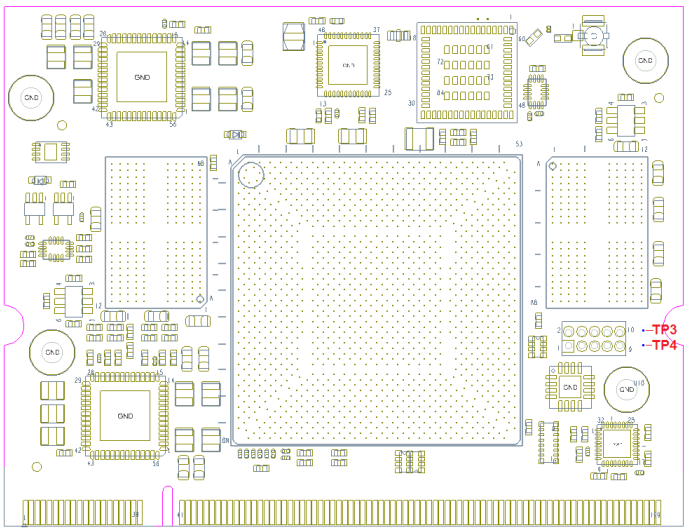


Table 49: System Control Unit Signals

Pin#	Assy	Pin Function	Notes	Ball
TP4		SCU_UART0_RX		AF28
TP3		SCU_UART0_TX		AA29

8.18 Secure Non-Volatile Storage

Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.

Table 50: Secure Non-Volatile Storage

Pin#	Assy	Pin Function	Notes	Ball
66	TM	SNVS_TAMPER_OUT0		BD46
156	TM	SNVS_TAMPER_IN0		BE41

8.19 JTAG

The SOM consists of the System JTAG Controller (SJC) which provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

Table 51: JTAG signals 10-pin Header Connector

Pin #	Assy	Pin Function	Notes	Ball
1		JTAG_VTREF	JTAG reference voltage (3.3v)	
2		JTAG_TMS	JTAG Test Mode select	BA49
3		GND	Digital Ground	
4		JTAG_TCK	JTAG Test Clock	BC51
5		GND	Digital Ground	
6		JTAG_TDO	JTAG Test Data Out	BD52
7		RTCK	JTAG Return clock	
8		JTAG_TDI	JTAG Test Data In	BE51
9		JTAG_TRST_B	JTAG TAP reset	BE53
10		JTAG_SRST_B	JTAG System reset	

8.20 Cortex M4

The SOM exposes one configurable Cortex-M4 subsystem and a dedicated Cortex-M4 subsystem within the SCU. The modular set of Cortex-M4 platform components offer a low-latency execution environment with real-time and low-power processing capability.

Table 52: Cortex M4 GPIO Signals

Pin#	Assy	Pin Function	Notes	Ball
115		M40_GPIO0_IO00		AR47
171		M40_GPIO0_IO01		AU53

Table 53: Cortex M4 Timer and PWM Module Signals

Pin#	Assy	Pin Function	Notes	Ball
115		M40_TPM0_CH0		AR47
171		M40_TPM0_CH1		AU53

8.21 General Purpose IO

The SOM provides IO pins which can be used as GPIOs. See Chapter 7 for a complete SOM connectors' signal list and GPIO multiplexing.

9. Power and Control

9.1 Power

Table 54: Power

Pin #	Pin Function	Notes
31,32,33,34,35,36 103,105,107,109, 111	VBAT	VAR-SOM-MX8 single 3.3V supply voltage input Pins 31,33,35 are disconnected from VBAT in SOMs with “CMP” assembly option
36	LICELL	RTC back-up battery 1.8V/3.0V/3.3V supply voltage input. Available only SOM with "TM" assembly option.
38	VDD_ENET1_1P8_2P5_3P3_IN	VAR-SOM-MX8 1.8V/2.5V/3.3V supply voltage input. The following SOM pins are referenced to this voltage: 40,54,55,56,57,71,73,81,96,113,120, 122,177 When using the above pins for alternate functions of ENET1: • For RMII - voltage supply should be 3.3V • For RGMII - voltage supply should be 1.8V/2.5V
104	USB_OTG1_VBUS	USB Host VBUS (5V) input
106	USB_OTG2_VBUS	USB OTG VBUS (5V) input

9.2 Ground

Table 55: Digital Ground Pins

Pin #	Pin Function	Notes
1,2,7,8,13,14,19,27,28, 37,47,58,59,66, 67,76,78,89,95,101,112, 118,126,132,138,139, 144,149,158,159,169, 172,178,179,185	GND	Digital ground Note: Pins 1,58 are connected to ground only in SOMs without “1588” assembly option
66	GND	Pin 66 is connected to ground only in SOMs without “TM” assembly option
195	AGND	Audio Interface ground reference

9.3 General System Control Signals

Table 56: General System Control Signals

Pin #	Pin Function	Notes
49	SW_3P3	SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Connect to pin 38 in case of 3.3V supply.
98	POR_B_3V3	System Reset Input. Active on falling edge. A logic low '0' on this pin will reset the system.

9.4 Boot Configuration

Table 57: SOM boot options

	Pin # 42 (LVDS0_GPIO01)	Notes
eMMC Boot	1	1) Pin 42 is pulled High internally on SOM, referenced to 3.3V. 2) To set to logic '1' or '0' externally use strong pull - 1K Ohm or less.
SD Boot	0	

10. Assembly Options

To make the solution as Flexible as possible the following assembly options were added. The assembly options help customers to order the SOM subversion that include only the needed interfaces with a lower cost.

10.1 LVDS/DSI/DP

The SOM can be ordered with one of the below assembly options. Depending on the assembly option, different SoC balls will be exported to SOM connector pins.

Table 58: LVDS/DSI/DP

	Default SOM option (LD)		Special SOM option #1 (DSI)		Special SOM option #2 (DP)	
Pin #	Pin name	Ball	Pin name	Ball	Pin name	Ball
181	LVDS0_CH1_TX3_P	BH38	MIPI_DSI0_DATA3_P	BL25	HDMI_TX0_AUX_P	BH2
183	LVDS0_CH1_TX3_N	BG37	MIPI_DSI0_DATA3_N	BN25	HDMI_TX0_AUX_N	BG3
192	LVDS0_CH1_TX2_N	BG39	MIPI_DSI0_DATA2_N	BN29	N/A	N/A
194	LVDS0_CH1_TX2_P	BH40	MIPI_DSI0_DATA2_P	BL29	N/A	N/A

10.2 Tamper

The SOM can be ordered with the Tamper related pins exposed.

Table 59: TM

	Default SOM option (no TM)		Special SOM option #1 (TM)	
Pin #	Pin name	Ball	Pin name	Ball
36	VBAT	N/A	LICELL	PF8100.46
66	GND	N/A	SNVS_TAMPER_OUT0	BD46
156	HDMI_TX0_CEC	BJ1	SNVS_TAMPER_IN0	BE41

10.3 1588

The SOM can be ordered with the 1588 interface exposed.

Table 60: 1588

	Default SOM option (no 1588)		Special SOM option #1 (1588)	
Pin #	Pin name	Ball	Pin name	Ball
1	GND	N/A	ENET1_REFCLK_125M_25M	A11
58	GND	N/A	ENET0_REFCLK_125M_25M	B10

10.4 CMP

The SOM can be ordered with pins 31,33,35 disconnected from VBAT for compatibility with i.MX6 based SOMs pinout.

Table 61: CMP

	Default SOM option (no CMP)		Special SOM option #1 (CMP)	
Pin #	Pin name	Ball	Pin name	Ball
31	VBAT	N/A	Not connected	N/A
33	VBAT	N/A	Not connected	N/A
35	VBAT	N/A	Not connected	N/A

10.5 Ethernet PHY

The SOM can be ordered without Ethernet0 PHY chip assembled, it allows reducing the overall cost of the product in case the Ethernet Interfaces are not used.

10.6 Analog Audio Codec

The SOM can be ordered without Audio Codec chip assembled, it allows reducing the overall cost of the product in case the Analog Audio is not used.

10.7 Dual band Wi-Fi and BT/BLE combo

The SOM can be ordered without the Dual band Wi-Fi and BT/BLE combo chip assembled, it allows reducing the overall cost of the product in case the Wi-Fi and BT/BLE is not used.

10.8 Bluetooth

The SOM can be ordered with UART1 interface not connected to WiFi/Bluetooth module. In this case the Bluetooth interface will not be available. For testing purposes same operation can be achieved by pulling GPIO4_IO26. It will disable ON-SOM level translator and allow UART1 operation externally.

10.9 Resistive Touch

The SOM can be ordered without Resistive Touch controller assembled, it allows reducing the overall cost of the product in case the Resistive Touch is not used.

10.10 LPDDR4

The SOM can be ordered with different RAM size capacities, it allows reducing the overall cost of the product in case lower RAM size is sufficient.

10.11 eMMC

The SOM can be ordered with different eMMC size capacities, it allows reducing the overall cost of the product in case lower eMMC size is sufficient.

11. Electrical Specifications

11.1 Absolute Maximum Ratings

Table 62: Absolute Maximum Ratings

Pin #	Min	Max	Units	Comments
VBAT	-0.3	3.6	V	
LICELL	-0.3	5.5	V	
USB_OTG1_VBUS/ USB_OTG2_VBUS	-0.3	5.5	V	
USB_OTG1_DP/USB_OTG1_DN	-0.3	3.63	V	
USB_OTG2_DP/USB_OTG2_DN				
VDD_ENET1_1P8_2P5_3P3_IN	-0.3	3.8	V	
Vin/Vout input/output voltage range (GPIO Type Pins)	-0.3	OVDD+0.3		OVDD is the I/O supply voltage
ESD damage immunity Human Body Model (HBM)	--	2000	V	PCIe differential pairs, HDMI-TX and USB3 (including OTG2) interfaces are 1000V HBM instead of 2000V
ESD damage immunity Charge Device Model (CDM)	--	500	V	PCIe differential pairs, HDMI-TX and USB3 (including OTG2) interfaces are 250V HBM instead of 500V

11.2 Operating Conditions

Table 63: Operating Ranges

Parameter		Min.	Typ.	Max.	Unit
VBAT		3.25	3.3	3.45	V
LICELL		-	-	4.2	V
VDD_ENET1_1P8_2P5_3P3_IN	1.8	1.65	1.8	1.95	V
	2.5	2.4	2.5	2.6	
	3.3	3	3.3	3.6	

11.3 Power Consumption

Table 64: VAR-SOM-MX8 Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.3V	1.53A	5.04W	Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz
Run	3.3V	1.37A	4.52W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	3.3V	1.05A	3.46W	Linux up
Standby	3.3V	TBD	TBD	Memory retention mode
Off (RTC)	3V	0.18mA	0.54mW	All power rails are Off, only Internal SOC RTC is powered

NOTE

Setup:
HW: VAR-SOM-MX8QM_1612C_4096R_16G_AC_EC_TP_WBD_ET_REV1.1
SW: fsl-imx8qm-var-som.dtb

DISCLAIMER:
The power consumption measurements apply only to limited operation scenarios. Actual power consumption may vary depending on the interfacing peripherals and user application modes; Users must conduct testing per their specific operation scenarios.

12. Environmental Specifications

Table 65: Environmental Specifications

Parameter	Min	Max
Extended Operating Temperature Range	-25°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model:		
50°C, Class B-1, GM	121K hrs.	
50°C, Class B-1, GB	1400K hrs.	

Note: Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

13. Mechanical Drawings

13.1 Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-2.5-M2-B**

13.2 Thermal Management

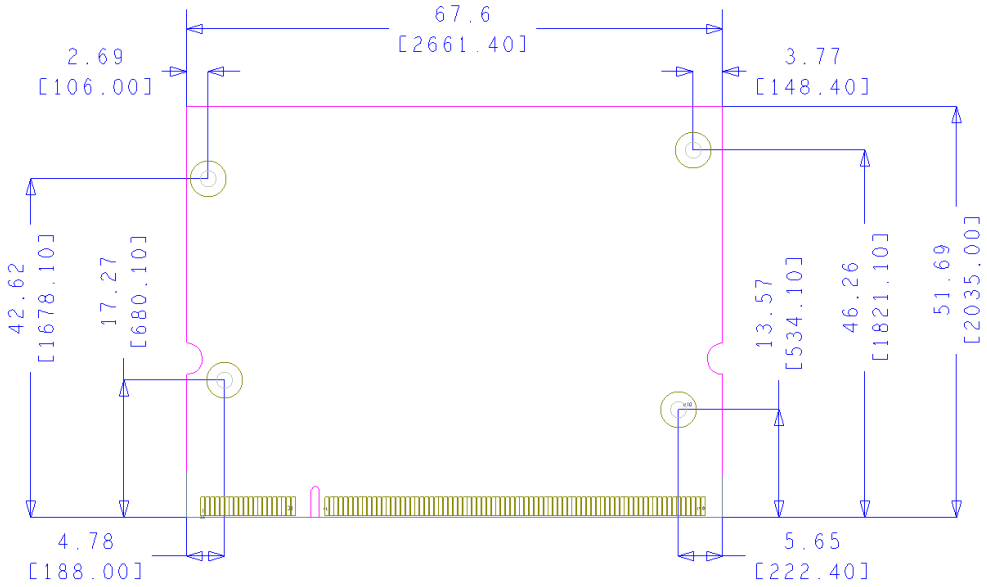
Certain operation scenarios may prompt the use of an external heat dissipation solution.
To handle intensive applications where thermal management is required, Variscite offers a heat sink designed for the VAR-SOM-MX8/X:

Variscite PN: VHP-MX8

DISCLAIMER:
Implemented solution may vary depending on the device operation scenario as well as its mechanical design. Thermal solution must be evaluated.

13.3 SOM Dimensions

Figure 4: VAR-SOM-MX8 Mechanics in millimeters [mils]



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