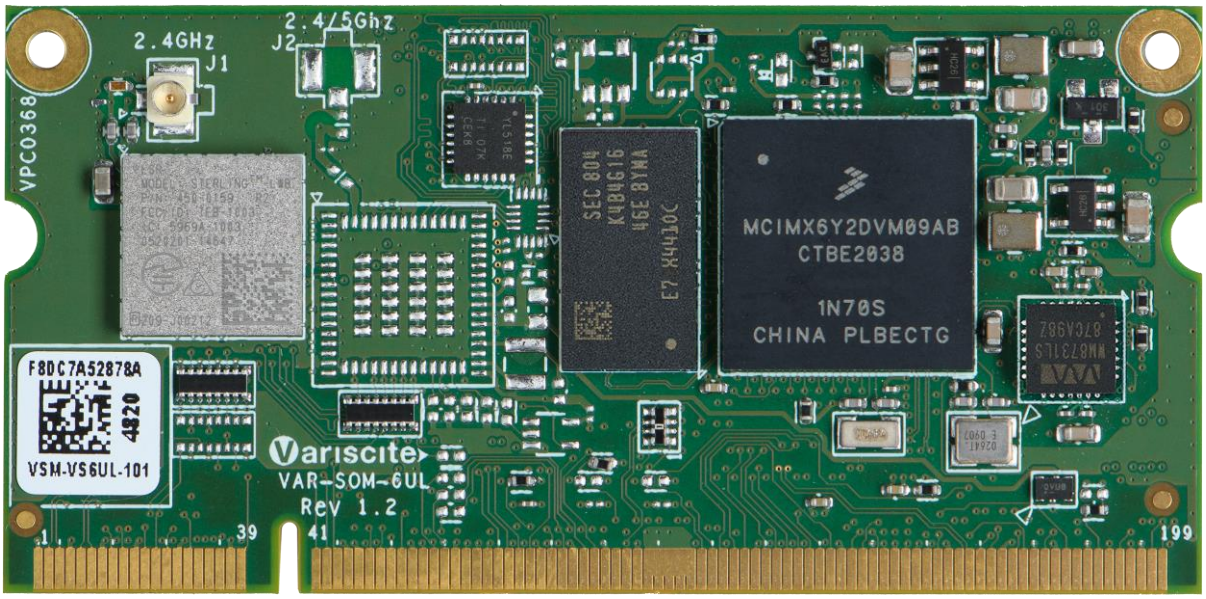
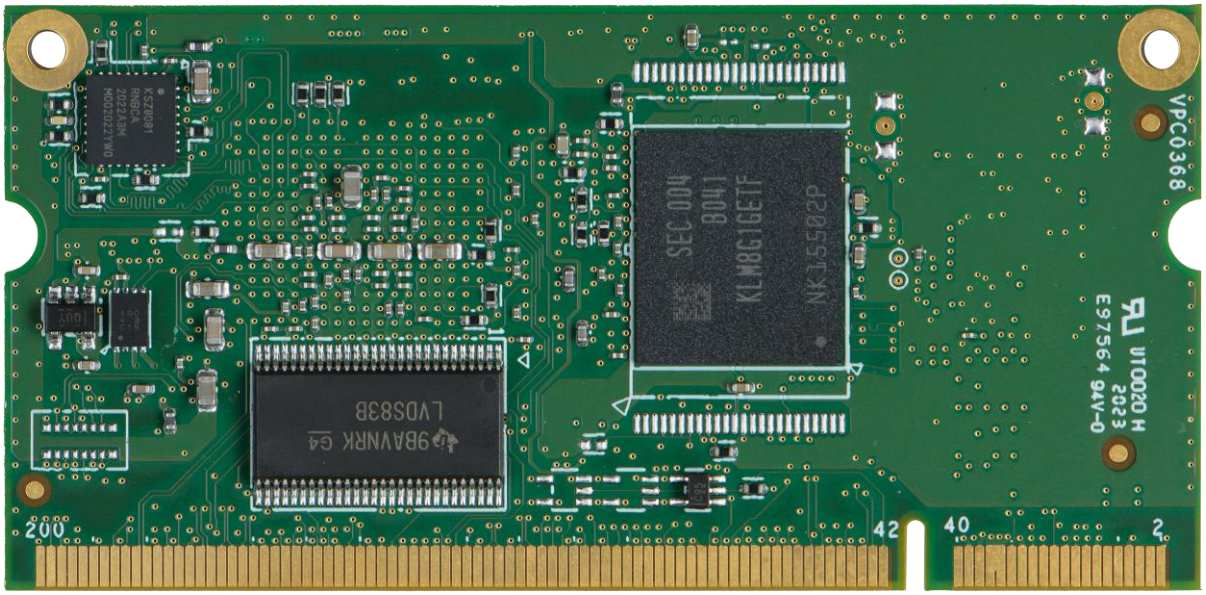
VARISCITE LTD.

VAR-SOM-6UL V1.x Datasheet

NXP i.MX 6UL™/6ULL™/6ULZ™- based System-on-Module





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VAR-SOM-6UL Datasheet

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1. Document Revision History

Revision	Date	Notes
1.0	Apr 21, 2019	Initial
1.1	May 13,2019	Block Diagram changed: SAI1 is compatible with other SOMs. Syntax errors fixed. ESPI2 compatible pins table changed.
1.2	Jun 12,2019	Pin 121, Pin 115 assembly options changed. EPDC Table changed i.MX6ULZ Notes added
1.3	Jun 23,2021	New SOM revision 1.2 - LVDS Bridge PN changed in Table 2. - SOM Pictures updated Table 1 EC option description changed.
1.4	May 1, 2022	Updated sections: 4.2, 5.5, 8.3
1.5	Feb 27, 2023	Updated section 13 Updated the eMMC sections 4.2, 5.2
1.6	March 5, 2023	Corrected Typo Section 5.4 Heading
1.7	Feb 8, 2024	Updated section 5.5.2
1.8	October 13, 2024	Corrected ethernet PHY P/N typo sections 5.3,7.3,8.8

2. Table of Contents

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4. Overview

4.1 General Information

The VAR-SOM-6UL is a power-optimized cost-effective System-on-Module that perfectly fits various embedded and industrial products and segment. It is based on i.MX6UL/6ULL/6ULZ up to 900MHz ARM® Cortex™-A7 multipurpose processor from NXP/Freescale.

The VAR-SOM-6UL provides an ideal building block for simple integration with a wide range of products in target markets requiring low power consumption, small size and a very cost-effective solution.

Variscite also provides a complete hardware and software development kit (DVK) for the SoM in the form of a carrier board with 200pins edge connector for the VAR-SOM-6UL and an optional TFT display and touch panel. The carrier board of the VAR-SOM-6UL is ideal not only as reference for the customer to develop its own custom board but also as a cost-effective solution for production.

Supporting products:

- Concerto-Board – carrier board, complements the VAR-SOM-6UL
  - ✓ Carrier Board, compatible with VAR-SOM-6UL
  - ✓ Schematics
- VAR-DVK-6UL: full development kit, including:
  - ✓ Concerto-Board
  - ✓ VAR-SOM-6UL
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

Contact Variscite support services for further information: mailto:support@variscite.com.

4.2 Feature Summary

- NXP/Freescale i.MX 6UltraLite / 6ULL
  - Power optimized up to 900MHz ARM Cortex-A7™
  - Up to 512MB DDR3L, 512MB NAND / 128GB eMMC
  - Integrated security features
  - 2D pixel acceleration engine (PxP)
- Display Support
  - 18bits LVDS support up to WXGA (1366 x 768)
  - 24bits Parallel LCD up to WXGA (1366 x 768)
  - Touch screen controller
  - EPDC for E-Ink EPD panels up to 2048x1536@106Hz (6ULL only)
- Networking
  - 2 x 10/100Mbps Ethernet
  - Certified Wi-Fi 802.11 b/g/n (Single Band Option)
  - Certified Wi-Fi 802.11 ac/a/b/g/n (Dual Band Option)
  - Bluetooth: 5.2 / BLE
- USB
  - USB 2.0 OTG
  - USB 2.0 Host
- Audio
  - Digital audio SAI/SPDIF
  - ESAI (6ULL only)
  - Analog microphone (stereo)
  - Headphone out, line-in
- Camera
  - Parallel input
- Other Interfaces:
  - Dual CAN, I2C, SPI, PWM, JTAG, UART, SD/MMC
- Power
  - Single 3.3V
  - Low Power consumption, optimized in both operational and suspend modes
- Dimensions (W x L x H): 67.5mm x 33mm x 4mm
- Industrial temperature support

Note: NXP/Freescale i.MX 6ULZ SOC has limited feature list. Please check out NXP datasheet for exact differences.

4.3 Block Diagram

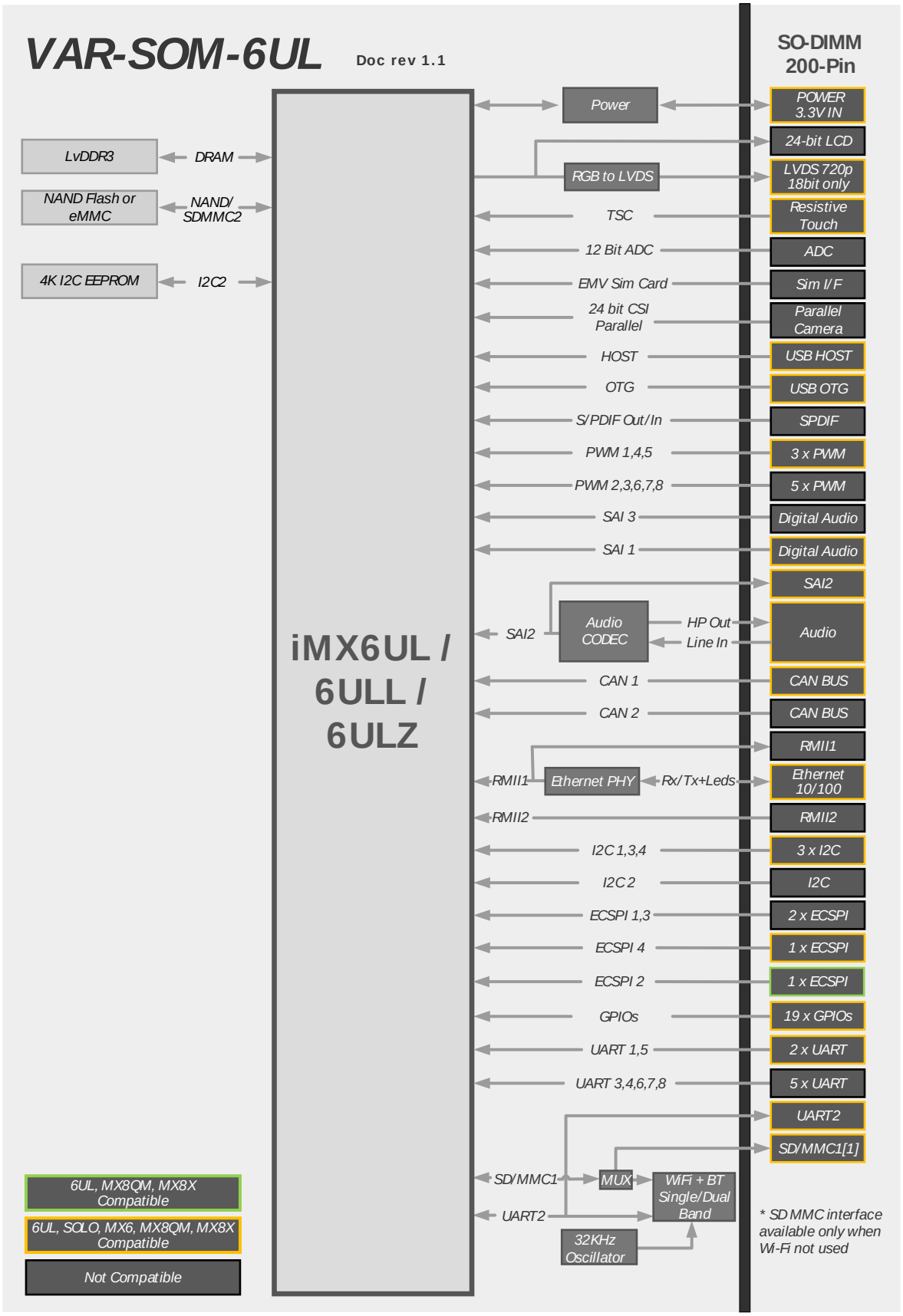


Figure 1 : VAR-SOM-6UL Block Diagram

5. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-6UL.
NXP/Freescale i.MX6ULZ does not have all below features and interfaces.
Please check out i.MX6ULZ datasheet and reference manual for available interfaces.

5.1 NXP/Freescale i.MX 6UL/6ULL

5.1.1 Overview

The i.MX 6UltraLite / 6ULL is a high performance, ultra-efficient processor family with featuring NXP/Freescale's advanced implementation of the single ARM Cortex®-A7 core, which operates at speeds of up to 900MHz. i.MX 6UltraLite / 6ULL includes integrated power management module that reduces the complexity of external power supply and simplifies the power sequencing. Each processor in this family provides various memory interfaces, Quad SPI, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors. The i.MX 6UltraLite / 6ULL processors are specifically useful for applications such as:

- Electronics Point-of-Sale device
- Telematics
- IoT Gateway
- Access control panels
- Human Machine Interfaces (HMI)
- Smart appliances
- Industrial control and automation

5.1.2 ARM Cortex-A7 Platform

The i.MX 6UltraLite / 6ULL processors are based on ARM Cortex-A7 MPCore™ Platform, which has the following features:

- Supports single ARM Cortex-A7 MPCore (with TrustZone) with:
    - 32 KByte L1 Instruction Cache
    - 32 KByte L1 Data Cache
    - Private Timer and Watchdog
    - Cortex-A7 NEON MPE (Media Processing Engine) Co-processor
- General Interrupt Controller (GIC) with 128 interrupts support
- Global Timer
- Snoop Control Unit (SCU)
- 128 KB unified I/D L2 cache
- Single Master AXI bus interface output of L2 cache
- NEON MPE coprocessor
    - SIMD Media Processing Architecture
    - NEON register file with 32x64-bit general-purpose registers
    - NEON Integer execute pipeline (ALU, Shift, MAC)
    - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
    - NEON load/store and permute pipeline
    - 32 double-precision VFPv3 floating point registers

5.1.3 Memory Interfaces

The SoC-level memory system consists of the following additional components:

- Boot ROM, including HAB (96 KB)
- Internal multimedia/shared, fast access RAM (OCRAM, 128 KB)
- Secure/non-secure RAM (32 KB)

External memory interfaces: The i.MX 6UltraLite / 6ULL processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
SoM Supports:

- 16-bit LV-DDR3-800
- 8-bit NAND-Flash

5.1.4 DMA engine

The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:

- Powered by a 16-bit Instruction-Set micro-RISC engine
- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- 48 events with total flexibility to trigger any combination of channels
- Memory accesses including linear, FIFO, and 2D addressing
- Shared peripherals between ARM and SDMA Very fast Context-Switching with 2-level priority based preemptive multi-tasking
- DMA units with auto-flush and prefetch capability
- Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)
- DMA ports can handle unit-directional and bi-directional flows (copy mode)
- Up to 8-word buffer for configurable burst transfers for EMIv2.5
- Support of byte-swapping and CRC calculations
- Library of Scripts and API is available

5.1.5 Display Subsystem

The chip display and graphics subsystem consist of the dedicated modules found here.

- LCDIF (LCD interface): 24-bit parallel RGB LCD interface.
  The LCDIF is a general-purpose display controller that is used to drive a wide range of display devices. These displays can vary in size and capability. Many of these displays have had an asynchronous parallel MPU interface for command and data transfer to an integrated frame buffer. There are other popular displays that support moving pictures and require the RGB interface mode or the VSYNC mode for high-speed data transfers. In addition to these displays, it is also common to provide support for digital video encoders that accept ITU-R BT.656 format 4:2:2 YCbCr digital component video and convert it to analog TV signals. The LCDIF block supports these different interfaces by providing fully programmable functionality. The block has several major features:
    - Bus master interface to source frame buffer data for display refresh and a DMA interface to manage input data transfers from the LCD requiring minimal CPU overhead.
    - 8/16/18/24/32-bit LCD data bus support available depending on I/O mux options.

    - Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
    - ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation
- PXP pixel pipeline: pixel/image processing engine for LCD display
  The pixel pipeline is used to perform image processing on image/video buffers before sending to an LCD display. The main features of PXP include:
    - Multiple input/output format support, including YUV/RGB/Grayscale
    - Supports both RGB/YUV scaling
    - Supports overlay with Alpha blending
- CSI (camera sensor interface): up to 16-bit parallel interface for image sensor.
  The CSI enables the chip to connect directly to external CMOS image sensors. CMOS image sensors are separated into two classes, dumb and smart. Dumb sensors are those that support only traditional sensor timing (Vertical SYNC and Horizontal SYNC) and output only Bayer and statistics data, while smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats). The capabilities of the CSI include:
    - Configurable interface logic to support most commonly available CMOS sensors.
    - Support for CCIR656 video interface as well as traditional sensor interface.
    - 8-bit/24-bit data port for YCC, YUV, or RGB data input.
    - 8-bit/10-bit/16-bit data port for Bayer data input.
    - Full control of 8-bit/pixel, 10-bit/pixel or 16-bit/pixel data format to 32-bit receive FIFO packing.
    - 128 × 32 FIFO to store received image pixel data. Receive FIFO overrun protection mechanism.
    - Embedded DMA controllers to transfer data from receive FIFO or statistic FIFO through AHB bus.
    - Support 2D DMA transfer from the receive FIFO to the frame buffers in the external memory.
    - Support double buffering two frames in the external memory.
    - Single interrupt source to interrupt controller from maskable interrupt sources: Start of Frame, End of Frame, Change of Field, FIFO full, FIFO overrun, DMA transfer done, CCIR error and AHB bus response error.
    - Configurable master clock frequency output to sensor.
    - Statistic data generation for Auto Exposure (AE) and Auto White Balance (AWB) control of the camera (only for Bayer data and 8-bit/pixel format).

5.1.6 Audio Back End

- Medium Quality Sound (MQS)
  MQS is used to generate medium quality audio via a standard GPIO in the pinmux. The user can connect stereo speakers or headphones to a power amplifier without an additional DAC chip.
    - 2-channel, MSB-valid 16 bit, MSB first
    - Frame sync aligned with the left channel data
    - 44.1 kHZ or 48 kHZ I2S signals from SAI1
    - SNR target as no more than 20 dB for the signals below 10 kHZ
    - Signals Over 10 kHZ have worse THD + N values
- Synchronous Audio Interface (SAI)
    - Transmitter with independent Bit Clock and Frame Sync supporting 1 data line
    - Receiver with independent Bit Clock and Frame Sync supporting 1 data line

- Maximum Frame Size of 32 Words
- Word size programmable from 8-bits to 32-bits
- Word size configured separately for first word and remaining words in frame.
- Asynchronous FIFO for each Transmit and Receive data line
- Graceful restart after FIFO Error

- Sony/Philips Digital Interface (SPDIF)
  The Sony/Philips Digital Interface (SPDIF) module is a stereo that allows the processor transmit digital audio over it using the IEC60958 standard, consumer format. i.MX 6UltraLite / 6ULL provides one SPDIF transmitter with one output and one SPDIF receiver with four inputs.
  - The SPDIF allows the handling of both SPDIF channel status (CS) and User (U) data.
  - For the SPDIF transmitter, the audio data is provided by the processor via the SPDIFTxLeft and SPDIFTxRight registers, and the data is stored in two 16-word-deep FIFOs, one for the right channel, the other for the left channel. The FIFOs support programmable watermark levels so that FIFO Empty service request can be triggered when the combined number of empty data words locations in both FIFOs is 8, 16, 24 or 32 words. It is recommended to program the watermark level to trigger a FIFO Empty service request when 16-word locations are empty. For optimal performance when servicing the FIFO Empty service request, the FIFOs should be written alternately, starting with the left channel FIFO. The Channel Status bits are also provided via the corresponding registers. The SPDIF transmitter generates an SPDIF output bit stream in the bi-phase mark format (IEC 60958), which consists of audio data, channel status and user bits.
  - The data handled by the SPDIF module is 24-bit wide. The 24-bit SPDIF data is aligned in the 24 least significant bits of the 32-bit shared peripheral bus data word. The 8 most significant bits of the 32-bit word are ignored by the SPDIF Transmitter when data is being stored in the Transmit FIFOs from the peripheral bus. The 8 most significant bits of the 32-bit word are zeroed by the SPDIF Receiver module when the data is being read from the Receiver FIFOs to the peripheral bus.
  - Note that 16-bit data is left-aligned in the 24-bit word format of the SPDIF. When 16-bit data is to be transmitted, the 32-bit word to be written to the SPDIF Transmit FIFOs should be created as follows: the 16-bit data should be located in the middle two bytes of the 32-bit data word and the 8 bits of the LSB must be set to zero, while the 8 bits of the MSB will be ignored.
  - The SPDIF Transmit clock is generated by the SPDIF internal clock generator module and the clock sources are from outside of the SPDIF block. The clock sources should provide a clock that is at least 64 x Fs, where Fs is the sampling frequency. The external clock source should provide at least 128 x Fs. Clocks of higher frequency may be provided as long as the multiplication factor is a power of 2 (for example, 128x, 256x or 512x). Also, clock frequency precision of 100ppm or better should be provided

5.1.7 10/100 Ethernet Controller

The core implements a dual speed 10/100 Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full duplex 10/100 Mbit/s Ethernet LANs.
The MAC operation is fully programmable and can be used in Network Interface Card (NIC), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819.

The core also implements a hardware acceleration block to optimize the performance of network controllers providing TCP/IP, UDP, and ICMP protocol services. The acceleration block performs critical functions in hardware, which are typically implemented with large software overhead.
The core implements programmable embedded FIFOs that can provide buffering on the receive path for lossless flow control.
Advanced power management features are available with magic packet detection and programmable power-down modes.
A unified DMA (uDMA), internal to the ENET module, optimizes data transfer between the ENET core and the SoC, and supports an enhanced buffer descriptor programming model to support IEEE 1588 functionality.
The programmable 10/100 Ethernet MAC with IEEE 1588 integrates a standard IEEE 802.3 Ethernet MAC with a time-stamping module. The IEEE 1588 standard provides accurate clock synchronization for distributed control nodes for industrial automation applications.
Ethernet MAC features:

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking
- Supports zero-length preamble
- Dynamically configurable to support 10/100 Mbit/s operation
- Supports 10/100 Mbit/s full-duplex and configurable half-duplex operation
- Compliant with the AMD magic packet detection with interrupt for node remote power management
- Seamless interface to commercial Ethernet PHY devices via one of the following:
    - 4-bit Media Independent Interface (MII) operating at 2.5/25 MHz.
    - 4-bit non-standard MII-Lite (MII without the CRS and COL signals) operating at 2.5/25 MHz.
    - 2-bit Reduced MII (RMII) operating at 50 MHz.
- Simple 64-Bit FIFO user-application interface
- CRC-32 checking at full speed with optional forwarding of the frame check sequence (FCS) field to the client
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- In full-duplex mode:
    - Implements automated pause frame (802.3 x31A) generation and termination, providing flow control without user application intervention
    - Pause quanta used to form pause frames — dynamically programmable
    - Pause frame generation additionally controllable by user application offering flexible traffic flow control
    - Optional forwarding of received pause frames to the user application
    - Implements standard flow-control mechanism
- In half-duplex mode: provides full collision support, including jamming, backoff, and automatic retransmission
- Supports VLAN-tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames)
- Programmable promiscuous mode support to omit MAC destination address checking on receive
- Multicast and unicast address filtering on receive based on 64-entry hash table, reducing higher layer processing load
- Programmable frame maximum length providing support for any standard or proprietary frame length
- Statistics indicators for frame traffic and errors (alignment, CRC, length) and pause frames providing for IEEE 802.3 basic and mandatory management information database (MIB) package and remote network monitoring (RFC 2819)

- Simple handshake user application FIFO interface with fully programmable depth and threshold levels
- Provides separate status word for each received frame on the user interface providing information such as frame length, frame type, VLAN tag, and error information
- Multiple internal loopback options
- MDIO master interface for PHY device configuration and management supports two programmable MDIO base addresses, and standard (IEEE 802.3 Clause 22) and extended (Clause 45) MDIO frame formats
- Supports legacy FEC buffer descriptors
- Interrupt coalescing reduces the number of interrupts generated by the MAC, reducing CPU loading

5.2 Memory

5.2.1 RAM

The VAR-SOM-6UL is available with up to 512MB of DDR3L memory.

5.2.2 Non-volatile Storage Memory

The VAR-SOM-6UL is available with a variety of non-volatile storage memory options, used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.
The VAR-SOM-6UL can arrive with up to 512MB SLC NAND flash or up to 128GB MLC eMMC (note: it is not possible to use both on-SOM NAND and eMMC at the same time).

5.3 10/100 Ethernet PHY

The VAR-SOM-6UL features Micrel™ KSZ8081RNB Ethernet PHY. KSZ8081RNB is a single supply 10Base-T/100BaseTX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.
The KSZ8081RNB is a highly integrated PHY solution. It reduces the board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low noise regulator to supply the 1.2V core and by offering 1.8/2.5/3.3V interface support.

5.4 WM8731L Audio

The WM8731L is low power stereo CODEC with an integrated headphone driver. The WM8731/L is designed specifically for portable MP3 audio and speech players and recorders. The WM8731 is also ideal for MD, CD-RW machines and DAT recorders. Stereo line and mono microphone level audio inputs are provided, along with a mute function, programmable line level volume control and a bias voltage output suitable for an electret type microphone. Stereo 24-bit multi-bit sigma delta ADCs and DACs are used with oversampling digital interpolation and decimation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported. Stereo audio outputs are buffered for driving headphones from a programmable volume control, line level outputs are also provided along with anti-thump mute and power up/down circuitry.
Features:

- Highly Efficient Headphone Driver
- Audio Performance
    - ADC SNR 90dB ('A' weighted)
    - DAC SNR 100dB ('A' weighted)
- ADC and DAC Sampling Frequency: 8kHz – 96kHz
- Selectable ADC High Pass Filter
- 2 or 3-Wire MPU Serial Control Interface
- Programmable Audio Data Interface Modes
    - I2S, Left, Right Justified or DSP
    - 16/20/24/32-bit Word Lengths
    - Master or Slave Clocking Mode
- Microphone Input and Electret Bias with Side Tone Mixer Digital microphone

5.5 Wi-Fi + BT

5.5.1 VAR-SOM-6UL Dual Band Option

The VAR-SOM-6UL contains LSR's pre-certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 5.2 wireless connectivity.

5.5.2 VAR-SOM-6UL Single Band Option

The VAR-SOM-6UL contains LSR's pre-certified high-performance Sterling-LWB™ 2.4 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW4343W chipset supporting IEEE 802.11 b/g/n, BT 2.1+EDR, and BLE 5.1 wireless connectivity.

Both the VAR-SOM-6UL modules realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

VAR-SOM-6UL Key Features:

- IEEE 802.11 ac/a/b/g/n (Dual Band Option)
- IEEE 802.11 b/g/n (Single Band Option)
- Bluetooth 2.1+EDR, and BLE 5.2
- U.FL connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- SIG certified Bluetooth driver
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- Industrial operating Temperature Range: -40 to +85

6. VAR-SOM-6UL Hardware Configuration

The table below lists the Hardware configurations options orderable for the VAR-SOM-6UL.

Table 1 Hardware Configuration Options

Option	Description
EC	Ethernet PHY assembled on SOM
AC	Audio Codec assembled on SOM
WB	Single band Wi-Fi and BT/BLE combo assembled on SOM
WBD	Dual band Wi-Fi and BT/BLE combo assembled on SOM
TP	Resistive Touch option assembled on SOM
LD	LVDS Bridge assembled on SOM
eMMC	eMMC storage memory option assembled on SOM
NAND	NAND storage memory option assembled on SOM

Note: Other orderable options are available and are not part of this datasheet.
Please refer to Variscite official website for full list of configuration options.

7. External Connectors

7.1 Board to Board Connector

The VAR-SOM-6UL exposes a 200-pin SO-DIMM connector.

- The recommended mating connectors for baseboard interfacing are:
    1. Concraft - 0701A0BE52E
    2. Tyco Electronics -1565917-4

7.2 Wi-Fi & BT Connector

In Modules with Wi-Fi "WBD" Configuration - a combined Wi-Fi + BT antenna connector is assembled.

- Connector type: U.FL JACK connector
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 VAR-SOM-6UL Connector Pin-out

Table 2: VAR-SOM-6UL Pinout

Pin #	Assembly	Pin Name	Notes	GPIO	Ball
1		DGND			
2		DGND			
3	EC	ETH_RXDP			KSZ8081RNB-5
3	No EC	NC			
4					
5	EC	ETH_RXDN			KSZ8081RNB-4
5	No EC	NC			
6					
7		DGND			
8		DGND			
9	EC	ETH_TXDP			KSZ8081RNB-7
9	No EC	NC			
10					
11	EC	ETH_TXDN			KSZ8081RNB-6
11	No EC	NC			
12					
13		DGND			
14		DGND			
15	EC	LINKSPEED			KSZ8081RNB-31
15	No EC	NC			
16	EC	LINKLED			KSZ8081RNB-30
16	No EC	NC			
17		PWM4_OUT		GPIO1_IO[5]	SOC-M17
18	AC	NC			
18	No AC	SAI2_TX_DATA		GPIO1_IO[15]	SOC-N14
19		DGND			
20	AC	NC			
20	No AC	SAI2_MCLK		GPIO1_IO[11]	SOC-P14
21		SAI1_RX_DATA		GPIO4_IO[27]	SOC-D2
22		SAI1_RX_BCLK		GPIO4_IO[24]	SOC-E1
23		SAI1_RX_SYNC		GPIO4_IO[23]	SOC-E2
24		SAI1_TX_SYNC		GPIO4_IO[25]	SOC-D4
25		SAI1_TX_BCLK		GPIO4_IO[26]	SOC-D3
26		SAI1_TX_DATA		GPIO4_IO[28]	SOC-D1

Pin #	Assembly	Pin Name	Notes	GPIO	Ball
27		DGND			
28		DGND			
29		GPIO1_10		GPIO1_IO[10]	SOC-P15
30		MDIO		GPIO1_IO[6]	SOC-K17
31		DGND			
32		VCC_3V3_IN			
33		DGND			
34		VCC_3V3_IN			
35		DGND			
36		VCC_COIN			SOC-P12
37		DGND			
38		VCC_3V3_IN			
39		ECSPI4_SS0		GPIO2_IO[15]	SOC-D16
40					
41		ECSPI4_MISO		GPIO2_IO[14]	SOC-D17
42		BOOT_SEL			
43		ECSPI4_SCLK		GPIO2_IO[12]	SOC-A16
44		CAN1_TX		GPIO1_IO[26]	SOC-H15
45		ECSPI4_MOSI		GPIO2_IO[13]	SOC-B15
46		CAN1_RX		GPIO1_IO[27]	SOC-G14
47		DGND			
48		UART3_RX		GPIO1_IO[25]	SOC-H16
49		VCC_3V3			
50		BT_UART_CTS_B	Can be used only when BT is OFF or Not assembled	GPIO1_IO[22]	SOC-J15
51		BT_UART_RTS_B	Can be used only when BT is OFF or Not assembled	GPIO1_IO[23]	SOC-H14
52		BT_UART_TX	Can be used only when BT is OFF or Not assembled	GPIO1_IO[20]	SOC-J17
53		BT_UART_RX	Can be used only when BT is OFF or Not assembled	GPIO1_IO[21]	SOC-J16
54		UART5_RX		GPIO4_IO[22]	SOC-E3
55		UART5_CTS		GPIO1_IO[9]	SOC-M15
56		UART5_TX		GPIO4_IO[21]	SOC-E4
57		UART5_RTS		GPIO1_IO[8]	SOC-N17
58		DGND			
59		DGND			
60		CONN_CLK	Can be used only when Wi-Fi module is OFF or Not assembled	GPIO2_IO[17]	SOC-C1

Pin #	Assembly	Pin Name	Notes	GPIO	Ball
61		CONN_DATA2	Can be used only when Wi-Fi module is OFF or Not assembled	GPIO2_IO[20]	SOC-B1
62		CONN_DATA0	Can be used only when Wi-Fi module is OFF or Not assembled	GPIO2_IO[18]	SOC-B3
63		CONN_DATA1	Can be used only when Wi-Fi module is OFF or Not assembled	GPIO2_IO[19]	SOC-B2
64		CONN_CMD	Can be used only when Wi-Fi module is OFF or Not assembled	GPIO2_IO[16]	SOC-C2
65		CONN_DATA3	Can be used only when Wi-Fi module is OFF or Not assembled	GPIO2_IO[21]	SOC-A2
66		DGND			
67		DGND			
68		PWM2_OUT		GPIO3_IO[6]	SOC-A9
69		PWM1_OUT		GPIO3_IO[5]	SOC-B9
70		ECSPI2_MOSI		GPIO1_IO[30]	SOC-F17
71		NAND_CE1_B		GPIO4_IO[14]	SOC-B5
72		GPIO5_3		GPIO5_IO[3]	SOC-P10
73		GPIO5_1		GPIO5_IO[1]	SOC-R9
74		MDC		GPIO1_IO[7]	SOC-L16
75		ECSPI2_SCLK		GPIO1_IO[28]	SOC-G17
76		DGND			
77		ECSPI2_MISO		GPIO1_IO[31]	SOC-G13
78		DGND			
79		ECSPI2_SS0		GPIO1_IO[29]	SOC-G16
80		GPIO1_0		GPIO1_IO[0]	SOC-K13
81		GPIO5_7		GPIO5_IO[7]	SOC-N10
82	LD	LCD_DATA11	Must be left floating	GPIO3_IO[16]	SOC-D12
82	No LD	LCD_DATA11		GPIO3_IO[16]	SOC-D12
83		DEBUG_UART_RX		GPIO1_IO[17]	SOC-K16
84		DEBUG_UART_RTS_B		GPIO1_IO[19]	SOC-J14
85		DEBUG_UART_TX		GPIO1_IO[16]	SOC-K14
86		DEBUG_UART_CTS_B		GPIO1_IO[18]	SOC-K15
87		I2C1_SDA		GPIO4_IO[17]	SOC-F5
88		I2C1_SCL		GPIO4_IO[18]	SOC-E5
89		DGND			
90		I2C3_SDA		GPIO2_IO[9]	SOC-C16
91		BOOT1		GPIO5_IO[11]	SOC-U10

Pin #	Assembly	Pin Name	Notes	GPIO	Ball
92		I2C3_SCL		GPIO2_IO[8]	SOC-C17
93		BOOT0		GPIO5_IO[10]	SOC-T10
94		OTG1_ID		GPIO1_IO[24]	SOC-H17
95		DGND			
96	LD	LCD_DATA6	Must be left floating	GPIO3_IO[11]	SOC-A10
96	No LD	LCD_DATA6		GPIO3_IO[11]	SOC-A10
97					
98		POR			SOC-P8
99					
100	eMMC	NAND_CLE		GPIO4_IO[15]	SOC-A4
100	NAND	NC			
101		DGND			
102	eMMC	NAND_WP_B		GPIO4_IO[11]	SOC-D5
102	NAND	NC			
103		VCC_3V3_IN			
104		USB_OTG2_VBUS			SOC-U12
105		VCC_3V3_IN			
106		USB_OTG1_VBUS			SOC-T12
107		VCC_3V3_IN			
108		USB_OTG2_DN			SOC-T13
109		VCC_3V3_IN			
110		USB_OTG2_DP			SOC-U13
111		VCC_3V3_IN			
112		DGND			
113	LD	LCD_DATA7	Must be left floating	GPIO3_IO[12]	SOC-D11
113	No LD	LCD_DATA7		GPIO3_IO[12]	SOC-D11
114		USB_OTG1_DN			SOC-T15
115		LCD_DATA17	Must be left floating	GPIO3_IO[22]	SOC-B13
116		USB_OTG1_DP			SOC-U15
117	LD	LCD_DATA4	Must be left floating	GPIO3_IO[9]	SOC-C10
117	No LD	LCD_DATA4		GPIO3_IO[9]	SOC-C10
118		DGND			
119	LD	LCD_DATA2	Must be left floating	GPIO3_IO[7]	SOC-E10
119	No LD	LCD_DATA2		GPIO3_IO[7]	SOC-E10
120		GPIO5_5		GPIO5_IO[5]	SOC-N8
121	LD	LCD_DATA3	Must be left floating	GPIO3_IO[8]	SOC-D10
121	No LD	LCD_DATA3		GPIO3_IO[8]	SOC-D10

Pin #	Assembly	Pin Name	Notes	GPIO	Ball
122		GPIO5_9		GPIO5_IO[9]	SOC-R6
123	LD	LCD_DATA12	Must be left floating	GPIO3_IO[17]	SOC-C12
123	No LD	LCD_DATA12		GPIO3_IO[17]	SOC-C12
124	LD	LCD_DATA20	Must be left floating	GPIO3_IO[25]	SOC-C14
124	No LD	LCD_DATA20		GPIO3_IO[25]	SOC-C14
125	LD	LCD_DATA13	Must be left floating	GPIO3_IO[18]	SOC-B12
125	No LD	LCD_DATA13		GPIO3_IO[18]	SOC-B12
126		DGND			
127	LD	LCD_DATA14	Must be left floating	GPIO3_IO[19]	SOC-A12
127	No LD	LCD_DATA14		GPIO3_IO[19]	SOC-A12
128	eMMC	NAND_READY_B		GPIO4_IO[12]	SOC-A3
128	NAND	NC			
129	LD	LCD_DATA15	Must be left floating	GPIO3_IO[20]	SOC-D13
129	No LD	LCD_DATA15		GPIO3_IO[20]	SOC-D13
130		USB_OTG1_CHD_B			SOC-U16
131	LD	LCD_DATA18	Must be left floating	GPIO3_IO[23]	SOC-A13
131	No LD	LCD_DATA18		GPIO3_IO[23]	SOC-A13
132		DGND			
133	LD	LCD_DATA19	Must be left floating	GPIO3_IO[24]	SOC-D14
133	No LD	LCD_DATA19		GPIO3_IO[24]	SOC-D14
134	eMMC	NAND_DQS		GPIO4_IO[16]	SOC-E6
134	NAND	NC		GPIO4_IO[16]	
135	LD	LCD_DATA22	Must be left floating	GPIO3_IO[27]	SOC-A14
135	No LD	LCD_DATA22		GPIO3_IO[27]	SOC-A14
136		ONOFF			SOC-R8
137	LD	LCD_DATA23	Must be left floating	GPIO3_IO[28]	SOC-B16
137	No LD	LCD_DATA23		GPIO3_IO[28]	SOC-B16
138		DGND			
139		DGND			
140		PMIC_STBY_REQ			SOC-U9
141		LCD_DATA8		GPIO3_IO[13]	SOC-B11
142		PMIC_ON_REQ			
143		LCD_DATA9		GPIO3_IO[14]	SOC-A11
144		DGND			
145		LCD_RESET		GPIO3_IO[4]	SOC-E9
146	EC	ETH1_TX_CLK		GPIO2_IO[6]	SOC-F14
146	No EC	ETH1_TX_CLK		GPIO2_IO[6]	SOC-F14

Pin #	Assembly	Pin Name	Notes	GPIO	Ball
147	LD	LCD_CLK	Must be left floating	GPIO3_IO[0]	SOC-A8
147	No LD	LCD_CLK		GPIO3_IO[0]	SOC-A8
148	EC	ETH1_TX_EN	Must be left floating	GPIO2_IO[5]	SOC-F15
148	No EC	ETH1_TX_EN		GPIO2_IO[5]	SOC-F15
149		DGND			
150	EC	ETH1_TDATA0	Must be left floating	GPIO2_IO[3]	SOC-E15
150	No EC	ETH1_TDATA0		GPIO2_IO[3]	SOC-E15
151	EC	ETH1_RX_EN	Must be left floating	GPIO2_IO[2]	SOC-E16
151	No EC	ETH1_RX_EN		GPIO2_IO[2]	SOC-E16
152	EC	ETH1_TDATA1	Must be left floating	GPIO2_IO[4]	SOC-E14
152	No EC	ETH1_TDATA1		GPIO2_IO[4]	SOC-E14
153	EC	ETH1_RX_ER	Must be left floating	GPIO2_IO[7]	SOC-D15
153	No EC	ETH1_RX_ER		GPIO2_IO[7]	SOC-D15
154	LD	LCD_DATA10	Must be left floating	GPIO3_IO[15]	SOC-E12
154	No LD	LCD_DATA10		GPIO3_IO[15]	SOC-E12
155	EC	ETH1_RDATA0	Must be left floating	GPIO2_IO[0]	SOC-F16
155	No EC	ETH1_RDATA0		GPIO2_IO[0]	SOC-F16
156		NC			
157	EC	ETH1_RDATA1	Must be left floating	GPIO2_IO[1]	SOC-E17
157	No EC	ETH1_RDATA1		GPIO2_IO[1]	SOC-E17
158		DGND			
159		DGND			
160	LD	LVDS_TX1_N			SN75LVDS83BDGG
160	No LD	NC			
161	LD	LVDS_TX0_N			SN75LVDS83BDGG
161	No LD	NC			
162	LD	LVDS_TX1_P			SN75LVDS83BDGG
162	No LD	NC			
163	LD	LVDS_TX0_P			SN75LVDS83BDGG
163	No LD	NC			
164	LD	LVDS_TX2_N			SN75LVDS83BDGG
164	No LD	NC			
165	LD	LCD_HSYNC	Must be left floating	GPIO3_IO[2]	SOC-D9
165	No LD	LCD_HSYNC		GPIO3_IO[2]	SOC-D9
166	LD	LVDS_TX2_P			SN75LVDS83BDGG
166	No LD	NC			
167	LD	LCD_VSYNC	Must be left floating	GPIO3_IO[3]	SOC-C9

Pin #	Assembly	Pin Name	Notes	GPIO	Ball
167	No LD	LCD_VSYNC		GPIO3_IO[3]	SOC-C9
168	LD	LVDS_CLK_N			SN75LVDS83BDGG
168	No LD	NC			
169		DGND			
170	LD	LVDS_CLK_P			SN75LVDS83BDGG
170	No LD	NC			
171		LCD_DATA16		GPIO3_IO[21]	SOC-C13
172		DGND			
173	LD	LCD_DATA5	Must be left floating	GPIO3_IO[10]	SOC-B10
173	No LD	LCD_DATA5		GPIO3_IO[10]	SOC-B10
174		I2C4_SCL		GPIO2_IO[10]	SOC-B17
175	LD	LCD_DATA21	Must be left floating	GPIO3_IO[26]	SOC-B14
175	No LD	LCD_DATA21		GPIO3_IO[26]	SOC-B14
176		I2C4_SDA		GPIO2_IO[11]	SOC-A15
177		GPIO5_8		GPIO5_IO[8]	SOC-N9
178		DGND			
179		DGND			
180		CCM_CLK1_N			SOC-P16
181		LCD_ENABLE		GPIO3_IO[1]	SOC-B8
182		CCM_CLK1_P			SOC-P17
183		NC			
184		NC			
185		DGND			
186		NC			
187	TP	GPIO1_3		GPIO1_IO[3]	SOC-L17
188		NC			
189		GPIO1_4		GPIO1_IO[4]	SOC-M16
190		NC			
191		GPIO1_2		GPIO1_IO[2]	SOC-L14
192		NC			
193		GPIO1_1		GPIO1_IO[1]	SOC-L15
194		NC			
195		AGND			
196	AC	NC			
196	No AC	SAI2_TX_SYNC-1		GPIO1_IO[12]	SOC-N15
197	AC	LLINEIN			WM8731L-24
197	No AC	SAI2_TX_BCLK-1		GPIO1_IO[13]	SOC-N16

Pin #	Assembly	Pin Name	Notes	GPIO	Ball
198	AC	HPLOUT			WM8731L-13
198	No AC	SAI2_RX_DATA		GPIO1_IO[14]	SOC-M14
199	AC	RLINEIN			WM8731L-23
199	No AC	SAI2_TX_SYNC-2		GPIO1_IO[12]	SOC-N15
200	AC	HPROUT			WM8731L-14
200	No AC	SAI2_TX_BCLK-2		GPIO1_IO[13]	SOC-N16

7.4 VAR-SOM-6UL Connector Pin Mux

Table 3: VAR-SOM-6UL Pin Mux

Pin	Assy	Ball	Alt 0	Alt 1	Alt 2	Alt 3	Alt 4	Alt 5	Alt 6	Alt 7	Alt 8
17		M17	ANATOP_ENET_REF_CLK2	PWM4_OUT	ANATOP_OTG2_ID	CSI_FIELD	USDHC1_VSELECT	GPIO1_IO[5]	ENET2_1588_EVENT0_OUT	CCM_PLL3_BYP	UART5_RX
18	No AC	N14	TRSTB	GPT2_COMPARE3	SAI2_TX_DATA	CCM_OUT2	PWM8_OUT	GPIO1_IO[15]	ANATOP_24M_OUT		CAAM_WRAPPER_RNG_OSC_OBS
20	No AC	P14	TMS	GPT2_CAPTURE1	SAI2_MCLK	CCM_CLKO1	CCM_WAIT	GPIO1_IO[11]	SDMA_EXT_EVENT[1]		EPIT1_OUT
21		D2	CSI_DATA[8]	USDHC2_DATA6	SIM2_PORT1_SVEN	ECSPI1_MOSI	WEIM_AD[6]	GPIO4_IO[27]	SAI1_RX_DATA	TPSMP_HDATA[30]	USDHC1_RESET
22		E1	CSI_DATA[5]	USDHC2_DATA3	SIM2_PORT1_PD	ECSPI2_MISO	WEIM_AD[3]	GPIO4_IO[24]	SAI1_RX_BCLK	TPSMP_HDATA[27]	UART5_CTS
23		E2	CSI_DATA[4]	USDHC2_DATA2	SIM1_PORT1_TRXD	ECSPI2_MOSI	WEIM_AD[2]	GPIO4_IO[23]	SAI1_RX_SYNC	TPSMP_HDATA[26]	UART5_RTS
24		D4	CSI_DATA[6]	USDHC2_DATA4	SIM2_PORT1_CLK	ECSPI1_SCLK	WEIM_AD[4]	GPIO4_IO[25]	SAI1_TX_SYNC	TPSMP_HDATA[28]	USDHC1_WP
25		D3	CSI_DATA[7]	USDHC2_DATA5	SIM2_PORT1_RST	ECSPI1_SS0	WEIM_AD[5]	GPIO4_IO[26]	SAI1_TX_BCLK	TPSMP_HDATA[29]	USDHC1_CD
26		D1	CSI_DATA[9]	USDHC2_DATA7	SIM2_PORT1_TRXD	ECSPI1_MISO	WEIM_AD[7]	GPIO4_IO[28]	SAI1_TX_DATA	TPSMP_HDATA[31]	USDHC1_VSELECT
29		P15	MOD	GPT2_CLK	SPDIF_OUT	ANATOP_ENET_REF_CLK_25M	CCM_PMIC_RDY	GPIO1_IO[10]	SDMA_EXT_EVENT[0]		
30		K17	ENET1_MDIO	ENET2_MDIO	USB_OTG_PWR_WAKE	CSI_MCLK	USDHC2_WP	GPIO1_IO[6]	CCM_WAIT	CCM_REF_EN	UART1_CTS
39		D16	ENET2_RX_ER	UART8_RTS	SIM2_PORT0_SVEN	ECSPI4_SS0	WEIM_ADDR[25]	GPIO2_IO[15]	KPP_COL[7]	SIM_M_HADDR[22]	GLOBAL WDOG
41		D17	ENET2_TX_CLK	UART8_CTS	SIM2_PORT0_RST	ECSPI4_MISO	ANATOP_ENET_REF_CLK2	GPIO2_IO[14]	KPP_ROW[7]	SIM_M_HADDR[21]	ANATOP_OTG2_ID
43		A16	ENET2_TDATA[1]	UART8_TX	SIM2_PORT0_TRXD	ECSPI4_SCLK	WEIM_EB[3]	GPIO2_IO[12]	KPP_ROW[6]	SIM_M_HADDR[19]	USB_OTG2_PWR
44		H15	UART3_CTS	ENET2_RX_CLK	CAN1_TX	CSI_DATA[10]	ENET1_1588_EVENT1_IN	GPIO1_IO[26]	ANATOP_USBPHY1_TSTI_TX_HIZ	SIM_M_HADDR[1]	EPIT2_OUT
45		B15	ENET2_TX_EN	UART8_RX	SIM2_PORT0_CLK	ECSPI4_MOSI	WEIM_ACLK_FREERUN	GPIO2_IO[13]	KPP_COL[6]	SIM_M_HADDR[20]	USB_OTG2_OC
46		G14	UART3_RTS	ENET2_TX_ER	CAN1_RX	CSI_DATA[11]	ENET1_1588_EVENT1_OUT	GPIO1_IO[27]	ANATOP_USBPHY2_TSTO_RX_HS_RXD	SIM_M_HADDR[2]	WDOG1_WDOG
48		H16	UART3_RX	ENET2_RDATA[3]	SIM2_PORT0_PD	CSI_DATA[0]	UART2_RTS	GPIO1_IO[25]	ANATOP_USBPHY1_TSTI_TX_EN	SIM_M_HADDR[0]	EPIT1_OUT
50		J15	UART2_CTS	ENET1_CRS	CAN2_TX	CSI_DATA[8]	GPT1_COMPARE2	GPIO1_IO[22]	ANATOP_USBPHY2_TSTO_RX_FS_RXD	DE	ECSPI3_MOSI
51		H14	UART2_RTS	ENET1_COL	CAN2_RX	CSI_DATA[9]	GPT1_COMPARE3	GPIO1_IO[23]	ANATOP_USBPHY1_TSTO_RX_FS_RXD	FAIL	ECSPI3_MISO

Pin	Assy	Ball	Alt 0	Alt 1	Alt 2	Alt 3	Alt 4	Alt 5	Alt 6	Alt 7	Alt 8
52		J17	UART2_TX	ENET1_TDATA[2]	I2C4_SCL	CSI_DATA[6]	GPT1_CAPTURE1	GPIO1_IO[20]	ANATOP_USBPHY1_TSTO_RX_DISCON_DET	RAWNAND_TESTER_TRIGGER	ECSPI3_SS0
53		J16	UART2_RX	ENET1_TDATA[3]	I2C4_SDA	CSI_DATA[7]	GPT1_CAPTURE2	GPIO1_IO[21]	ANATOP_USBPHY1_TSTO_RX_HS_RXD	DONE	ECSPI3_SCLK
54		E3	CSI_DATA[3]	USDHC2_DATA1	SIM1_PORT1_SVEN	ECSPI2_SS0	WEIM_AD[1]	GPIO4_IO[22]	SAI1_MCLK	TPSMP_HDATA[25]	UART5_RX
55		M15	PWM2_OUT	GLOBAL WDOG	SPDIF_IN	CSI_HSYNC	USDHC2_RESET	GPIO1_IO[9]	USDHC1_RESET	ECSPI3_TESTER_TRIGGER	UART5_CTS
56		E4	CSI_DATA[2]	USDHC2_DATA0	SIM1_PORT1_RST	ECSPI2_SCLK	WEIM_AD[0]	GPIO4_IO[21]	INT_BOOT	TPSMP_HDATA[24]	UART5_TX
57		N17	PWM1_OUT	WDOG1_WDOG	SPDIF_OUT	CSI_VSYNC	USDHC2_VSELECT	GPIO1_IO[8]	CCM_PMIC_RDY	ECSPI2_TESTER_TRIGGER	UART5_RTS
60		C1	USDHC1_CLK	GPT2_COMPARE2	SAI2_MCLK	SPDIF_IN	WEIM_ADDR[20]	GPIO2_IO[17]	CCM_OUT0	OBSERVE_MUX_OUT[0]	USB_OTG1_OC
61		B1	USDHC1_DATA2	GPT2_CAPTURE1	SAI2_RX_DATA	CAN2_TX	WEIM_ADDR[23]	GPIO2_IO[20]	CCM_CLKO1	OBSERVE_MUX_OUT[3]	USB_OTG2_OC
62		B3	USDHC1_DATA0	GPT2_COMPARE3	SAI2_TX_SYNC	CAN1_TX	WEIM_ADDR[21]	GPIO2_IO[18]	CCM_OUT1	OBSERVE_MUX_OUT[1]	ANATOP_OTG1_ID
63		B2	USDHC1_DATA1	GPT2_CLK	SAI2_TX_BCLK	CAN1_RX	WEIM_ADDR[22]	GPIO2_IO[19]	CCM_OUT2	OBSERVE_MUX_OUT[2]	USB_OTG2_PWR
64		C2	USDHC1_CMD	GPT2_COMPARE1	SAI2_RX_SYNC	SPDIF_OUT	WEIM_ADDR[19]	GPIO2_IO[16]	SDMA_EXT_EVENT[0]	TPSMP_HDATA[18]	USB_OTG1_PWR
65		A2	USDHC1_DATA3	GPT2_CAPTURE2	SAI2_TX_DATA	CAN2_RX	WEIM_ADDR[24]	GPIO2_IO[21]	CCM_CLKO2	OBSERVE_MUX_OUT[4]	ANATOP_OTG2_ID
68		A9	LCD_DATA[1]	PWM2_OUT	CA7_PLATFORM_TRACE[1]	ENET1_1588_EVENT2_OUT	I2C3_SCL	GPIO3_IO[6]	BT_CFG[1]	SIM_M_HADDR[29]	SAI1_TX_SYNC
69		B9	LCD_DATA[0]	PWM1_OUT	CA7_PLATFORM_TRACE[0]	ENET1_1588_EVENT2_IN	I2C3_SDA	GPIO3_IO[5]	BT_CFG[0]	SIM_M_HADDR[28]	SAI1_MCLK
70		F17	UART5_TX	ENET2_CRS	~~I2C2_SCL~~	CSI_DATA[14]	CSU_CSU_ALARM_AUT[0]	GPIO1_IO[30]	ANATOP_USBPHY2_TSTO_RX_SQUELCH	SIM_M_HADDR[5]	ECSPI2_MOSI
71		B5	RAWNAND_CE1	USDHC1_DATA6	QSPIA_DATA[2]	ECSPI3_MOSI	WEIM_ADDR[18]	GPIO4_IO[14]	ANATOP_TESTO[14]	TPSMP_HDATA[16]	UART3_CTS
72		P10	TAMPER[3]					GPIO5_IO[3]			
73		R9	TAMPER[1]					GPIO5_IO[1]			
74		L16	ENET1_MDC	ENET2_MDC	USB_OTG_HOST_MODE	CSI_PIXCLK	USDHC2_CD	GPIO1_IO[7]	CCM_STOP	ECSPI1_TESTER_TRIGGER	UART1_RTS
75		G17	UART4_TX	ENET2_TDATA[2]	I2C1_SCL	CSI_DATA[12]	CSU_CSU_ALARM_AUT[2]	GPIO1_IO[28]	ANATOP_USBPHY1_TSTO_PLL_CLK20DIV	SIM_M_HADDR[3]	ECSPI2_SCLK
77		G13	UART5_RX	ENET2_COL	~~I2C2_SDA~~	CSI_DATA[15]	CSU_CSU_INT_DEB	GPIO1_IO[31]	ANATOP_USBPHY2_TSTO_RX_DISCON_DET	SIM_M_HADDR[6]	ECSPI2_MISO
79		G16	UART4_RX	ENET2_TDATA[3]	I2C1_SDA	CSI_DATA[13]	CSU_CSU_ALARM_AUT[1]	GPIO1_IO[29]	ANATOP_USBPHY2_TSTO_PLL_CLK20DIV	SIM_M_HADDR[4]	ECSPI2_SS0
80		K13	~~I2C2_SCL~~	GPT1_CAPTURE1	ANATOP_OTG1_ID	ANATOP_ENET_REF_CLK1	MQS_RIGHT	GPIO1_IO[0]	ENET1_1588_EVENT0_IN	SYSTEM_RESET	WDOG3_WDOG

Pin	Assy	Ball	Alt 0	Alt 1	Alt 2	Alt 3	Alt 4	Alt 5	Alt 6	Alt 7	Alt 8
81		N10	TAMPER[7]					GPIO5_IO[7]			
82	No LD	D12	LCD_DATA[11]	SAI3_RX_BCLK	CA7_PLATFORM_TRACE[11]	CSI_DATA[19]	WEIM_DATA[3]	GPIO3_IO[16]	BT_CFG[11]	SIM_M_HPROT[3]	CAN2_RX
83		K16	UART1_RX	ENET1_RDATA[3]	I2C3_SDA	CSI_DATA[3]	GPT1_CLK	GPIO1_IO[17]	ANATOP_USBPHY1_TSTI_TX_HS_MODE	USDHC1_TESTER_TRIGGER	SPDIF_IN
84		J14	UART1_RTS	ENET1_TX_ER	USDHC1_CD	CSI_DATA[5]	ENET2_1588_EVENT1_OUT	GPIO1_IO[19]	ANATOP_USBPHY1_TSTO_RX_SQUELCH	QSPI_TESTER_TRIGGER	USDHC2_CD
85		K14	UART1_TX	ENET1_RDATA[2]	I2C3_SCL	CSI_DATA[2]	GPT1_COMPARE1	GPIO1_IO[16]	ANATOP_USBPHY1_TSTI_TX_LS_MODE	ECSPI4_TESTER_TRIGGER	SPDIF_OUT
86		K15	UART1_CTS	ENET1_RX_CLK	USDHC1_WP	CSI_DATA[4]	ENET2_1588_EVENT1_IN	GPIO1_IO[18]	ANATOP_USBPHY1_TSTI_TX_DN	USDHC2_TESTER_TRIGGER	USDHC2_WP
87		F5	CSI_MCLK	USDHC2_CD	RAWNAND_CE2	I2C1_SDA	WEIM_CS0	GPIO4_IO[17]	SNVS_HP_WRAPPER_VIO_5_CTL	TPSMP_HDATA[20]	UART6_TX
88		E5	CSI_PIXCLK	USDHC2_WP	RAWNAND_CE3	I2C1_SCL	WEIM_OE	GPIO4_IO[18]	SNVS_HP_WRAPPER_VIO_5	TPSMP_HDATA[21]	UART6_RX
90		C16	ENET2_RDATA[1]	UART6_RX	SIM1_PORT0_CLK	I2C3_SDA	ENET1_MDC	GPIO2_IO[9]	KPP_COL[4]	SIM_M_HADDR[16]	USB_OTG1_OC
91		U10	BOOT_MODE[1]					GPIO5_IO[11]			
92		C17	ENET2_RDATA[0]	UART6_TX	SIM1_PORT0_TRXD	I2C3_SCL	ENET1_MDIO	GPIO2_IO[8]	KPP_ROW[4]	SIM_M_HADDR[15]	USB_OTG1_PWR
93		T10	BOOT_MODE[0]					GPIO5_IO[10]			
94		H17	UART3_TX	ENET2_RDATA[2]	SIM1_PORT0_PD	CSI_DATA[1]	UART2_CTS	GPIO1_IO[24]	ANATOP_USBPHY1_TSTI_TX_DP	JTAG_ACT	ANATOP_OTG1_ID
96	No LD	A10	LCD_DATA[6]	UART7_CTS	CA7_PLATFORM_TRACE[6]	ENET2_1588_EVENT3_IN	SPDIF_LOCK	GPIO3_IO[11]	BT_CFG[6]	SIM_M_HBURST[2]	ECSPI1_SS2
100	eMMC	A4	RAWNAND_CLE	USDHC1_DATA7	QSPIA_DATA[3]	ECSPI3_MISO	WEIM_ADDR[16]	GPIO4_IO[15]	ANATOP_TESTO[15]	TPSMP_HDATA[19]	UART3_RTS
102	eMMC	D5	RAWNAND_WP	USDHC1_RESET	QSPIA_SCLK	PWM4_OUT	WEIM_BCLK	GPIO4_IO[11]	ANATOP_TESTO[11]	TPSMP_HDATA[13]	ECSPI3_RDY
113	No LD	D11	LCD_DATA[7]	UART7_RTS	CA7_PLATFORM_TRACE[7]	ENET2_1588_EVENT3_OUT	SPDIF_EXT_CLK	GPIO3_IO[12]	BT_CFG[7]	SIM_M_HMASTLOCK	ECSPI1_SS3
115		B13	LCD_DATA[17]	UART7_RX	CA7_PLATFORM_TRACE_CTL	CSI_DATA[0]	WEIM_DATA[9]	GPIO3_IO[22]	BT_CFG[25]	SIM_M_HWRITE	USDHC2_DATA7
117	No LD	C10	LCD_DATA[4]	UART8_CTS	CA7_PLATFORM_TRACE[4]	ENET2_1588_EVENT2_IN	SPDIF_SR_CLK	GPIO3_IO[9]	BT_CFG[4]	SIM_M_HBURST[0]	SAI1_TX_DATA
119	No LD	E10	LCD_DATA[2]	PWM3_OUT	CA7_PLATFORM_TRACE[2]	ENET1_1588_EVENT3_IN	I2C4_SDA	GPIO3_IO[7]	BT_CFG[2]	SIM_M_HADDR[30]	SAI1_TX_BCLK
120		N8	TAMPER[5]					GPIO5_IO[5]			
121	No LD	D10	LCD_DATA[3]	PWM4_OUT	CA7_PLATFORM_TRACE[3]	ENET1_1588_EVENT3_OUT	I2C4_SCL	GPIO3_IO[8]	BT_CFG[3]	SIM_M_HADDR[31]	SAI1_RX_DATA
122		R6	TAMPER[9]					GPIO5_IO[9]			

Pin	Assy	Ball	Alt 0	Alt 1	Alt 2	Alt 3	Alt 4	Alt 5	Alt 6	Alt 7	Alt 8
123	No LD	C12	LCD_DATA[12]	SAI3_TX_SYNC	CA7_PLATFORM_TRACE[12]	CSI_DATA[20]	WEIM_DATA[4]	GPIO3_IO[17]	BT_CFG[12]	SIM_M_HREADYOUT	ECSPI1_RDY
124	No LD	C14	LCD_DATA[20]	UART8_TX	ECSPI1_SCLK	CSI_DATA[12]	WEIM_DATA[12]	GPIO3_IO[25]	BT_CFG[28]	TPSMP_HTRANS[0]	USDHC2_DATA0
125	No LD	B12	LCD_DATA[13]	SAI3_TX_BCLK	CA7_PLATFORM_TRACE[13]	CSI_DATA[21]	WEIM_DATA[5]	GPIO3_IO[18]	BT_CFG[13]	SIM_M_HRESP	USDHC2_RESET
127	No LD	A12	LCD_DATA[14]	SAI3_RX_DATA	CA7_PLATFORM_TRACE[14]	CSI_DATA[22]	WEIM_DATA[6]	GPIO3_IO[19]	BT_CFG[14]	SIM_M_HSIZE[0]	USDHC2_DATA4
128	eMMC	A3	RAWNAND_READY	USDHC1_DATA4	QSPIA_DATA[0]	ECSPI3_SS0	WEIM_CS1	GPIO4_IO[12]	ANATOP_TESTO[12]	TPSMP_HDATA[14]	UART3_TX
129	No LD	D13	LCD_DATA[15]	SAI3_TX_DATA	CA7_PLATFORM_TRACE[15]	CSI_DATA[23]	WEIM_DATA[7]	GPIO3_IO[20]	BT_CFG[15]	SIM_M_HSIZE[1]	USDHC2_DATA5
131	No LD	A13	LCD_DATA[18]	PWM5_OUT	CA7_PLATFORM_EVENTO	CSI_DATA[10]	WEIM_DATA[10]	GPIO3_IO[23]	BT_CFG[26]	TPSMP_CLK	USDHC2_CMD
133	No LD	D14	LCD_DATA[19]	PWM6_OUT	GLOBAL WDOG	CSI_DATA[11]	WEIM_DATA[11]	GPIO3_IO[24]	BT_CFG[27]	TPSMP_HDATA_DIR	USDHC2_CLK
134	eMMC	E6	RAWNAND_DQS	CSI_FIELD	QSPIA_SS0	PWM5_OUT	WEIM_WAIT	GPIO4_IO[16]	SDMA_EXT_EVENT[1]	TPSMP_HDATA[17]	SPDIF_EXT_CLK
135	No LD	A14	LCD_DATA[22]	MQS_RIGHT	ECSPI1_MOSI	CSI_DATA[14]	WEIM_DATA[14]	GPIO3_IO[27]	BT_CFG[30]	TPSMP_HDATA[0]	USDHC2_DATA2
137	No LD	B16	LCD_DATA[23]	MQS_LEFT	ECSPI1_MISO	CSI_DATA[15]	WEIM_DATA[15]	GPIO3_IO[28]	BT_CFG[31]	TPSMP_HDATA[1]	USDHC2_DATA3
141		B11	LCD_DATA[8]	SPDIF_IN	CA7_PLATFORM_TRACE[8]	CSI_DATA[16]	WEIM_DATA[0]	GPIO3_IO[13]	BT_CFG[8]	SIM_M_HPROT[0]	CAN1_TX
143		A11	LCD_DATA[9]	SAI3_MCLK	CA7_PLATFORM_TRACE[9]	CSI_DATA[17]	WEIM_DATA[1]	GPIO3_IO[14]	BT_CFG[9]	SIM_M_HPROT[1]	CAN1_RX
145		E9	LCD_RESET	LCD_CS	CA7_PLATFORM_EVENTI	SAI3_TX_DATA	GLOBAL WDOG	GPIO3_IO[4]	ANATOP_TESTI[3]	SIM_M_HADDR[27]	ECSPI2_SS3
146	No EC	F14	ENET1_TX_CLK	UART7_CTS	PWM7_OUT	CSI_DATA[22]	ANATOP_ENET_REF_CLK1	GPIO2_IO[6]	KPP_ROW[3]	SIM_M_HADDR[13]	GPT1_CLK
147	No LD	A8	LCD_CLK	LCD_WR_RWN	UART4_TX	SAI3_MCLK	WEIM_CS2	GPIO3_IO[0]	OCOTP_CTRL_WRAPPER_FUSE_LATCHED	SIM_M_HADDR[23]	WDOG1_WDOG_RST_DEB
148	No EC	F15	ENET1_TX_EN	UART6_RTS	PWM6_OUT	CSI_DATA[21]	ENET2_MDC	GPIO2_IO[5]	KPP_COL[2]	SIM_M_HADDR[12]	WDOG2_WDOG_RST_DEB
150	No EC	E15	ENET1_TDATA[0]	UART5_CTS	ANATOP_24M_OUT	CSI_DATA[19]	CAN2_RX	GPIO2_IO[3]	KPP_COL[1]	SIM_M_HADDR[10]	USDHC2_VSELECT
151	No EC	E16	ENET1_RX_EN	UART5_RTS	OSC32K_32K_OUT	CSI_DATA[18]	CAN2_TX	GPIO2_IO[2]	KPP_ROW[1]	SIM_M_HADDR[9]	USDHC1_VSELECT
152	No EC	E14	ENET1_TDATA[1]	UART6_CTS	PWM5_OUT	CSI_DATA[20]	ENET2_MDIO	GPIO2_IO[4]	KPP_ROW[2]	SIM_M_HADDR[11]	WDOG1_WDOG_RST_DEB
153	No EC	D15	ENET1_RX_ER	UART7_RTS	PWM8_OUT	CSI_DATA[23]	WEIM_CRE	GPIO2_IO[7]	KPP_COL[3]	SIM_M_HADDR[14]	GPT1_CAPTURE2
154	No LD	E12	LCD_DATA[10]	SAI3_RX_SYNC	CA7_PLATFORM_TRACE[10]	CSI_DATA[18]	WEIM_DATA[2]	GPIO3_IO[15]	BT_CFG[10]	SIM_M_HPROT[2]	CAN2_TX
155	No EC	F16	ENET1_RDATA[0]	UART4_RTS	PWM1_OUT	CSI_DATA[16]	CAN1_TX	GPIO2_IO[0]	KPP_ROW[0]	SIM_M_HADDR[7]	USDHC1_LCTL

Pin	Assy	Ball	Alt 0	Alt 1	Alt 2	Alt 3	Alt 4	Alt 5	Alt 6	Alt 7	Alt 8
157	No EC	E17	ENET1_RDATA[1]	UART4_CTS	PWM2_OUT	CSI_DATA[17]	CAN1_RX	GPIO2_IO[1]	KPP_COL[0]	SIM_M_HADDR[8]	USDHC2_LCTL
165	No LD	D9	LCD_HSYNC	LCD_RS	UART4_CTS	SAI3_TX_BCLK	WDOG3_WDOG_RST_DEB	GPIO3_IO[2]	ANATOP_TESTI[1]	SIM_M_HADDR[25]	ECSPI2_SS1
167	No LD	C9	LCD_VSYNC	LCD_BUSY	UART4_RTS	SAI3_RX_DATA	WDOG2_WDOG	GPIO3_IO[3]	ANATOP_TESTI[2]	SIM_M_HADDR[26]	ECSPI2_SS2
171		C13	LCD_DATA[16]	UART7_TX	CA7_PLATFORM_TRACE_CLK	CSI_DATA[1]	WEIM_DATA[8]	GPIO3_IO[21]	BT_CFG[24]	SIM_M_HSIZE[2]	USDHC2_DATA6
173	No LD	B10	LCD_DATA[5]	UART8_RTS	CA7_PLATFORM_TRACE[5]	ENET2_1588_EVENT2_OUT	SPDIF_OUT	GPIO3_IO[10]	BT_CFG[5]	SIM_M_HBURST[1]	ECSPI1_SS1
174		B17	ENET2_RX_EN	UART7_TX	SIM1_PORT0_RST	I2C4_SCL	WEIM_ADDR[26]	GPIO2_IO[10]	KPP_ROW[5]	SIM_M_HADDR[17]	ANATOP_ENET_REF_CLK_25M
175	No LD	B14	LCD_DATA[21]	UART8_RX	ECSPI1_SS0	CSI_DATA[13]	WEIM_DATA[13]	GPIO3_IO[26]	BT_CFG[29]	TPSMP_HTRANS[1]	USDHC2_DATA1
176		A15	ENET2_TDATA[0]	UART7_RX	SIM1_PORT0_SVEN	I2C4_SDA	WEIM_EB[2]	GPIO2_IO[11]	KPP_COL[5]	SIM_M_HADDR[18]	ANATOP_24M_OUT
177		N9	TAMPER[8]					GPIO5_IO[8]			
181		B8	LCD_ENABLE	LCD_RD_E	UART4_RX	SAI3_TX_SYNC	WEIM_CS3	GPIO3_IO[1]	ANATOP_TESTI[0]	SIM_M_HADDR[24]	ECSPI2_RDY
187	TP	L17	I2C1_SDA	GPT1_COMPARE3	USB_OTG2_OC	OSC32K_32K_OUT	USDHC1_CD	GPIO1_IO[3]	CCM_DI0_EXT_CLK	TESTER_ACK	UART1_RX
189		M16	ANATOP_ENET_REF_CLK1	PWM3_OUT	USB_OTG1_PWR	ANATOP_24M_OUT	USDHC1_RESET	GPIO1_IO[4]	ENET2_1588_EVENT0_IN	CCM_PLL2_BYP	UART5_TX
191		L14	I2C1_SCL	GPT1_COMPARE2	USB_OTG2_PWR	ANATOP_ENET_REF_CLK_25M	USDHC1_WP	GPIO1_IO[2]	SDMA_EXT_EVENT[0]	ANY_PU_RESET	UART1_TX
193		L15	~~I2C2_SDA~~	GPT1_COMPARE1	USB_OTG1_OC	ANATOP_ENET_REF_CLK2	MQS_LEFT	GPIO1_IO[1]	ENET1_1588_EVENT0_OUT	EARLY_RESET	WDOG1_WDOG
196	No AC	N15	TDO	GPT2_CAPTURE2	SAI2_TX_SYNC	CCM_CLKO2	CCM_STOP	GPIO1_IO[12]	MQS_RIGHT		EPIT2_OUT
197	No AC	N16	TDI	GPT2_COMPARE1	SAI2_TX_BCLK	CCM_OUT0	PWM6_OUT	GPIO1_IO[13]	MQS_LEFT		SIM1_POWER_FAIL
198	No AC	M14	TCK	GPT2_COMPARE2	SAI2_RX_DATA	CCM_OUT1	PWM7_OUT	GPIO1_IO[14]	OSC32K_32K_OUT		SIM2_POWER_FAIL
199	No AC	N15	TDO	GPT2_CAPTURE2	SAI2_TX_SYNC	CCM_CLKO2	CCM_STOP	GPIO1_IO[12]	MQS_RIGHT		EPIT2_OUT
200	No AC	N16	TDI	GPT2_COMPARE1	SAI2_TX_BCLK	CCM_OUT0	PWM6_OUT	GPIO1_IO[13]	MQS_LEFT		SIM1_POWER_FAIL

8. SOM's interfaces

Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 4: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
Differential signals including: Ethernet, PCIe clocks, MIPI (CSI and DSI), LVDS lines	100 Ω Differential
USB Differential signals	90 Ω Differential

8.1 Display Interfaces

8.1.1 LVDS

- LVDS supports the following features:
  - 3-lane LVDS Interface
  - Support display resolutions up to 1366 x 768 @ 60fps, 18bpp
  - Synchronization and control capabilities

Table 5: LVDS Signals

Pin #	Assy	PIN Function
168	LD	LVDS_CLK_N
170	LD	LVDS_CLK_P
161	LD	LVDS_TX0_N
163	LD	LVDS_TX0_P
160	LD	LVDS_TX1_N
162	LD	LVDS_TX1_P
164	LD	LVDS_TX2_N
166	LD	LVDS_TX2_P

8.1.2 Parallel LCD

The SOM exposes one 24bit LCD interface with the following capabilities:

- Bus master interface to source frame buffer data for display refresh and a DMA interface to manage input data transfers from the LCD requiring minimal CPU overhead.
- 8/16/18/24-bit LCD data bus support available depending on I/O mux options.
- Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
- ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation

Table 6: Parallel LCD Signals

Pin #	Assy	PIN Function	Notes	Ball
147	No LD	LCD_CLK	Must be left floating if LVDS bridge assembled	A8
69		LCD_DATA[0]		B9
68		LCD_DATA[1]		A9
119	No LD	LCD_DATA[2]	Must be left floating if LVDS bridge assembled	E10
121	No LD	LCD_DATA[3]	Must be left floating if LVDS bridge assembled	D10
117	No LD	LCD_DATA[4]	Must be left floating if LVDS bridge assembled	C10
173	No LD	LCD_DATA[5]	Must be left floating if LVDS bridge assembled	B10
96	No LD	LCD_DATA[6]	Must be left floating if LVDS bridge assembled	A10
113	No LD	LCD_DATA[7]	Must be left floating if LVDS bridge assembled	D11
141		LCD_DATA[8]		B11
143		LCD_DATA[9]		A11
154	No LD	LCD_DATA[10]	Must be left floating if LVDS bridge assembled	E12
82	No LD	LCD_DATA[11]	Must be left floating if LVDS bridge assembled	D12
123	No LD	LCD_DATA[12]	Must be left floating if LVDS bridge assembled	C12
125	No LD	LCD_DATA[13]	Must be left floating if LVDS bridge assembled	B12
127	No LD	LCD_DATA[14]	Must be left floating if LVDS bridge assembled	A12
129	No LD	LCD_DATA[15]	Must be left floating if LVDS bridge assembled	D13
171		LCD_DATA[16]		C13
115		LCD_DATA[17]		B13
131	No LD	LCD_DATA[18]	Must be left floating if LVDS bridge assembled	A13
133	No LD	LCD_DATA[19]	Must be left floating if LVDS bridge assembled	D14
124	No LD	LCD_DATA[20]	Must be left floating if LVDS bridge assembled	C14
175	No LD	LCD_DATA[21]	Must be left floating if LVDS bridge assembled	B14
135	No LD	LCD_DATA[22]	Must be left floating if LVDS bridge assembled	A14
137	No LD	LCD_DATA[23]	Must be left floating if LVDS bridge assembled	B16
181		LCD_ENABLE		B8

Pin #	Assy	PIN Function	Notes	Ball
165	No LD	LCD_HSYNC	Must be left floating if LVDS bridge assembled	D9
145		LCD_RESET		E9
167	No LD	LCD_VSYNC	Must be left floating if LVDS bridge assembled	C9

8.1.3 EPDC

The SOM exposes The EPDC is a feature-rich, low power and high-performance direct drive active matrix EPD controller. It is specifically designed to drive E-INK EPD panels supporting a wide variety of TFT backplanes.

Key features of the EPDC are as follows:

- TFT resolutions up to 4096 x 4096 pixels with 20 Hz refresh (programmable up to 8191 x 8191)
- TFT resolutions up to 1650 x 2332 pixels at 106 Hz refresh
- Industry standard bus interfaces (AMBA AXI and APB)
- Up to 5-bit pixel representation for up to 32 greyscale levels

Table 7: EPDC Signals

Pin	Assembly	PIN Function	Notes	Ball
147	No LD	EPDC_SDCLK	Positive Source Driver-Shift Clock	A8
125	No LD	EPDC_BDR[0]	Panel-Border Control	B12
131	No LD	EPDC_BDR[1]	Panel-Border Control	A13
171		EPDC_GDCLK	Gate Driver-Clock	C13
145		EPDC_GDOE	Gate Driver-Output Enable	E9
129	No LD	EPDC_GDRL	Gate Driver-Shift direction	D13
115		EPDC_GDSP	Gate Driver-Start Pulse	B13
154	No LD	EPDC_PWRCOM	Panel-Power control	E12
123	No LD	EPDC_PWRCTRL[0]	Panel-Power control	C12
79		EPDC_PWRCTRL[1]	Panel-Power control	G16
141		EPDC_PWRIRQ	Panel-Power irq	B11
82	No LD	EPDC_PWRSTAT	Panel-Power status good	D12
143		EPDC_PWRWAKE	Panel-Power control wake signal	A11
167	No LD	EPDC_SDCE[0]	Source Driver-Chip-enable/StartPulse	C9
175	No LD	EPDC_SDCE[1]	Source Driver-Chip-enable/StartPulse	B14
135	No LD	EPDC_SDCE[2]	Source Driver-Chip-enable/StartPulse	A14
137	No LD	EPDC_SDCE[3]	Source Driver-Chip-enable/StartPulse	B16
155	No EC	EPDC_SDCE[4]	Source Driver-Chip-enable/StartPulse	F16
157	No EC	EPDC_SDCE[5]	Source Driver-Chip-enable/StartPulse	E17

Pin	Assembly	PIN Function	Notes	Ball
151	No EC	EPDC_SDCE[6]	Source Driver-Chip-enable/StartPulse	E16
150	No EC	EPDC_SDCE[7]	Source Driver-Chip-enable/StartPulse	E15
152	No EC	EPDC_SDCE[8]	Source Driver-Chip-enable/StartPulse	E14
148	No EC	EPDC_SDCE[9]	Source Driver-Chip-enable/StartPulse	F15
69		EPDC_SDDO[0]	Source Driver-Shift signal	B9
68		EPDC_SDDO[1]	Source Driver-Shift signal	A9
174		EPDC_SDDO[10]	Source Driver-Shift signal	B17
176		EPDC_SDDO[11]	Source Driver-Shift signal	A15
43		EPDC_SDDO[12]	Source Driver-Shift signal	A16
45		EPDC_SDDO[13]	Source Driver-Shift signal	B15
41		EPDC_SDDO[14]	Source Driver-Shift signal	D17
39		EPDC_SDDO[15]	Source Driver-Shift signal	D16
119	No LD	EPDC_SDDO[2]	Source Driver-Shift signal	E10
121	No LD	EPDC_SDDO[3]	Source Driver-Shift signal	D10
117	No LD	EPDC_SDDO[4]	Source Driver-Shift signal	C10
173	No LD	EPDC_SDDO[5]	Source Driver-Shift signal	B10
96	No LD	EPDC_SDDO[6]	Source Driver-Shift signal	A10
113	No LD	EPDC_SDDO[7]	Source Driver-Shift signal	D11
92		EPDC_SDDO[8]	Source Driver-Shift signal	C17
90		EPDC_SDDO[9]	Source Driver-Shift signal	C16
181		EPDC_SDLE	Source Driver-Latch Enable	B8
165	No LD	EPDC_SDOE	Source Driver-Output Enable	D9
146	No EC	EPDC_SDOED	Source Driver-Output Enable (to VDD)	F14
153	No EC	EPDC_SDOEZ	Source Driver-Output Enable (to Zero)	D15
127	No LD	EPDC_SDSHR	Source Driver-Shift dir	A12
133	No LD	EPDC_VCOM[0]	Panel-VCOM	D14
124	No LD	EPDC_VCOM[1]	Panel-VCOM	C14

Note: The EPDC interface is available in iMX6ULL based SOMs only.

8.2 Audio

8.2.1 Synchronous Audio Interface (SAI)

The SOM exposes 3 Synchronous Audio Interfaces, one of them used internally by audio codec or/and by Bluetooth Audio. SAI2 is used by Audio Codec SAI1 is not accessible and is used only on SoMs that does not have analog audio interface.

- Transmitter with independent Bit Clock and Frame Sync supporting 1 data line
- Receiver with independent Bit Clock and Frame Sync supporting 1 data line
- Maximum Frame Size of 32 Words
- Word size programmable from 8-bits to 32-bits
- Word size configured separately for first word and remaining words in frame.
- Asynchronous FIFO for each Transmit and Receive data line
- Graceful restart after FIFO Error

Table 8: SAI Signals

Pin	Assembly	PIN Function	Notes	Ball
54		SAI1_MCLK		E3
69		SAI1_MCLK		B9
22		SAI1_RX_BCLK		E1
21		SAI1_RX_DATA		D2
121	No LD	SAI1_RX_DATA		D10
23		SAI1_RX_SYNC		E2
25		SAI1_TX_BCLK		D3
119	No LD	SAI1_TX_BCLK		E10
26		SAI1_TX_DATA		D1
117	No LD	SAI1_TX_DATA		C10
24		SAI1_TX_SYNC		D4
68		SAI1_TX_SYNC		A9
20	No AC	SAI2_MCLK		P14
60		SAI2_MCLK		C1
61		SAI2_RX_DATA		B1
198	No AC	SAI2_RX_DATA		M14
64		SAI2_RX_SYNC		C2
63		SAI2_TX_BCLK		B2
197	No AC	SAI2_TX_BCLK		N16
200	No AC	SAI2_TX_BCLK		N16
18	No AC	SAI2_TX_DATA		N14
65		SAI2_TX_DATA		A2
62		SAI2_TX_SYNC		B3
196	No AC	SAI2_TX_SYNC		N15

Pin	Assembly	PIN Function	Notes	Ball
199	No AC	SAI2_TX_SYNC		N15
147	No LD	SAI3_MCLK		A8
143		SAI3_MCLK		A11
82	No LD	SAI3_RX_BCLK		D12
127	No LD	SAI3_RX_DATA		A12
167	No LD	SAI3_RX_DATA		C9
154	No LD	SAI3_RX_SYNC		E12
125	No LD	SAI3_TX_BCLK		B12
165	No LD	SAI3_TX_BCLK		D9
129	No LD	SAI3_TX_DATA		D13
145		SAI3_TX_DATA		E9
123	No LD	SAI3_TX_SYNC		C12
181		SAI3_TX_SYNC		B8

8.2.2 Analog Audio Interface

The SOM exposes 1 Stereo Line In input and 1 Stereo Headphone Interface. Audio is provided via WM8731L audio codec.

Table 9: Analog Audio Signals

Pin	Assembly	PIN Function	Notes	Ball
195		AGND		
197	AC	LLINEIN		WM8731L-24
198	AC	HPLOUT		WM8731L-13
199	AC	RLINEIN		WM8731L-23
200	AC	HPROUT		WM8731L-14

8.2.3 Sony/Philips Digital Interface (SPDIF)

The SOM exposes 1 SPDIF interface.

Table 10: SPDIF Signals

Pin	Assembly	PIN Function	Notes	Ball
134	eMMC	SPDIF_EXT_CLK		E6
113	No LD	SPDIF_EXT_CLK		D11
55		SPDIF_IN		M15
83		SPDIF_IN		K16
141		SPDIF_IN		B11
60		SPDIF_IN		C1
96	No LD	SPDIF_LOCK		A10
29		SPDIF_OUT		P15
57		SPDIF_OUT		N17
85		SPDIF_OUT		K14
173	No LD	SPDIF_OUT		B10
64		SPDIF_OUT		C2
117	No LD	SPDIF_SR_CLK		C10

8.3 Wi-Fi and Bluetooth Interface

The SOM contains a certified high-performance Wi-Fi and Bluetooth module.
For Single band assembly option: IEEE 802.11 b/g/n + Bluetooth 2.1+EDR, and BLE 5.1
For Dual band assembly option: IEEE 802.11 ac/a/b/g/n + Bluetooth 2.1+EDR, and BLE 5.2
The modules have an antenna connection through a U.FL JACK connector.
Antenna cable connected to module must have 50-Ω impedance.
In order to give the most flexible solution the Bluetooth UART bus is buffered and it can be disconnected from the module and used by external circuity.

One of the following options can be implemented:

- The system will use all the wireless interfaces: Wi-Fi and Bluetooth. In this case all the external pins of the interfaces should be left floating.
- The system will use only Wi-Fi; the Bluetooth interface will not be used. In this case The Bluetooth should be disabled; the Bluetooth module pins will be entering Hi-Z and the SOC pins will be accessible.

The Wi-Fi module connected to the i.MX6 Ultralight processor via SD1 SD Card interface. The second available interface is used by the SOM for the internal boot and storage. The SD card interface SD1 is mixed and routed to the external connector and the Wi-Fi module to allow SD Card recovery and to ease the development process. This means that booting from the SD card must be done with the kernel that does not have W-Fi module definitions inside i.e. Wi-Fi interface is not accessible when booting from SD card.
The SOM can be ordered without Wi-Fi module assembled and, in this case, the SD1 interface is directly routed to the SOM connector. In this case the routing does not pass the mixer chip and the pins can be used for other interfaces.

8.4 USB ports

The USB controller block provides high performance USB functionality that conforms to the Universal Serial Bus Specification, Rev. 2.0 (Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, Philips; 2000), and the On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification (Hewlett-Packard Company, Intel Corporation, LSI Corporation, Microsoft Corporation, Renesas Electronics Corporation, ST-Ericsson; 2012).
The USB controller consists of two independent USB controller cores: two On-The-Go (OTG) controller cores. Each controller core supports UTMI interface. See Features for more details. All two controller cores are single-port cores. For the OTG cores, there is only one port. The port can be used as either a downstream or an upstream port.

Table 11: USB Signals

Pin	Assembly	PIN Function	Notes	Ball
130		USB_OTG1_CHD_B		SOC-U16
94		OTG1_ID		
114		USB_OTG1_DN		SOC-T15
116		USB_OTG1_DP		SOC-U15
106		USB_OTG1_VBUS		SOC-T12
108		USB_OTG2_DN		SOC-T13
110		USB_OTG2_DP		SOC-U13
104		USB_OTG2_VBUS		SOC-U12

8.5 UART Interfaces

The SOM exposes up to 8 UART interfaces that are mixed with other peripherals. Part of them is used on the SOM and can be accessible only in subset versions of the SOM.

Universal Asynchronous Receiver/Transmitter (UART) provides serial communication capability with external devices through a level converter and an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility. UART supports NRZ encoding format, RS485 compatible 9 bit data format and IrDA compatible infrared slow data rate (SIR) format.

UART2 is in use by BT module, in order to use it the BT interface should be disabled or the SOM should be ordered without Wi-Fi module.

Table 12: UART Signals

Pin	Assembly	PIN Function	Notes	Ball
30		UART1_CTS		K17
86		UART1_CTS		K15
74		UART1_RTS		L16
84		UART1_RTS		J14
83		UART1_RX		K16
187	TP	UART1_RX		L17
85		UART1_TX		K14
191		UART1_TX		L14
50		UART2_CTS	Used by Bluetooth	J15
94		UART2_CTS	Used by Bluetooth	H17
48		UART2_RTS	Used by Bluetooth	H16
51		UART2_RTS	Used by Bluetooth	H14
53		UART2_RX	Used by Bluetooth	J16
52		UART2_TX	Used by Bluetooth	J17
44		UART3_CTS		H15
71		UART3_CTS		B5
100	eMMC	UART3_RTS		A4
46		UART3_RTS		G14
48		UART3_RX		H16
128	eMMC	UART3_TX		A3
94		UART3_TX		H17
157	No EC	UART4_CTS		E17
165	No LD	UART4_CTS		D9

Pin	Assembly	PIN Function	Notes	Ball
155	No EC	UART4_RTS		F16
167	No LD	UART4_RTS		C9
79		UART4_RX		G16
181		UART4_RX		B8
147	No LD	UART4_TX		A8
75		UART4_TX		G17
150	No EC	UART5_CTS		E15
22		UART5_CTS		E1
55		UART5_CTS		M15
151	No EC	UART5_RTS		E16
23		UART5_RTS		E2
57		UART5_RTS		N17
17		UART5_RX		M17
54		UART5_RX		E3
77		UART5_RX		G13
56		UART5_TX		E4
70		UART5_TX		F17
189		UART5_TX		M16
152	No EC	UART6_CTS		E14
148	No EC	UART6_RTS		F15
88		UART6_RX		E5
90		UART6_RX		C16
87		UART6_TX		F5
92		UART6_TX		C17
146	No EC	UART7_CTS		F14
96	No LD	UART7_CTS		A10
153	No EC	UART7_RTS		D15
113	No LD	UART7_RTS		D11
115		UART7_RX		B13
176		UART7_RX		A15
171		UART7_TX		C13
174		UART7_TX		B17
117	No LD	UART8_CTS		C10
41		UART8_CTS		D17
173	No LD	UART8_RTS		B10
39		UART8_RTS		D16
175	No LD	UART8_RX		B14

Pin	Assembly	PIN Function	Notes	Ball
45		UART8_RX		B15
124	No LD	UART8_TX		C14
43		UART8_TX		A16

8.6 I2C Interface

The SOM exposes 3 I2C interfaces on the external connectors.
I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

I2C2 is in use internally for DDR calibration values and control of the Audio Codec. It cannot be used.

Table 13: I2C Signals

Pin	Assembly	PIN Function	Notes	Ball
75		I2C1_SCL		G17
88		I2C1_SCL		E5
191		I2C1_SCL		L14
79		I2C1_SDA		G16
87		I2C1_SDA		F5
187	TP	I2C1_SDA		L17
85		I2C3_SCL		K14
92		I2C3_SCL		C17
68		I2C3_SCL		A9
83		I2C3_SDA		K16
90		I2C3_SDA		C16
69		I2C3_SDA		B9
52		I2C4_SCL		J17
174		I2C4_SCL		B17
121	No LD	I2C4_SCL		D10
53		I2C4_SDA		J16
176		I2C4_SDA		A15
119	No LD	I2C4_SDA		E10

8.7 Flexible Controller Area Network (FLEXCAN)

The SOM Exposes 2 FLEXCAN interfaces.
The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported.

Table 14: FLEXCAN Signals

Pin	Assembly	PIN Function	Notes	Ball
46		CAN1_RX		G14
157	No EC	CAN1_RX		E17
63		CAN1_RX		B2
143		CAN1_RX		A11
44		CAN1_TX		H15
155	No EC	CAN1_TX		F16
141		CAN1_TX		B11
62		CAN1_TX		B3
51		CAN2_RX		H14
150	No EC	CAN2_RX		E15
65		CAN2_RX		A2
82	No LD	CAN2_RX		D12
50		CAN2_TX		J15
151	No EC	CAN2_TX		E16
61		CAN2_TX		B1
154	No LD	CAN2_TX		E12

8.8 10/100-Mbps Ethernet MAC (ENET)

The SOM implements a dual speed 10/100 Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. SOM contains on board Ethernet 10/100 PHY based on KSZ8081RNB chip. This PHY is assembled on ETH1 interface.
When adding second Ethernet interface to the SOM the pins 30 and 74 should be used as MDIO bus.

Table 15: ENET Signals

Pin	Assembly	PIN Function	Notes	Ball
29		ANATOP_ENET_REF_CLK_25M		P15
191		ANATOP_ENET_REF_CLK_25M		L14
174		ANATOP_ENET_REF_CLK_25M		B17
146	No EC	ANATOP_ENET_REF_CLK1		F14
80		ANATOP_ENET_REF_CLK1		K13
189		ANATOP_ENET_REF_CLK1		M16
41		ANATOP_ENET_REF_CLK2		D17
193		ANATOP_ENET_REF_CLK2		L15
17		ANATOP_ENET_REF_CLK2		M17
80		ENET1_1588_EVENT0_IN		K13
193		ENET1_1588_EVENT0_OUT		L15
44		ENET1_1588_EVENT1_IN		H15
46		ENET1_1588_EVENT1_OUT		G14
69		ENET1_1588_EVENT2_IN		B9
68		ENET1_1588_EVENT2_OUT		A9
119	No LD	ENET1_1588_EVENT3_IN		E10
121	No LD	ENET1_1588_EVENT3_OUT		D10
51		ENET1_COL		H14
50		ENET1_CRS		J15
74		ENET1_MDC		L16
90		ENET1_MDC		C16
30		ENET1_MDIO		K17
92		ENET1_MDIO		C17
155	No EC	ENET1_RDATA[0]		F16
157	No EC	ENET1_RDATA[1]		E17
85		ENET1_RDATA[2]		K14
83		ENET1_RDATA[3]		K16
86		ENET1_RX_CLK		K15
151	No EC	ENET1_RX_EN		E16
153	No EC	ENET1_RX_ER		D15

Pin	Assembly	PIN Function	Notes	Ball
150	No EC	ENET1_TDATA[0]		E15
152	No EC	ENET1_TDATA[1]		E14
52		ENET1_TDATA[2]		J17
53		ENET1_TDATA[3]		J16
146	No EC	ENET1_TX_CLK		F14
148	No EC	ENET1_TX_EN		F15
84		ENET1_TX_ER		J14
189		ENET2_1588_EVENT0_IN		M16
17		ENET2_1588_EVENT0_OUT		M17
86		ENET2_1588_EVENT1_IN		K15
84		ENET2_1588_EVENT1_OUT		J14
117	No LD	ENET2_1588_EVENT2_IN		C10
173	No LD	ENET2_1588_EVENT2_OUT		B10
96	No LD	ENET2_1588_EVENT3_IN		A10
113	No LD	ENET2_1588_EVENT3_OUT		D11
77		ENET2_COL		G13
70		ENET2_CRS		F17
74		ENET2_MDC	Internal MDIO bus	L16
148	No EC	ENET2_MDC		F15
30		ENET2_MDIO	Internal MDIO bus	K17
152	No EC	ENET2_MDIO		E14
92		ENET2_RDATA[0]		C17
90		ENET2_RDATA[1]		C16
94		ENET2_RDATA[2]		H17
48		ENET2_RDATA[3]		H16
44		ENET2_RX_CLK		H15
174		ENET2_RX_EN		B17
39		ENET2_RX_ER		D16
176		ENET2_TDATA[0]		A15
43		ENET2_TDATA[1]		A16
75		ENET2_TDATA[2]		G17
79		ENET2_TDATA[3]		G16
41		ENET2_TX_CLK		D17
45		ENET2_TX_EN		B15
46		ENET2_TX_ER		G14

8.9 Enhanced Configurable SPI (ECSPI)

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, Synchronous, four-wire serial communication block.
The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO). With data FIFOs, the ECSPI allows rapid data communication with fewer software interrupts.

Table 16: ECSPI Signals

Pin	Assembly	PIN Function	Notes	Ball
137	No LD	ECSPI1_MISO		B16
26		ECSPI1_MISO		D1
135	No LD	ECSPI1_MOSI		A14
21		ECSPI1_MOSI		D2
123	No LD	ECSPI1_RDY		C12
124	No LD	ECSPI1_SCLK		C14
24		ECSPI1_SCLK		D4
175	No LD	ECSPI1_SS0		B14
25		ECSPI1_SS0		D3
173	No LD	ECSPI1_SS1		B10
96	No LD	ECSPI1_SS2		A10
113	No LD	ECSPI1_SS3		D11
74		ECSPI1_TESTER_TRIGGER		L16
77		ECSPI2_MISO		G13
22		ECSPI2_MISO		E1
70		ECSPI2_MOSI		F17
23		ECSPI2_MOSI		E2
181		ECSPI2_RDY		B8
56		ECSPI2_SCLK		E4
75		ECSPI2_SCLK		G17
79		ECSPI2_SS0		G16
54		ECSPI2_SS0		E3
165	No LD	ECSPI2_SS1		D9
167	No LD	ECSPI2_SS2		C9
145		ECSPI2_SS3		E9
57		ECSPI2_TESTER_TRIGGER		N17
51		ECSPI3_MISO		H14
100	eMMC	ECSPI3_MISO		A4
50		ECSPI3_MOSI		J15
71		ECSPI3_MOSI		B5

Pin	Assembly	PIN Function	Notes	Ball
102	eMMC	ECSPI3_RDY		D5
53		ECSPI3_SCLK		J16
52		ECSPI3_SS0		J17
128	eMMC	ECSPI3_SS0		A3
55		ECSPI3_TESTER_TRIGGER		M15
41		ECSPI4_MISO		D17
45		ECSPI4_MOSI		B15
43		ECSPI4_SCLK		A16
39		ECSPI4_SS0		D16
85		ECSPI4_TESTER_TRIGGER		K14

8.10 Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) has a 16-bit counter, and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4 x 16 data FIFO.

Table 17: PWM Signals

Pin	Assembly	PIN Function	Notes	Ball
57		PWM1_OUT		N17
155	No EC	PWM1_OUT		F16
69		PWM1_OUT		B9
55		PWM2_OUT		M15
157	No EC	PWM2_OUT		E17
68		PWM2_OUT		A9
189		PWM3_OUT		M16
119	No LD	PWM3_OUT		E10
17		PWM4_OUT		M17
102	eMMC	PWM4_OUT		D5
121	No LD	PWM4_OUT		D10
131	No LD	PWM5_OUT		A13
134	eMMC	PWM5_OUT		E6
152	No EC	PWM5_OUT		E14
133	No LD	PWM6_OUT		D14
148	No EC	PWM6_OUT		F15
197	No AC	PWM6_OUT		N16
200	No AC	PWM6_OUT		N16
146	No EC	PWM7_OUT		F14
198	No AC	PWM7_OUT		M14
153	No EC	PWM8_OUT		D15
18	No AC	PWM8_OUT		N14

8.11 CMOS Sensor Interface (CSI)

The CSI enables the chip to connect directly to external CMOS image sensors. CMOS image sensors are separated into two classes, dumb and smart. Dumb sensors are those that support only traditional sensor timing (Vertical SYNC and Horizontal SYNC) and output only Bayer and statistics data, while smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats). The capabilities of the CSI include:

- Configurable interface logic to support most commonly available CMOS sensors.
- Support for CCIR656 video interface as well as traditional sensor interface.
- 8-bit / 24-bit data port for YCbCr, YUV, or RGB data input.
- 8-bit / 10-bit / 16-bit data port for Bayer data input.
- Full control of 8-bit/pixel, 10-bit/pixel or 16-bit / pixel data format to 32-bitreceive FIFO packing.
- 256 x 32 FIFO to store received image pixel data.
- Embedded DMA controllers to transfer data from receive FIFO or statistic FIFO through AHB bus.
- Support 2D DMA transfer from the receive FIFO to the frame buffers in the external memory.
- Support double buffering two frames in the external memory.
- Single interrupt source to interrupt controller from mask able interrupt sources: Start of Frame, End of Frame, Change of Field, FIFO full, FIFO overrun, DMA transfer done, CCIR error and AHB bus response error.
- Configurable master clock frequency output to sensor.

Table 18: Parallel CSI Signals

Pin	Assembly	PIN Function	Notes	Ball
48		CSI_DATA[0]		H16
115		CSI_DATA[0]		B13
94		CSI_DATA[1]		H17
171		CSI_DATA[1]		C13
56		CSI_DATA[2]		E4
85		CSI_DATA[2]		K14
83		CSI_DATA[3]		K16
54		CSI_DATA[3]		E3
86		CSI_DATA[4]		K15
23		CSI_DATA[4]		E2
84		CSI_DATA[5]		J14
22		CSI_DATA[5]		E1
52		CSI_DATA[6]		J17
24		CSI_DATA[6]		D4
53		CSI_DATA[7]		J16
25		CSI_DATA[7]		D3
50		CSI_DATA[8]		J15

Pin	Assembly	PIN Function	Notes	Ball
21		CSI_DATA[8]		D2
51		CSI_DATA[9]		H14
26		CSI_DATA[9]		D1
44		CSI_DATA[10]		H15
131	No LD	CSI_DATA[10]		A13
46		CSI_DATA[11]		G14
133	No LD	CSI_DATA[11]		D14
75		CSI_DATA[12]		G17
124	No LD	CSI_DATA[12]		C14
79		CSI_DATA[13]		G16
175	No LD	CSI_DATA[13]		B14
70		CSI_DATA[14]		F17
135	No LD	CSI_DATA[14]		A14
77		CSI_DATA[15]		G13
137	No LD	CSI_DATA[15]		B16
155	No EC	CSI_DATA[16]		F16
141		CSI_DATA[16]		B11
157	No EC	CSI_DATA[17]		E17
143		CSI_DATA[17]		A11
151	No EC	CSI_DATA[18]		E16
154	No LD	CSI_DATA[18]		E12
150	No EC	CSI_DATA[19]		E15
82	No LD	CSI_DATA[19]		D12
152	No EC	CSI_DATA[20]		E14
123	No LD	CSI_DATA[20]		C12
148	No EC	CSI_DATA[21]		F15
125	No LD	CSI_DATA[21]		B12
146	No EC	CSI_DATA[22]		F14
127	No LD	CSI_DATA[22]		A12
153	No EC	CSI_DATA[23]		D15
129	No LD	CSI_DATA[23]		D13
17		CSI_FIELD		M17
134	eMMC	CSI_FIELD		E6
55		CSI_HSYNC		M15
30		CSI_MCLK		K17
87		CSI_MCLK		F5
74		CSI_PIXCLK		L16

Pin	Assembly	PIN Function	Notes	Ball
88		CSI_PIXCLK		E5
57		CSI_VSYNC		N17

8.12 Analog to Digital Converter (ADC)

The analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within an integrated microcontroller system-on-chip.
The features of the ADC-Digital are as follows:

- Configuration registers
- 32-bit, word aligned, byte enabled registers. (Byte and Half word access is not supported)
- Linear successive approximation algorithm with up to 12-bit resolution with 10/11 bit accuracy.
- Up to 10 ENOB (dedicated Single Ended Channels)
- Up to 1MS/s sampling rate
- Up to 16 single-ended external analog inputs
- Single or continuous conversion (automatic return to idle after single conversion)
- Output Modes: (in right-justified unsigned format)
    - 12-bit
    - 10-bit
    - 8-bit
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Selectable voltage reference, Internal, External, or Alternate
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Operation in low power modes for lower noise operation
- Hardware average function
- Self-calibration mode

Table 19: ADC Signals

Pin	Assembly	PIN Function	Notes	Ball
80		GPIO1_IO[0]	Analog to Digital Converter 1 channel 0	K13
193		GPIO1_IO[1]	Analog to Digital Converter 1 channel 1	L15
191		GPIO1_IO[2]	Analog to Digital Converter 1 channel 2	L14
187	TP	GPIO1_IO[3]	Analog to Digital Converter 1 channel 3	L17
189		GPIO1_IO[4]	Analog to Digital Converter 1 channel 4	M16
17		GPIO1_IO[5]	Analog to Digital Converter 1 channel 5	M17
30		GPIO1_IO[6]	Analog to Digital Converter 1 channel 6	K17
74		GPIO1_IO[7]	Analog to Digital Converter 1 channel 7	L16
57		GPIO1_IO[8]	Analog to Digital Converter 1 channel 8	N17
55		GPIO1_IO[9]	Analog to Digital Converter 1 channel 9	M15
80		GPIO1_IO[0]	Analog to Digital Converter 2 channel 0	K13

Pin	Assembly	PIN Function	Notes	Ball
193		GPIO1_IO[1]	Analog to Digital Converter 2 channel 1	L15
191		GPIO1_IO[2]	Analog to Digital Converter 2 channel 2	L14
187	TP	GPIO1_IO[3]	Analog to Digital Converter 2 channel 3	L17
189		GPIO1_IO[4]	Analog to Digital Converter 2 channel 4	M16
17		GPIO1_IO[5]	Analog to Digital Converter 2 channel 5	M17
30		GPIO1_IO[6]	Analog to Digital Converter 2 channel 6	K17
74		GPIO1_IO[7]	Analog to Digital Converter 2 channel 7	L16
57		GPIO1_IO[8]	Analog to Digital Converter 2 channel 8	N17
55		GPIO1_IO[9]	Analog to Digital Converter 2 channel 9	M15

8.13 Touch Screen Controller (TSC)

TSC is responsible for providing control of ADC and touch screen analogue block to form a touch screen system, which achieves function of touch detection and touch location detection. The controller utilizes ADC hardware trigger function and control switches in touch screen analogue block. The controller only supports 4-wire of 5-wire screen touch modes.

Table 20: TSC Signals

Pin	Assembly	PIN Function	Notes	Ball
80		GPIO1_IO[0]	Wiper Touch Controller Input	K13
193		GPIO1_IO[1]	YNLR Touch Controller Input	L15
191		GPIO1_IO[2]	YPLL Touch Controller Input	L14
187	TP	GPIO1_IO[3]	XNUR Touch Controller Input	L17
189		GPIO1_IO[4]	XPUL Touch Controller Input	M16

8.14 SD Card (USDHC)

The SOM exposes up to two SDHC interfaces for connecting external SD Card.

8.14.1 USDHC1

USDHC1 is in use by Wi-Fi module (if available) in runtime so it cannot be used when wi-fi is active.
This interface can be used to boot from it and to update the internal storage.
This interface can be accessible in runtime when the Wi-Fi module is disabled.
To disable the Wi-Fi module GPIO5[6] should be set to low.

Table 21: USDHC1 Signals

Pin	Assembly	PIN Function	Notes	Ball
60		USDHC1_CLK	This line can be connected to Wi-Fi module via GPIO5[6]	C1
64		USDHC1_CMD	This line can be connected to Wi-Fi module via GPIO5[6]	C2
62		USDHC1_DATA0	This line can be connected to Wi-Fi module via GPIO5[6]	B3
63		USDHC1_DATA1	This line can be connected to Wi-Fi module via GPIO5[6]	B2
61		USDHC1_DATA2	This line can be connected to Wi-Fi module via GPIO5[6]	B1
65		USDHC1_DATA3	This line can be connected to Wi-Fi module via GPIO5[6]	A2
84		USDHC1_CD	This line is in use by Boot ROM and should be pulled low in order to boot from SD	J14

8.14.2 USDHC2

USDHC2 is in use by internal eMMC memory chip and it can be used only on SOMs with NAND chip assembled. This interface cannot be used as boot device.

Table 22: USDHC2 Signals

Pin	Assembly	PIN Function	Notes	Ball
74		USDHC2_CD		L16
84		USDHC2_CD		J14
87		USDHC2_CD		F5
133	No LD	USDHC2_CLK		D14
131	No LD	USDHC2_CMD		A13
56		USDHC2_DATA0		E4
124	No LD	USDHC2_DATA0		C14
175	No LD	USDHC2_DATA1		B14
54		USDHC2_DATA1		E3
135	No LD	USDHC2_DATA2		A14
23		USDHC2_DATA2		E2
137	No LD	USDHC2_DATA3		B16
22		USDHC2_DATA3		E1
24		USDHC2_DATA4		D4
127	No LD	USDHC2_DATA4		A12
25		USDHC2_DATA5		D3
129	No LD	USDHC2_DATA5		D13
171		USDHC2_DATA6		C13
21		USDHC2_DATA6		D2
115		USDHC2_DATA7		B13
26		USDHC2_DATA7		D1
157	No EC	USDHC2_LCTL		E17
55		USDHC2_RESET		M15
125	No LD	USDHC2_RESET		B12
86		USDHC2_TESTER_TRIGGER		K15
86		USDHC2_WP		K15
57		USDHC2_VSELECT		N17
150	No EC	USDHC2_VSELECT		E15
30		USDHC2_WP		K17
88		USDHC2_WP		E5

8.15 General Purpose Input Output (GPIO)

The GPIO general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.
When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CORE interrupts.

Table 23: GPIO Signals

Pin	Assembly	PIN Function	Notes	Ball
80		GPIO1_IO[0]		K13
193		GPIO1_IO[1]		L15
191		GPIO1_IO[2]		L14
187	TP	GPIO1_IO[3]		L17
189		GPIO1_IO[4]		M16
17		GPIO1_IO[5]		M17
30		GPIO1_IO[6]		K17
74		GPIO1_IO[7]		L16
57		GPIO1_IO[8]		N17
55		GPIO1_IO[9]		M15
29		GPIO1_IO[10]		P15
20	No AC	GPIO1_IO[11]		P14
196	No AC	GPIO1_IO[12]		N15
199	No AC	GPIO1_IO[12]		N15
197	No AC	GPIO1_IO[13]		N16
200	No AC	GPIO1_IO[13]		N16
198	No AC	GPIO1_IO[14]		M14
18	No AC	GPIO1_IO[15]		N14
85		GPIO1_IO[16]		K14
83		GPIO1_IO[17]		K16
86		GPIO1_IO[18]		K15
84		GPIO1_IO[19]		J14
52		GPIO1_IO[20]		J17
53		GPIO1_IO[21]		J16
50		GPIO1_IO[22]		J15
51		GPIO1_IO[23]		H14
94		GPIO1_IO[24]		H17
48		GPIO1_IO[25]		H16
44		GPIO1_IO[26]		H15

Pin	Assembly	PIN Function	Notes	Ball
46		GPIO1_IO[27]		G14
75		GPIO1_IO[28]		G17
79		GPIO1_IO[29]		G16
70		GPIO1_IO[30]		F17
77		GPIO1_IO[31]		G13
155	No EC	GPIO2_IO[0]		F16
157	No EC	GPIO2_IO[1]		E17
151	No EC	GPIO2_IO[2]		E16
150	No EC	GPIO2_IO[3]		E15
152	No EC	GPIO2_IO[4]		E14
148	No EC	GPIO2_IO[5]		F15
146	No EC	GPIO2_IO[6]		F14
153	No EC	GPIO2_IO[7]		D15
92		GPIO2_IO[8]		C17
90		GPIO2_IO[9]		C16
174		GPIO2_IO[10]		B17
176		GPIO2_IO[11]		A15
43		GPIO2_IO[12]		A16
45		GPIO2_IO[13]		B15
41		GPIO2_IO[14]		D17
39		GPIO2_IO[15]		D16
64		GPIO2_IO[16]		C2
60		GPIO2_IO[17]		C1
62		GPIO2_IO[18]		B3
63		GPIO2_IO[19]		B2
61		GPIO2_IO[20]		B1
65		GPIO2_IO[21]		A2
147	No LD	GPIO3_IO[0]		A8
181		GPIO3_IO[1]		B8
165	No LD	GPIO3_IO[2]		D9
167	No LD	GPIO3_IO[3]		C9
145		GPIO3_IO[4]		E9
69		GPIO3_IO[5]		B9
68		GPIO3_IO[6]		A9
119	No LD	GPIO3_IO[7]		E10
121	No LD	GPIO3_IO[8]		D10
117	No LD	GPIO3_IO[9]		C10

Pin	Assembly	PIN Function	Notes	Ball
173	No LD	GPIO3_IO[10]		B10
96	No LD	GPIO3_IO[11]		A10
113	No LD	GPIO3_IO[12]		D11
141		GPIO3_IO[13]		B11
143		GPIO3_IO[14]		A11
154	No LD	GPIO3_IO[15]		E12
82	No LD	GPIO3_IO[16]		D12
123	No LD	GPIO3_IO[17]		C12
125	No LD	GPIO3_IO[18]		B12
127	No LD	GPIO3_IO[19]		A12
129	No LD	GPIO3_IO[20]		D13
171		GPIO3_IO[21]		C13
115		GPIO3_IO[22]		B13
131	No LD	GPIO3_IO[23]		A13
133	No LD	GPIO3_IO[24]		D14
124	No LD	GPIO3_IO[25]		C14
175	No LD	GPIO3_IO[26]		B14
135	No LD	GPIO3_IO[27]		A14
137	No LD	GPIO3_IO[28]		B16
102	eMMC	GPIO4_IO[11]		D5
128	eMMC	GPIO4_IO[12]		A3
71		GPIO4_IO[14]		B5
100	eMMC	GPIO4_IO[15]		A4
134	eMMC	GPIO4_IO[16]		E6
87		GPIO4_IO[17]		F5
88		GPIO4_IO[18]		E5
56		GPIO4_IO[21]		E4
54		GPIO4_IO[22]		E3
23		GPIO4_IO[23]		E2
22		GPIO4_IO[24]		E1
24		GPIO4_IO[25]		D4
25		GPIO4_IO[26]		D3
21		GPIO4_IO[27]		D2
26		GPIO4_IO[28]		D1
73		GPIO5_IO[1]		R9
72		GPIO5_IO[3]		P10
120		GPIO5_IO[5]		N8

Pin	Assembly	PIN Function	Notes	Ball
81		GPIO5_IO[7]		N10
177		GPIO5_IO[8]		N9
122		GPIO5_IO[9]		R6
93		GPIO5_IO[10]		T10
91		GPIO5_IO[11]		U10

8.16 Power

The SOM gets its power from external 3.3VDC 2A power supply.

Table 24: Power Pins

Pin	Assembly	PIN Function	Notes	Ball
195		AGND		
1		DGND		
2		DGND		
7		DGND		
8		DGND		
13		DGND		
14		DGND		
19		DGND		
27		DGND		
28		DGND		
31		DGND		
33		DGND		
35		DGND		
37		DGND		
47		DGND		
58		DGND		
59		DGND		
66		DGND		
67		DGND		
76		DGND		
78		DGND		
89		DGND		
95		DGND		
101		DGND		
112		DGND		

Pin	Assembly	PIN Function	Notes	Ball
118		DGND		
126		DGND		
132		DGND		
138		DGND		
139		DGND		
144		DGND		
149		DGND		
158		DGND		
159		DGND		
169		DGND		
172		DGND		
178		DGND		
179		DGND		
185		DGND		
32		VCC_3V3_IN		
34		VCC_3V3_IN		
38		VCC_3V3_IN		
103		VCC_3V3_IN		
105		VCC_3V3_IN		
107		VCC_3V3_IN		
109		VCC_3V3_IN		
111		VCC_3V3_IN		

8.17 Control

The following control pins are exposed:

Table 25: Control Signals

Pin	PIN Function	Notes	Ball
49	VCC_3V3	Output. Goes high when the power to peripheral devices can be applied	
98	POR	Power on reset	SOC-P8
136	ONOFF	On-off pin	SOC-R8
36	VCC_COIN	Power of Tamper pins and internal RTC clock	SOC-P12

9. Boot Configuration

VAR-SOM-6UL can be programmed to boot from the following sources:

- Internal Boot
  - On board NAND Flash memory (if available)
  - On board eMMC Flash memory (if available)
- External Boot
  - External SD Card (using Wi-Fi SDHC Interface)

In order to be complied with other Variscite SOMs the selection of the boot mode is done internally on the SOM.
The only exposed pin for this purpose is Pin 42. Pulling it down will select External SD Card boot. Pulling it up or leaving it floating will select Internal Boot.

The SOC selection of the boot mode is done via strap options resistors on LCD_DATA lines.
In addition, Boot mode pins should be set to Internal Boot, BOOT_MODE[1:0]= 10.
Attention should be paid using these boot strap pins as inputs to the SOM. External drivers should be disabled in time of Reset otherwise, they may change the boot option and the SOM will not boot.

Table 26:Boot configuration pins

Pin#	PIN Function	Description	NAND	eMMC	SD Card
69	LCD_DATA[0]	Boot Configuration Byte 1 Bit 0	0	0	0
68	LCD_DATA[1]	Boot Configuration Byte 1 Bit 1	0	0	0
119	LCD_DATA[2]	Boot Configuration Byte 1 Bit 2	0	0	0
121	LCD_DATA[3]	Boot Configuration Byte 1 Bit 3	0	0	0
117	LCD_DATA[4]	Boot Configuration Byte 1 Bit 4	0	0	0
173	LCD_DATA[5]	Boot Configuration Byte 1 Bit 5	1	1	1
96	LCD_DATA[6]	Boot Configuration Byte 1 Bit 6	0	1	1
113	LCD_DATA[7]	Boot Configuration Byte 1 Bit 7	1	0	0
141	LCD_DATA[8]	Boot Configuration Byte 2 Bit 0	0	0	0
143	LCD_DATA[9]	Boot Configuration Byte 2 Bit 1	1	1	1
154	LCD_DATA[10]	Boot Configuration Byte 2 Bit 2	0	0	0
82	LCD_DATA[11]	Boot Configuration Byte 2 Bit 3	X	1	0
123	LCD_DATA[12]	Boot Configuration Byte 2 Bit 4	0	0	0
125	LCD_DATA[13]	Boot Configuration Byte 2 Bit 5	1	1	1
127	LCD_DATA[14]	Boot Configuration Byte 2 Bit 6	0	0	0
129	LCD_DATA[15]	Boot Configuration Byte 2 Bit 7	0	0	0
171	LCD_DATA[16]	Boot Configuration Byte 4 Bit 0	0	0	0
115	LCD_DATA[17]	Boot Configuration Byte 4 Bit 1	0	0	0
131	LCD_DATA[18]	Boot Configuration Byte 4 Bit 2	0	0	0
133	LCD_DATA[19]	Boot Configuration Byte 4 Bit 3	0	0	0

Pin#	PIN Function	Description	NAND	eMMC	SD Card
124	LCD_DATA[20]	Boot Configuration Byte 4 Bit 4	0	0	0
175	LCD_DATA[21]	Boot Configuration Byte 4 Bit 5	0	0	0
135	LCD_DATA[22]	Boot Configuration Byte 4 Bit 6	0	0	0
137	LCD_DATA[23]	Boot Configuration Byte 4 Bit 7	0	0	0
93	BOOT0	Boot mode bit 0 signal	0	0	0
91	BOOT1	Boot mode bit 1 signal	1	1	1

Note: “0” value in this table means the line is pulled low. “1” value in this table means the line is pulled high. The pull resistor can be SOC internal or placed externally on the SOM.

10. Compatible interfaces

The SOM was designed to be compatible to other Variscite SOMs as close as possible.
The following features of the SOM are compatible:

10.1 Ethernet

The SOM supports 10/100 Ethernet speeds while all other SOMs support 1000/100/10.
Connecting the following lines ensures the compatibility mode of 10/100.

Table 27: Ethernet compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
3	ETH_RXDP	V	V	V	V
5	ETH_RXDN	V	V	V	V
9	ETH_TXDP	V	V	V	V
11	ETH_TXDN	V	V	V	V
15	LINKSPEED	V	V	V	V
16	LINKLED	V	V	V	V

10.2 UART

10.2.1 UART 1

UART1 is used as Debug UART in Variscite Release.

Table 28: UART1 compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MXl
83	UART1_RX	V	V	V	V
84	UART1_RTS	V	V	V	V
85	UART1_TX	V	V	V	V
86	UART1_CTS	V	V	V	V

10.2.2 UART 2

UART2 is used by Wi-Fi module for Bluetooth. The BT should be disabled in order to use these pins.
To disable BT pull GPIO5[4] to a low state.

Table 29: UART2 compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
50	UART2_CTS	V	V	V	V
51	UART2_RTS	V	V	V	V
52	UART2_TX	V	V	V	V
53	UART2_RX	V	V	V	V

10.2.3 UART 5

Table 30: UART5 compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
54	UART5_RX	V	V	V	V
55	UART5_CTS	V	V	V	V
56	UART5_TX	V	V	V	V
57	UART5_RTS	V	V	V	V

10.3 I2C

10.3.1 I2C1

Table 31: I2C1 compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
87	I2C1_SDA	V	V	V	V
88	I2C1_SCL	V	V	V	V

10.3.2 I2C3

Table 32: I2C3 compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
90	I2C3_SDA	V	V	V	V
92	I2C3_SCL	V	V	V	V

10.3.3 I2C4

Table 33: I2C4 compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
174	I2C4_SCL	V	V	V	V
176	I2C4_SDA	V	V	V	V

10.4 SPI

10.4.1 ESPI2

Table 34: ESPI2 compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
70	ECSPI2_MOSI	X	X	V	V
75	ECSPI2_SCLK	V	V	V	V
77	ECSPI2_MISO	V	V	V	V
79	ECSPI2_SS0	V	V	V	V

10.4.2 ESPI4

Table 35: ESP42 compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
39	ECSPI4_SS0	V	V	V	V
41	ECSPI4_MISO	V	V	V	V
43	ECSPI4_SCLK	V	V	V	V
45	ECSPI4_MOSI	V	V	V	V

10.5 PWM

Table 36: PWM compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
69	PWM1_OUT	V	V	V	V
68	PWM2_OUT	V	V	V	V
17	PWM4_OUT	V	V	V	V

10.6 CAN

Table 37: CAN compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
44	CAN1_TX	V	V	V	V
46	CAN1_RX	V	V	V	V

10.7 Analog Audio

Table 38: Analog Audio compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
195	AGND	V	V	V	V
197	LLINEIN	V	V	V	V
198	HPLOUT	V	V	V	V
199	RLINEIN	V	V	V	V
200	HPROUT	V	V	V	V

10.8 Digital Audio

Table 39: SAI1 compatible pins

Pin	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
21	SAI1_RX_DATA	V	V	V	V
22	SAI1_RX_BCLK	V	V	V	V
23	SAI1_RX_SYNC	V	V	V	V
24	SAI1_TX_SYNC	V	V	V	V
25	SAI1_TX_BCLK	V	V	V	V
26	SAI1_TX_DATA	V	V	V	V

10.9 LVDS

LVDS interface is available only on SOMs with LD option selected
LVDS interface is limited to 1366 x 768 @ 60fps, 18bpp

Table 40: LVDS compatible pins

Pin #	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
168	LVDS_CLK_N	V	V	V	V
170	LVDS_CLK_P	V	V	V	V
161	LVDS_TX0_N	V	V	V	V
163	LVDS_TX0_P	V	V	V	V
160	LVDS_TX1_N	V	V	V	V
162	LVDS_TX1_P	V	V	V	V
164	LVDS_TX2_N	V	V	V	V
166	LVDS_TX2_P	V	V	V	V

10.10 SD Card

Table 41: USDHC1 compatible pins

Pin #	PIN Function	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
60	USDHC1_CLK	V	V	V	V
64	USDHC1_CMD	V	V	V	V
62	USDHC1_DATA0	V	V	V	V
63	USDHC1_DATA1	V	V	V	V
61	USDHC1_DATA2	V	V	V	V
65	USDHC1_DATA3	V	V	V	V
80	USDHC1_CD	V	V	V	V

10.11 USB

Table 42: USB compatible pins

94	OTG1_ID	VAR-SOM-SOLO	VAR-SOM-MX6	VAR-SOM-MX8	VAR-SOM-MX8X
114	USB_OTG1_DN	V	V	V	V
116	USB_OTG1_DP	V	V	V	V
106	USB_OTG1_VBUS	V	V	V	V
108	USB_OTG2_DN	V	V	V	V
110	USB_OTG2_DP	V	V	V	V
104	USB_OTG2_VBUS	V	V	V	V

10.12 Boot selects

Boot select pins is fully compatible with all other SOMs.

10.13 Power

Power pins are fully compatible with all other SOMs.

11. Assembly options

To make the solution as Flexible as possible the following assembly options were added. The assembly options help customers to order the SOM subversion that include only the needed interfaces with a lower cost.

11.1 Analog Audio Codec

The SOM can be ordered without Audio Codec chip assembled; it allows reducing the overall cost of the product in case the Analog Audio is not used.
When not assembled, the SoC balls which are normally connected to Codec are routed to SOM connector and exported on Analog codec interface pins.

Table 43: AC assembly options

Pin #	Default SOM option		Special SOM option	
	Pin name	Ball	Pin name	Ball
18	NC		SAI2_TX_DATA	SOC-N14
20	NC		SAI2_MCLK	SOC-P14
196	NC		SAI2_TX_SYNC-1	SOC-N15
197	LLINEIN	WM8731L-24	SAI2_TX_BCLK-1	SOC-N16
198	HPLOUT	WM8731L-13	SAI2_RX_DATA	SOC-M14
199	RLINEIN	WM8731L-23	SAI2_TX_SYNC-2	SOC-N15
200	HPROUT	WM8731L-14	SAI2_TX_BCLK-2	SOC-N16

11.2 Ethernet PHY0

The SOM can be ordered without Ethernet0 PHY chip assembled, it allows reducing the overall cost of the product in case the Ethernet Interfaces are not used.

11.3 DDR 3

The SOM can be ordered with different RAM size capacities, it allows reducing the overall cost of the product in case lower RAM size is sufficient.

11.4 eMMC

The SOM can be ordered with different eMMC size capacities, it allows reducing the overall cost of the product in case lower eMMC size is sufficient.

11.5 NAND

The SOM can be ordered with different NAND size capacities, it allows reducing the overall cost of the product in case lower storage size is sufficient.

12. Electrical specifications

12.1 Absolute maximum ratings

Table 44: Absolute Maximum Ratings

Parameter		Min	Max	Unit
VCC_3V3_IN	Main supply input voltage	-0.5	3.6	V
VCC_COIN	RTC supply input voltage	-0.5	3.6	V
USB_VBUS	USB_OTG1_VBUS, USB_OTG2_VBUS		5.5	V

12.2 Operating conditions

Table 45: Operating Ranges

Parameter		Min	Typ	Max	Unit
VCC_3V3_IN	Main supply input voltage	3.15	3.3	3.45	V
VCC_COIN	RTC supply input voltage	3.0	3.3	3.6	V
USB_VBUS	USB_OTG1_VBUS, USB_OTG2_VBUS	4.4	5.0	5.5	V

12.3 Power consumption

12.3.1 Single Band

Table 46: VAR-SOM-6UL Single Band Power Consumption

Mode	Voltage	Current	Power	Notes
Run	3.3V	350mA	1.15W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	3.3V	130mA	429mW	Linux up
Standby	3.3V	4.5mA	14.85mW	Memory retention mode
Off (RTC)	3.0V	120uA	360uW	Off mode, only RTC is powered
Recommended power supply rating	3.3V	1000mA	3.3W	Minimum Requirement for stable operation

Note: Although the Max continuous supply current to the LWB Wi-Fi module is < 300 mA, when providing power to the Wi-Fi module, a power source capable of supplying 600 mA peak current for a duration of ~20 msec is required by the Wi-Fi module

12.3.2 Dual Band

Table 45: VAR-SOM-6UL Dual Band Power Consumption

Mode	Voltage	Current	Power	Notes
Run	3.3V	422mA	1.39W	Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz
Run	3.3V	400mA	1.32W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	3.3V	148mA	488.4 mW	Linux up
Standby	3.3V	TBD	TBD	Memory retention mode
Off (RTC)	3.0V	120uA	360uW	Off mode, only RTC is powered
Recommended power supply rating	3.3V	1200mA	3.95W	Minimum Requirement for stable operation

Note: Although the Max continuous supply current to the LWB5 Wi-Fi module is < 320 mA, when providing power to the Wi-Fi module, a power source capable of supplying 750 mA peak current for a duration of ~20 msec is required by the Wi-Fi module

13. Environmental Specifications

Table 46: Environmental Specifications

	Min	Max
Commercial Operating Temperature Range	0 0C	+70 0C
Industrial Operating Temperature Range	-40C	+85 0C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Referring Telcordia Technologies Special Report SR-332, Issue 4 Reliability Prediction Method Model: 25Deg Celsius, Class B-1, GM	10296 Khrs >	
Shock Resistance	50G/20 ms	
Vibration	20G/0 - 600 Hz	

Note: Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

14. Mechanical Drawings

14.1 Carrier Board Mounting

The SOM has two mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

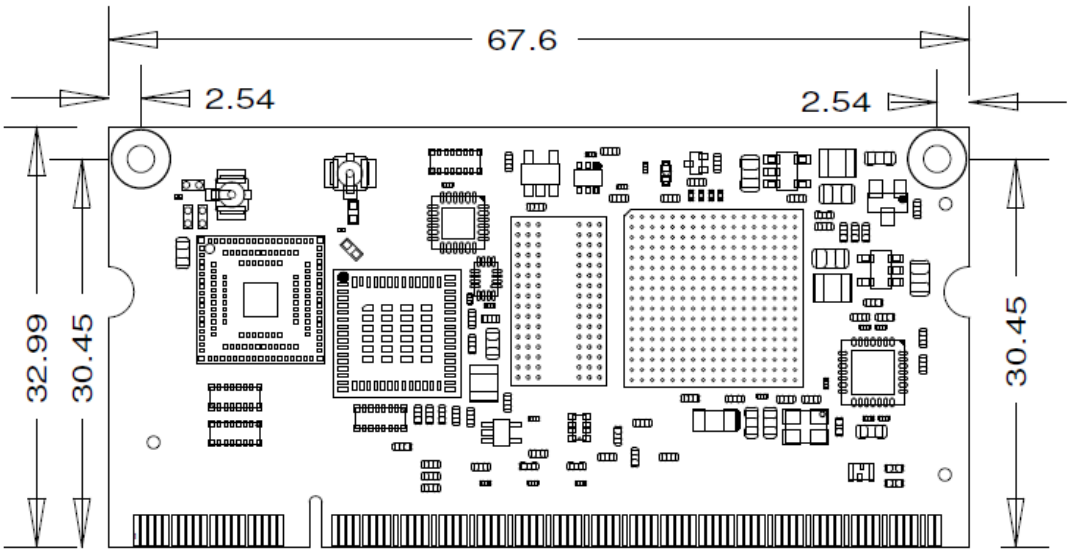
Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-3.0-M2-B**

14.2 SOM Dimensions

Figure 2: VAR-SOM-6UL Mechanics in millimeters



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