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5	Power, Reset, Boot, RTC, EEPROM
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Schematics are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.

Document	Carrier	
1.0	1.0	Initial
1.1	1.1	Released
1.2	1.1	Updated Block Diagrams
		Added SH1 were short symbol
		Updated Compatibility value for SOM pins 68,69,176
		Updated SOM pin 22 net name
		Fixed U2Z,B1, C113,1 net name
		Fixed R1-R2,R35-R38 net name
1.3	1.2	Removed SH1 wire short, J1_68 routed to capacitive touch Changed R29 to C185 Changed R123,R132 to N.C.
		Added resistors R138-152
		Removed AD_1Nux alternate function from VAR-SOM-MXMX Symbol
		Updated PCIe resistor assembly note
1.4	1.2	Updated Parallel Camera HDMI2P Note
1.5		Fixed ETH pin names VAR-SOM-MXMX Symbol
1.6	1.2A	Disconnected R129
1.6	1.2A	Added VAR-SOM-MXMX-MINI Block Diagram and Symbol
		PRE-RELEASE VERSION!!!! Subject to change without notice
1.7	1.2B	Fixed VAR-SOM-MXMX-MINI Symbol
		Changed U29,U30,U31 to P/N: FPF2193
		Changed R60 to 47k
1.8	1.2C	Update VAR-SOM-MXMX-MINI Symbol to V1.1 with side notes for v1.0B(Early access customers)
		Updated VAR-SOM-MXMX-MINI Block Diagram
		POR circuitry tied by VCC_50m; see U7 R60 R61 R60 R60 D5 Removed
1.9	1.2D	Raise VCC_3V3 to nominal 1.33V for VAR-SOM-MXMX-MINI/NANO power up threshold voltage requirement of >3.35V
1.10	1.2D	Reference for new designs: (changes not implemented in V1.2 BRD) Added x2 studs for heat plate support Base_per_3v3 added side note U7 (Base POR circuit) added CB_WD00 resistor assembly options U29 U30 U31 - Added assembly note VAR-SOM-MXMX-NANO pages updated with symbol pinout VAR-SOM-MXMX Connector update - added NC on P / assembly options Power switch in OFF position (no charge of Custom rails added) Ethernet magnetics - support two Manf: Pulse & UDE; Base R445 UDE matches VAR-SOM behaviour
1.11	1.3	Added VAR-SOM-MXMX-PLUS Preliminary Symbol and Block Diagram Symbol is Pre Release, Version! Subject to change without notice All C1210 capacitor footprints updated to C1210_0m *M51 to M56 not assembled
1.12	1.3A	ETH1 PHY clock filter U9 replaced with 49.5 Ohm /0603 resistor Added design notes for ETH1
1.13	1.4	* M55 and M56 location updated to heatplate design - Layout Update J1 Manufacturer PN, NAME and footprint to represent the assembled part Replace PCB AC0 capacitor with 0.01uF 0 ohm resistors Updated VAR-SOM-MXMX-PLUS Symbol pins 1 58 80, swap pins 41 43 and 84 147 J19 Modify Camera connector orientation Remove U8 U10 analog switches on ETH1 U9 revert to EMI filter on RGMII_RJ45 clock line Added RNT1 RNS RNS1 R151 R136 isolating stops on ETH1 RGMII signals U26 footprint updated to D5 Y1 C58 C67 updated * BOOT - Mode1 - R117 assembled * BOOT - Mode2 - Added P3 R149 USB6A PWR1 to HOST J23 always enabled * Remove R59 on pin J15 to identify symbol for VAR-SOM-MXMP 2nd MPI/CSI Lane2 routing J3 J30 pinout change
1.14	1.4A	* Support for VAR-SOM-MXMXMB USB OTG - Changed US P4 Pull for board identification, U21-9 connected to GPIO: - Changed R43,R130,R106 to N.C. - Changed R44,R132 to Assembled * Changed Q4 P/N from: TP2S7082L (EOL) to -> TP2S7081A * Updated VAR-SOM-MXMX-PLUS Block Diagram, Symbol pins 36,38 names * Added notes for SOM pins 29,79,84
1.15	1.4A	Changes in v1.141.44 for R43,R44 were not implemented (part of board identification) and only appear in revision history; board identification implemented via EEPROM U3. Board identification required for CS J23 to identify method of OTG to be used: P/N610 to GPIO
1.16	1.5	* Modified VCC_3V3 to 3.35V nominal for all SOMs. For VAR-SOM-MXMX-MINI/NANO, power up threshold voltage requirement of >3.35V is implemented using Q10,R152
1.17	1.5	* Added note for VAR-SOM-MXMX-MINI/NANO pin 91 * Updated note for I2C4B pull up resistors
1.18	1.5	* Updated note for PTFN6043BXY chip
1.19	1.5A	* Q10 changed to 2N7002P215 Transistor Q10 changed to 2N7002P to stabilize the SOM voltage in the OFF state Old transistor leakage current (IDG) changed the feedback current and increased the SOM voltage. 2N7002GP does not have SG diode that allowed IDGS to flow into the Gate * SOM Pin B4 Note changed
1.20	1.6	Ethernet PHY replaced to ADIN1300 R22,R23,R35,R36 assembled with Ferrite Bead C185 assembled with 10k resistor, R30 not assembled U2 changed to C8TL020438 USB3 crossover switch changed to C8TL020438
1.21	1.6A	Due to EOL: U35s changed to NLF182207H1A03 Due to allocation problems: U13 changed to SNE5SHV232D0R
1.22	1.6B	Due to allocation problems: U22,U29,U30,U31 changed to P/N: FPF2194
1.23	1.6C	Added VAR-SOM-AM62 Block Diagram and Symbol
1.24	1.7	Added VAR-SOM-MX93 Block Diagram and Symbol Temporary removed compatibility notes Added hard-wired EXP_MDIO_EN line.
1.25	1.7A	Due to allocation problems: U22,U29,U30,U31 changed to P/N: FPF2193
1.26	1.7B	J29 changed to USB3090-30-A
1.27	1.7C	Due to allocation problems: U2,U54 changed to P/N: TCYPC0215MT
1.28	1.7D	C14, C15, C16, C17 Are NC due to compatibility issues with VAR-SOM-MX93 Rev 2.0, WBE Assembly option.
1.29	1.7D	Added VAR-SOM-MX91 Block Diagram and Symbol

For cross probing between SOM symbol and the specific SOM Connector used, set the "Implementation" property value in SOM port symbol to one of the following:

1. VAR-SOM-MX6
2. VAR-SOM-MX8
3. VAR-SOM-MX8X
4. VAR-SOM-MX8M-MINI
5. VAR-SOM-MX8M-NANO
6. VAR-SOM-MX8M-PLUS
7. VAR-SOM-MX93
8. VAR-SOM-MX91
9. VAR-SOM-AM62

For complete alternate function per pin and specific SOM:
please refer to "VAR-SOMs Compatibility and Pinout.XLS" located at:
ftp://ftp.variscite.com/SOM_Compatibility

OFF PAGE CONNECTOR INDEX:

1. Function# :Interface common to ALL SOMs
2. J1.xxx-Function :Interface common to certain SOMs or Used for carrier board common function
3. J1.xxx :No common interface

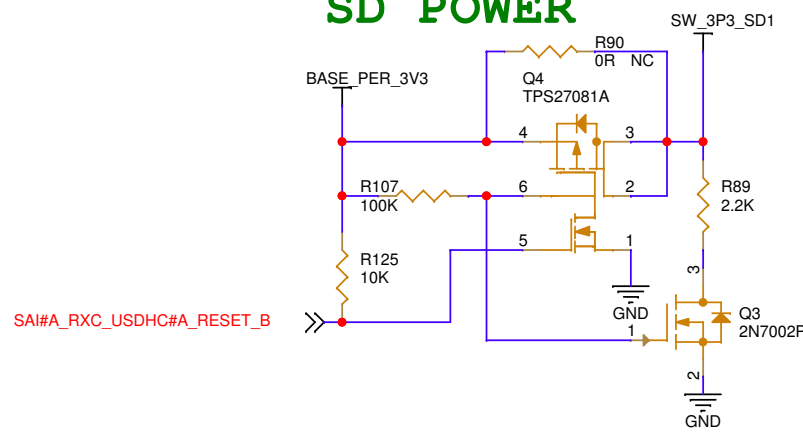
Compatibility list

Describes the ALT per SOM for compatibility.
Order of names: (MX6/MX8/MX8X/MX8MM/MX8MP)
Note: single name means identical name for all.

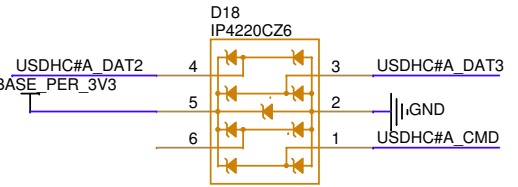
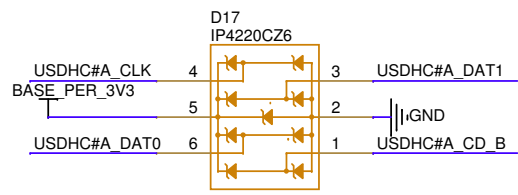
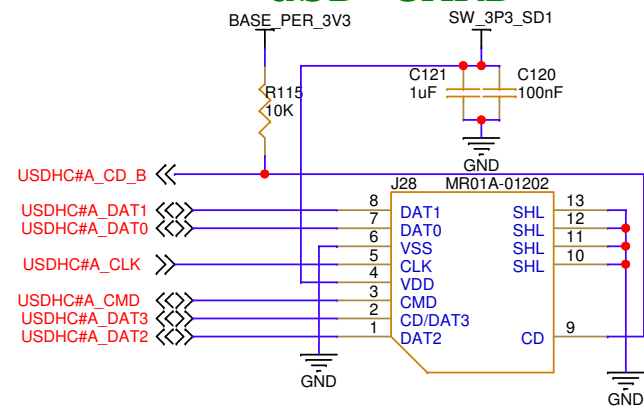


06. uSD, Audio, CAN

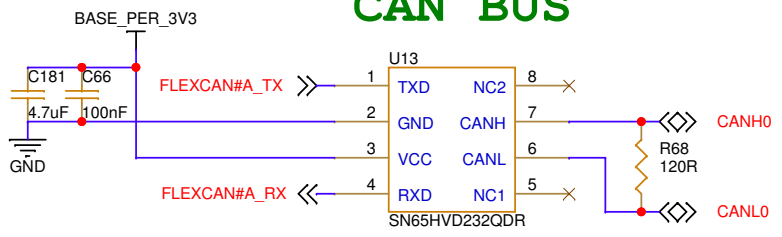
SD POWER



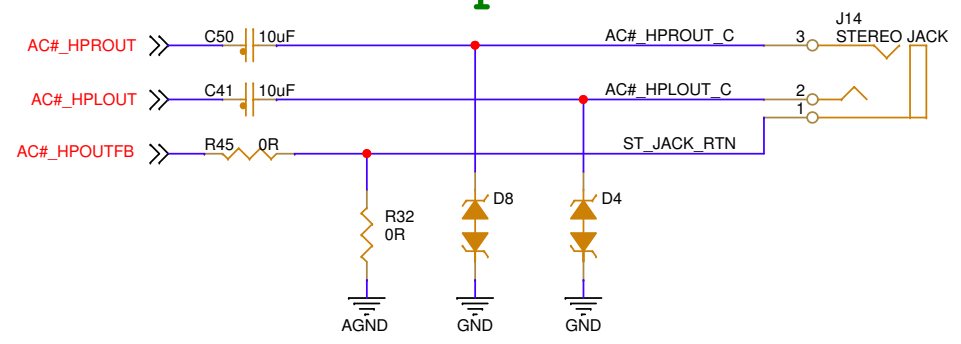
uSD CARD



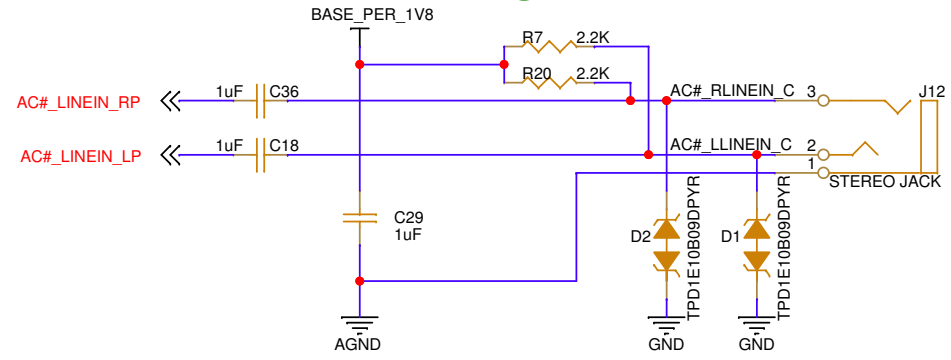
CAN BUS



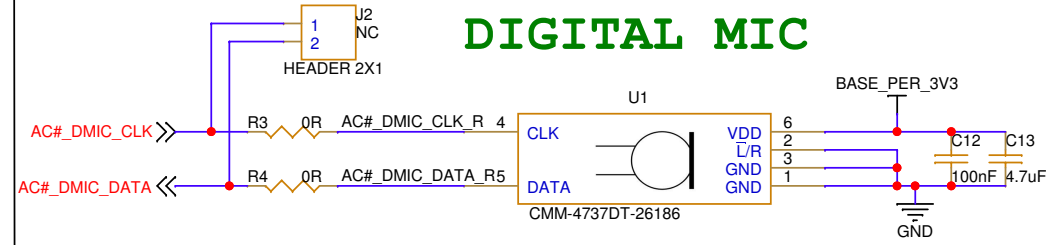
Headphones



Line In

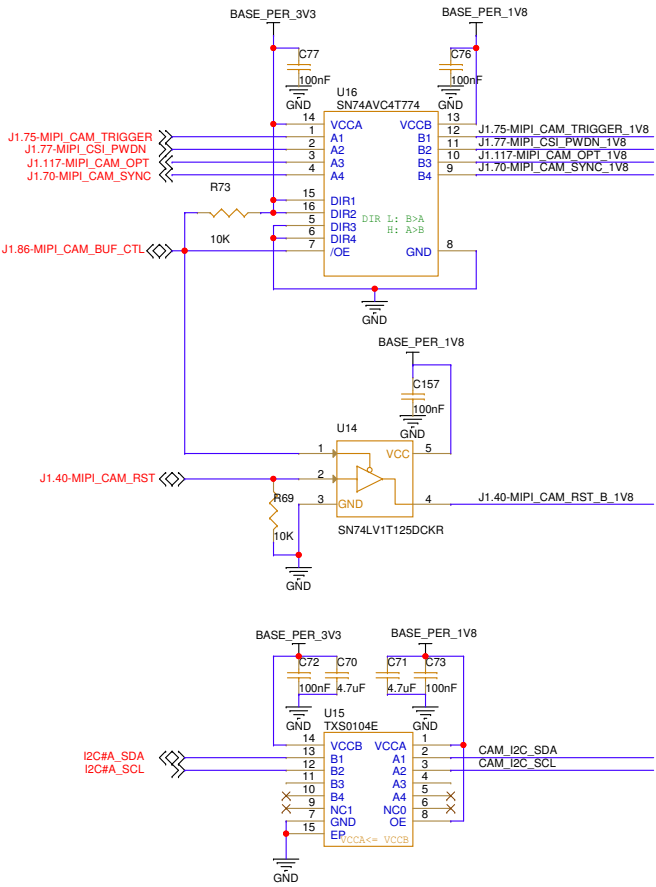


DIGITAL MIC

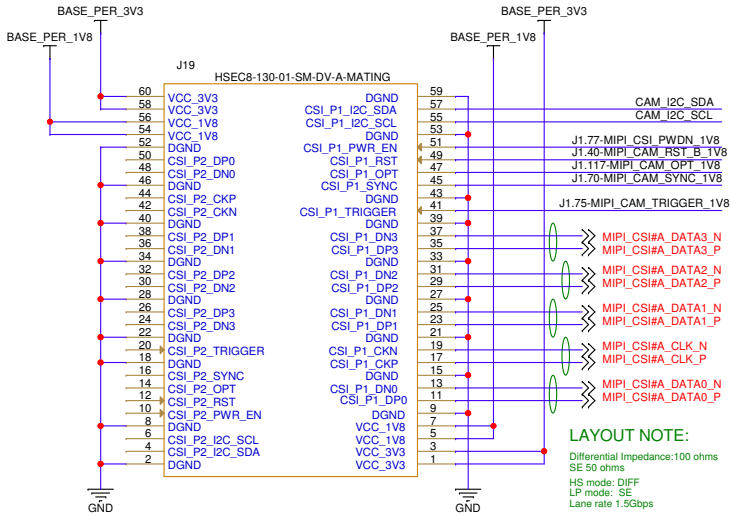


Title 06. uSD, Audio, CAN			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D
Designer: Aviad H.		Approved By:	
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07. Camera, HDMI, DP



MIPI-CSI



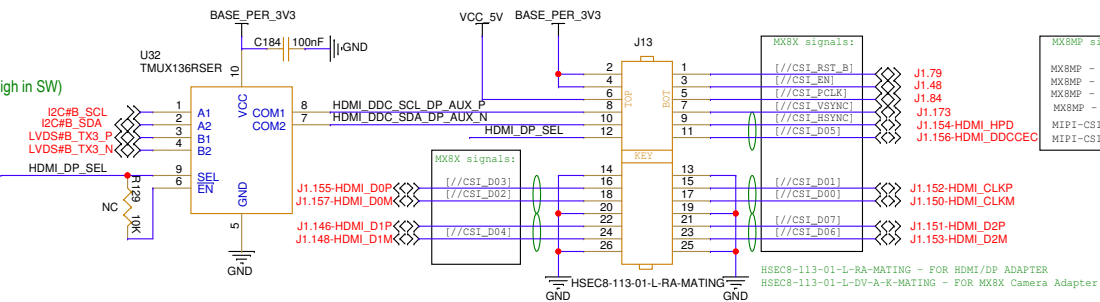
Note:
MIPI CSI#A signals appears on bottom side of J19
as of SymphonyBoard V1.4.

J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

Note for U32 (analog switch):
Switch is to enable support for the following adapters:
Parallel camera, HDMI, DisplayPort and second MIPI-CSI .

Switch select controlled on adaptor will select between:
1) I2C#B which can export
VAR-SOM-MX8X: I2C3 Used by parallel camera
VAR-SOM-MX8: HDMI DDC Used by HDMI (GPIO1_22 in should be set High in SW)
2) LVDS#B_TX3 which can export:
VAR-SOM-MX8(DP assembly option): HDMI AUX used by DP

Switch can be omitted when designing for only one of the the above interfaces.

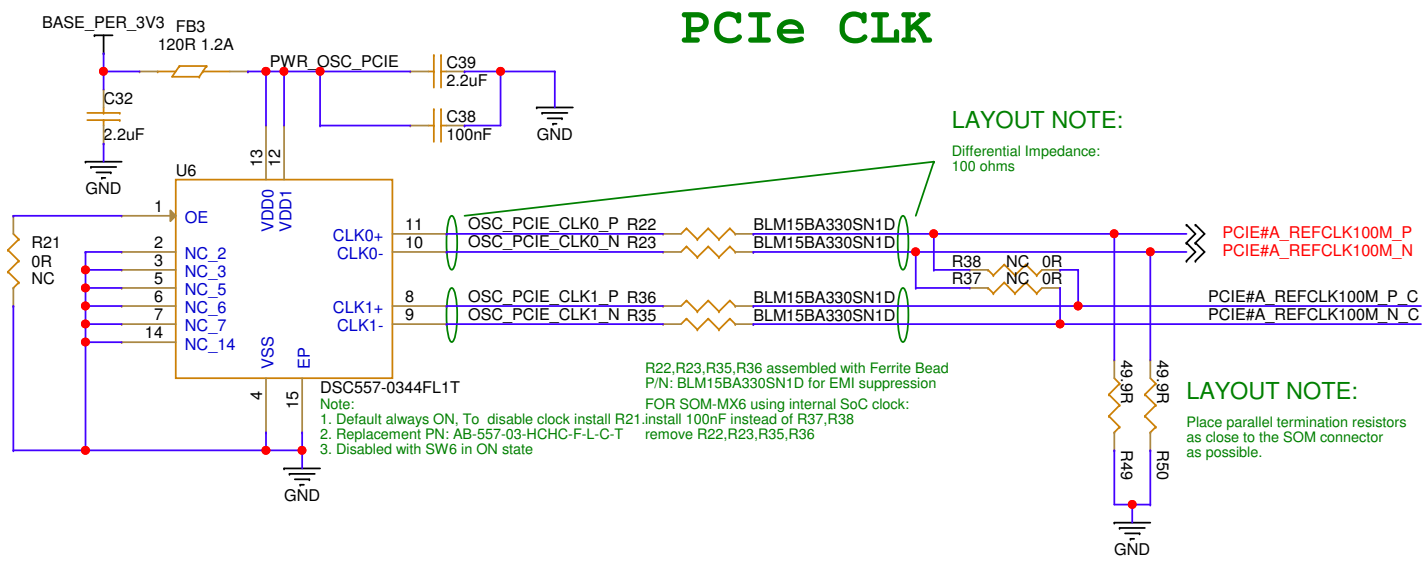


MX8MP signal note:
MX8MP - via 50mbps buffer on SOM
MX8MP - SOC IO
MX8MP - via 50mbps buffer on SOM
MX8MP - SOC IO
MIPI-CSI-D3_P diff. pair.for MX8MP
MIPI-CSI-D3_N diff. pair.for MX8MP

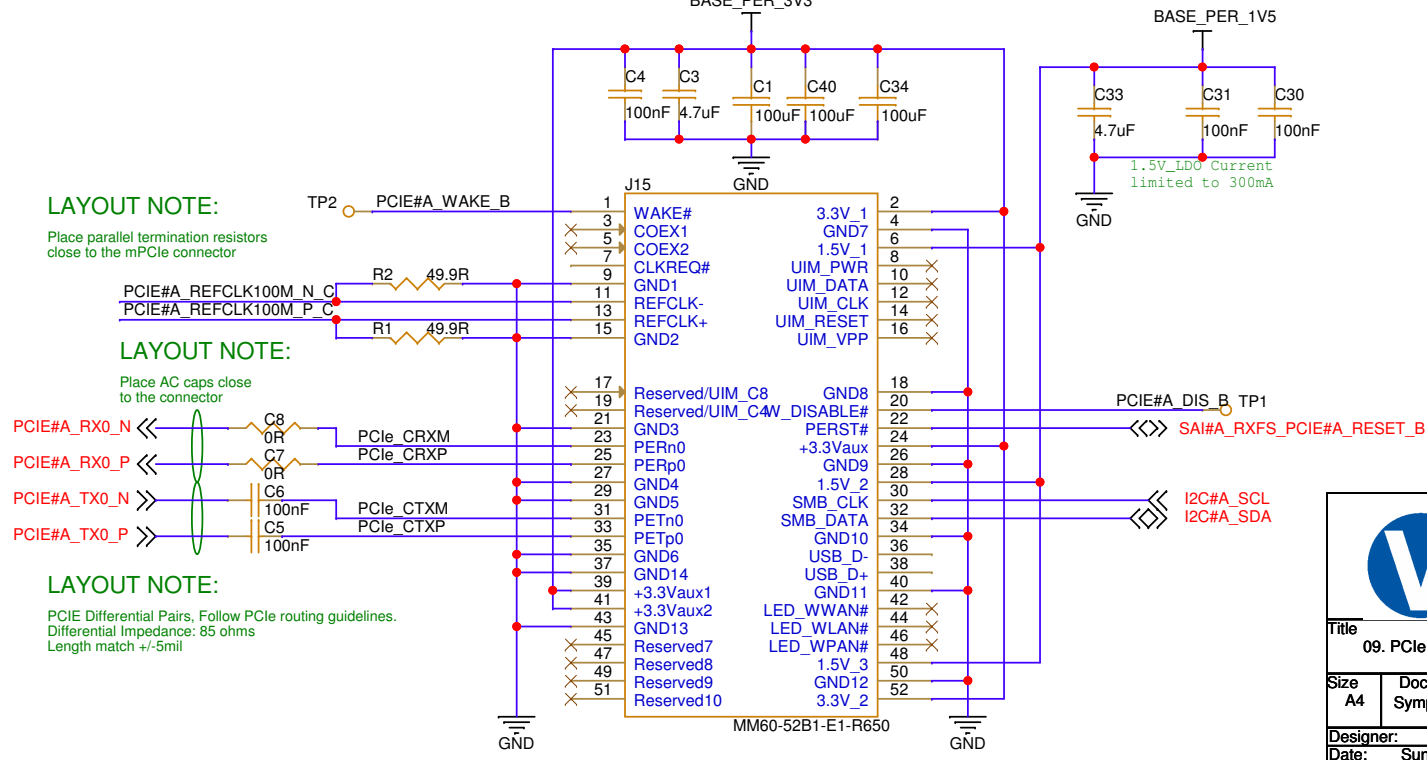
Title 07. Camera, HDMI, DP			
Size A3	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D_R1.29
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 5 of 24	

09. PCIe

PCIe CLK



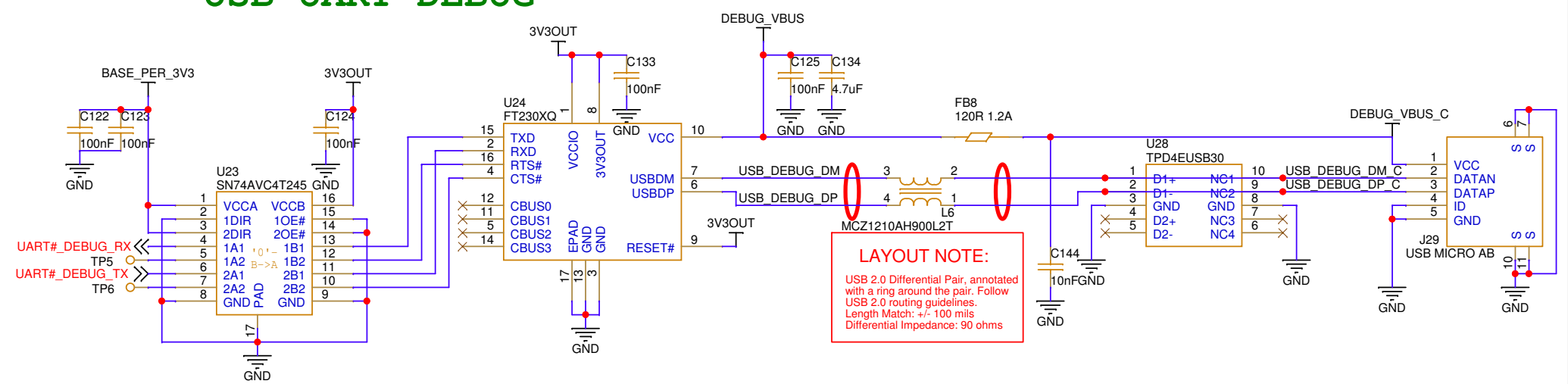
mPCIexp



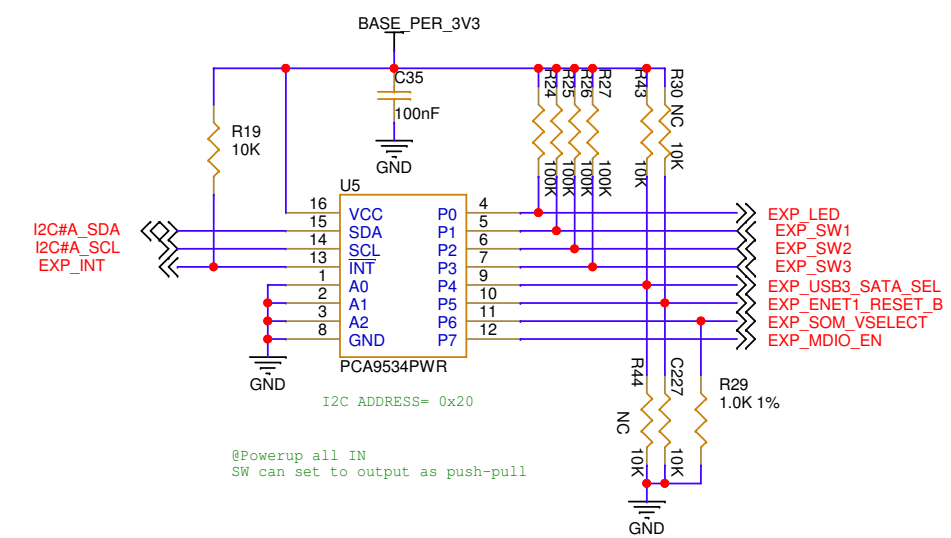
Title 09. PCIe			
Size A4	Document Number Symphony-Board	Project	Rev 1.7D_R1.2
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 7 of 24	

10. Debug, GPIO Exp, Buttons, LED

USB UART DEBUG

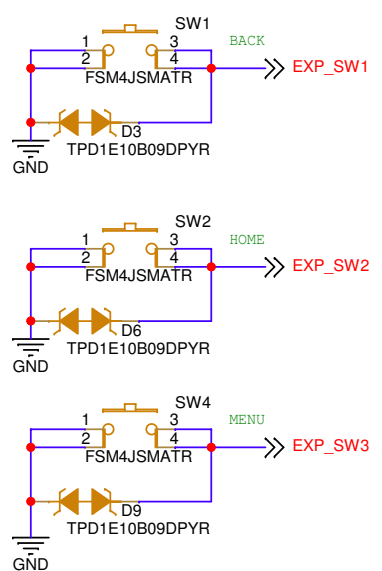


GPIO EXPANDER

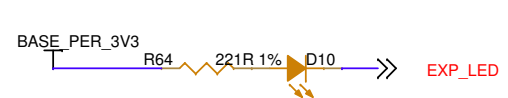


In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V.
When using pin 29 as an input pin driven by higher input voltage, use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

GP BUTTON



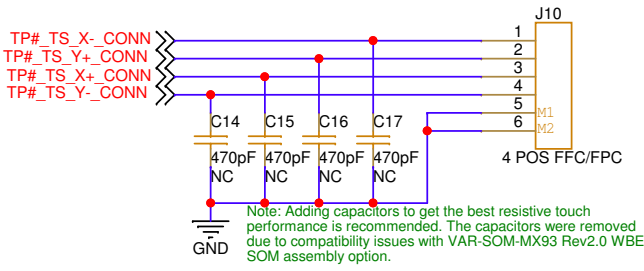
GP LED



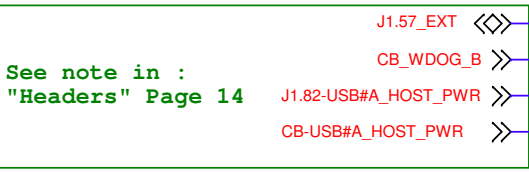
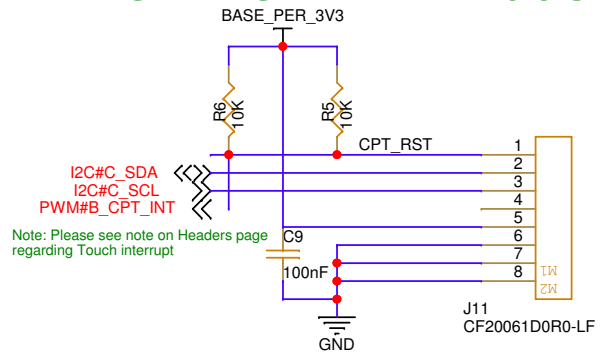
Title 10. Debug, GPIO Exp, Buttons, LED			
Size A4	Document Number Symphony-Board	Project	Rev 1.7D_R1.2
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 8 of 24	

11. LVDS, DSI, Touch

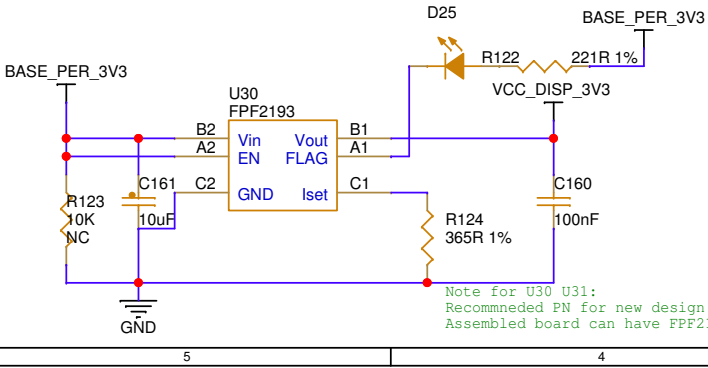
RESISTIVE TOUCH



CAPACITIVE TOUCH



Short circuit protection

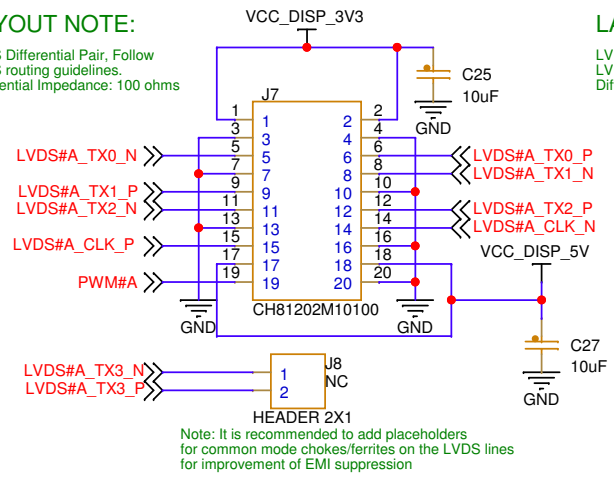


Note for U30 U31:
Recommended PN for new design PPF2193
Assembled board can have PPF2194.

LVDS DISPLAY A

LAYOUT NOTE:

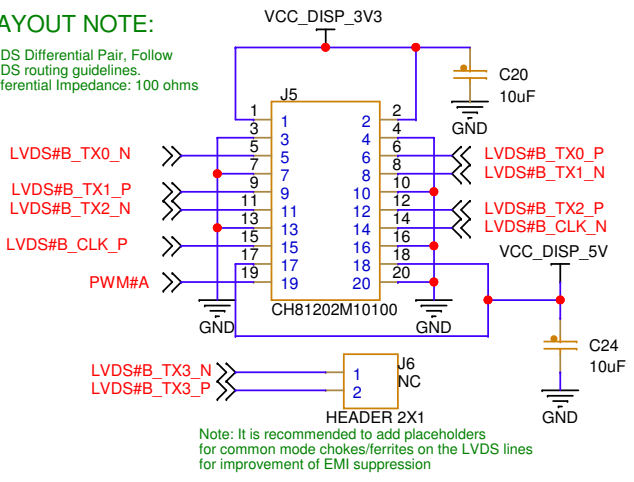
LVDS Differential Pair, Follow LVDS routing guidelines.
Differential Impedance: 100 ohms



LVDS DISPLAY B

LAYOUT NOTE:

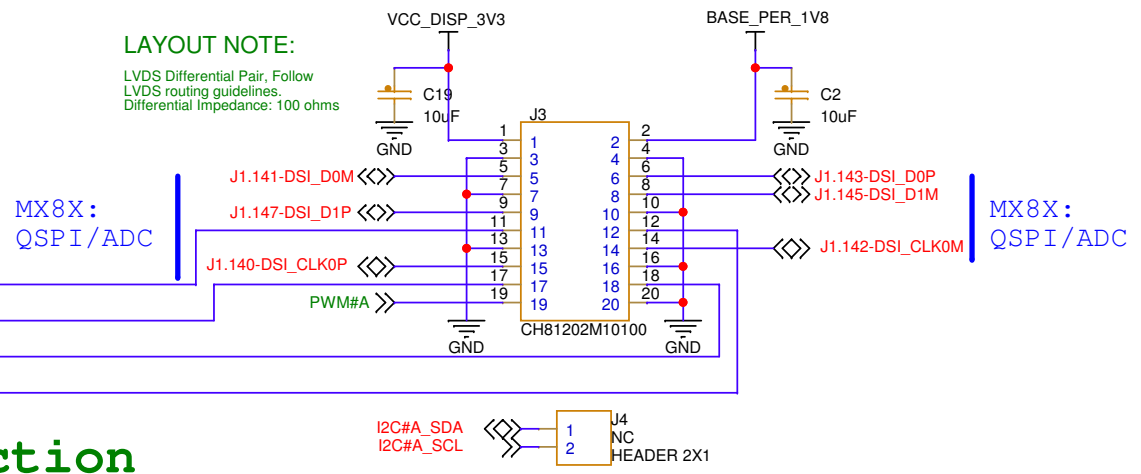
LVDS Differential Pair, Follow LVDS routing guidelines.
Differential Impedance: 100 ohms



MIPI DSI DISPLAY

LAYOUT NOTE:

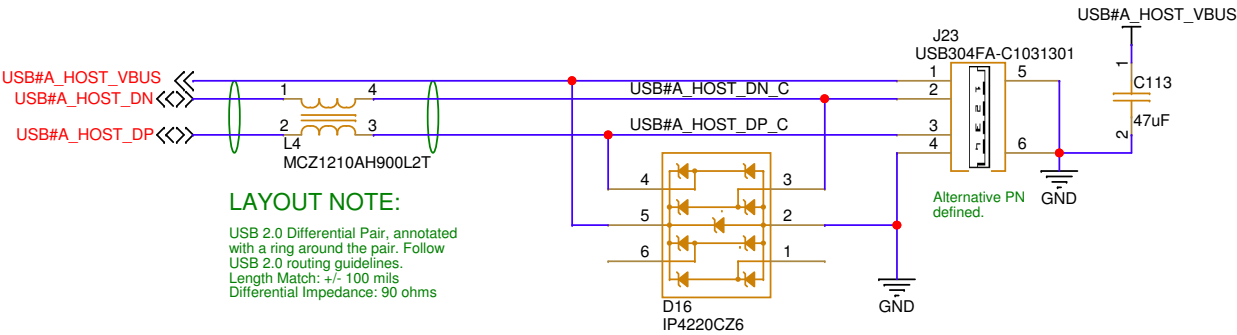
LVDS Differential Pair, Follow LVDS routing guidelines.
Differential Impedance: 100 ohms



Title 11. LVDS, DSI, Touch			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D_R
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 9 of 24	

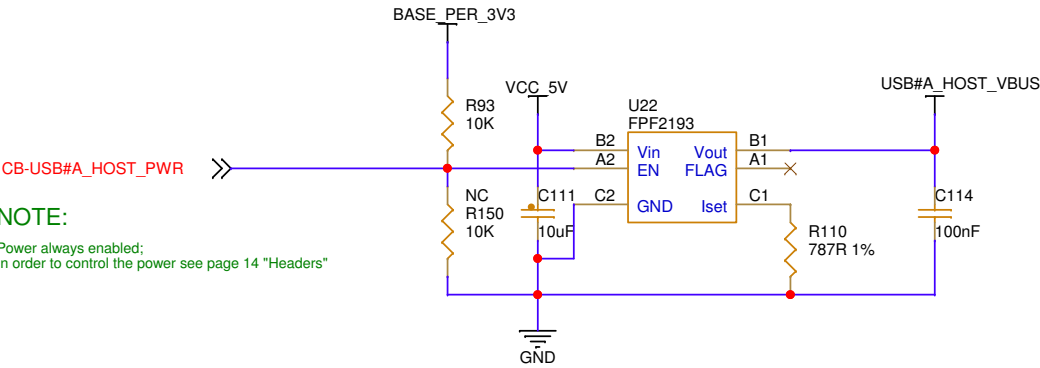
12. USB2 Host

USB2 Host



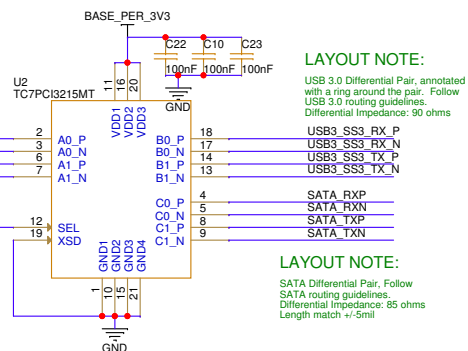
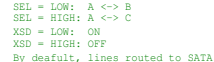
LAYOUT NOTE:
USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines.
Length Match: +/- 100 mils
Differential Impedance: 90 ohms

NOTE:
Power always enabled;
In order to control the power see page 14 "Headers"

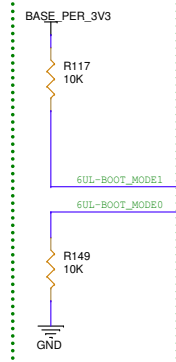


Title 12. USB2 Host			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D_R
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 10 of 24	

SATA/USB select

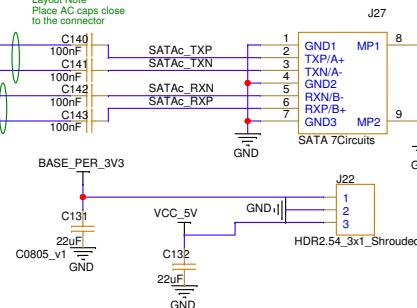


LAYOUT NOTE:
SATA Differential Pair, Follow
SATA routing guidelines.
Differential Impedance: 85 ohms
Length match +/-5mil

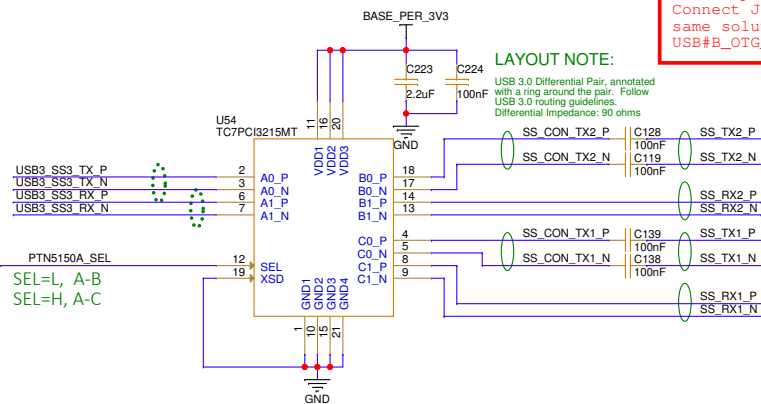


SATA Differential Pair, Follow
SATA routing guidelines.
Differential Impedance: 85 ohms
Length match +/-5mil

Layout Note
Place AC caps close to the connector



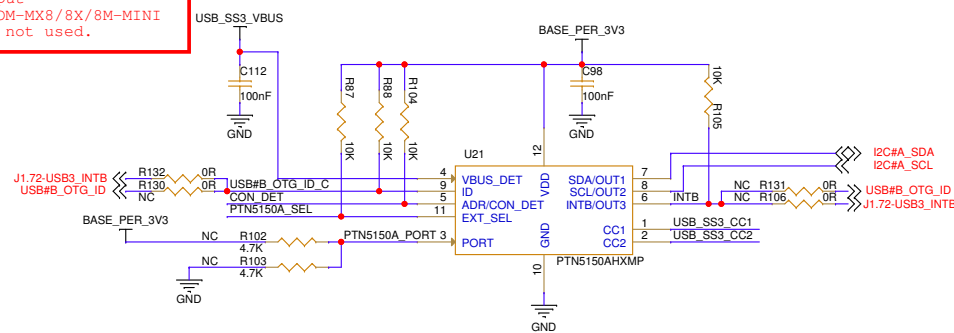
USB TYPE C Circuitry



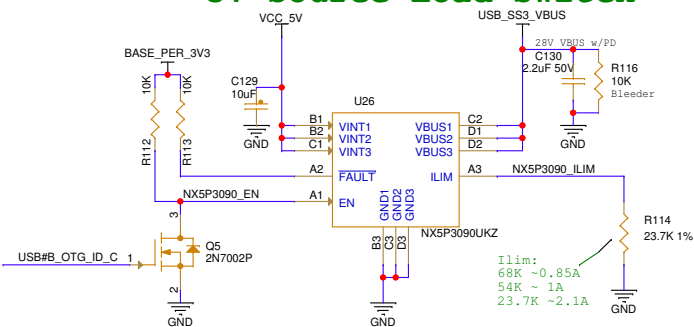
USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines.
Differential Impedance: 90 ohms

Usage of native USB_ID for iMX8MP requires patches not included in the formal release, pull up should be to 1.8V.
For simple OTG function for VAR-SOM-MX8M-PLUS Connect J1.72 GPIO to U22 PTN ID output - same solution applies also for VAR-SOM-MX8/8X/8M-MINI
USB#_OTG_ID can be left floating if not used.

Config Channel Logic Detection & Indication of Plug Orientation

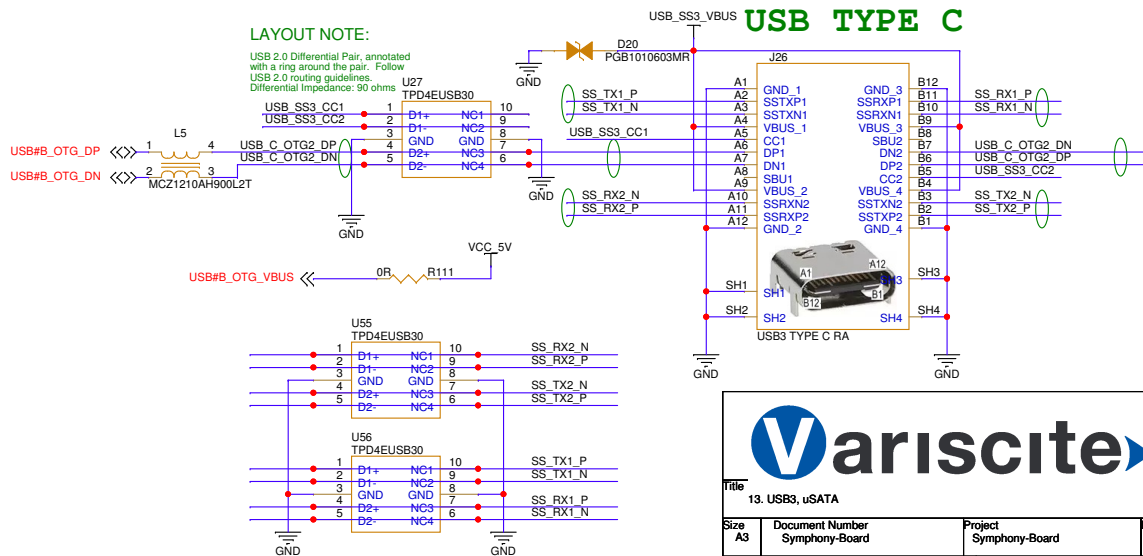


5V Source Load Switch



USB Profile 1 = 5 V @ 2.1 A

USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines.
Differential Impedance: 90 ohms

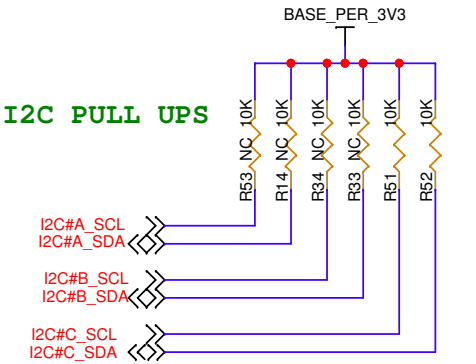
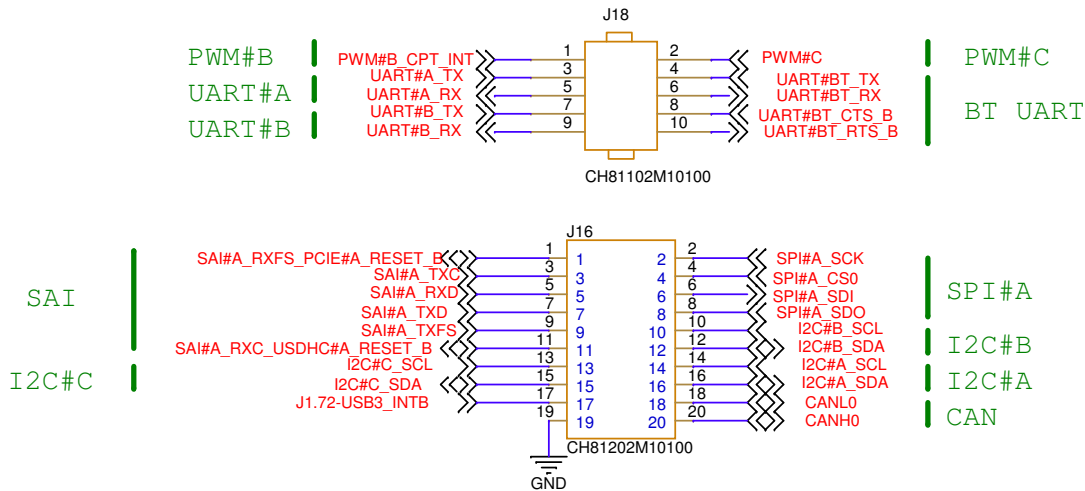


Title 13. USB3, uSATA

Size A3	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D
Designer: <u>Aviad H.</u>		Approved By:	
Date: Sunday, April 06, 2025		Sheet 11 of 24	

14. Headers

Headers arranged for compatible alternate function

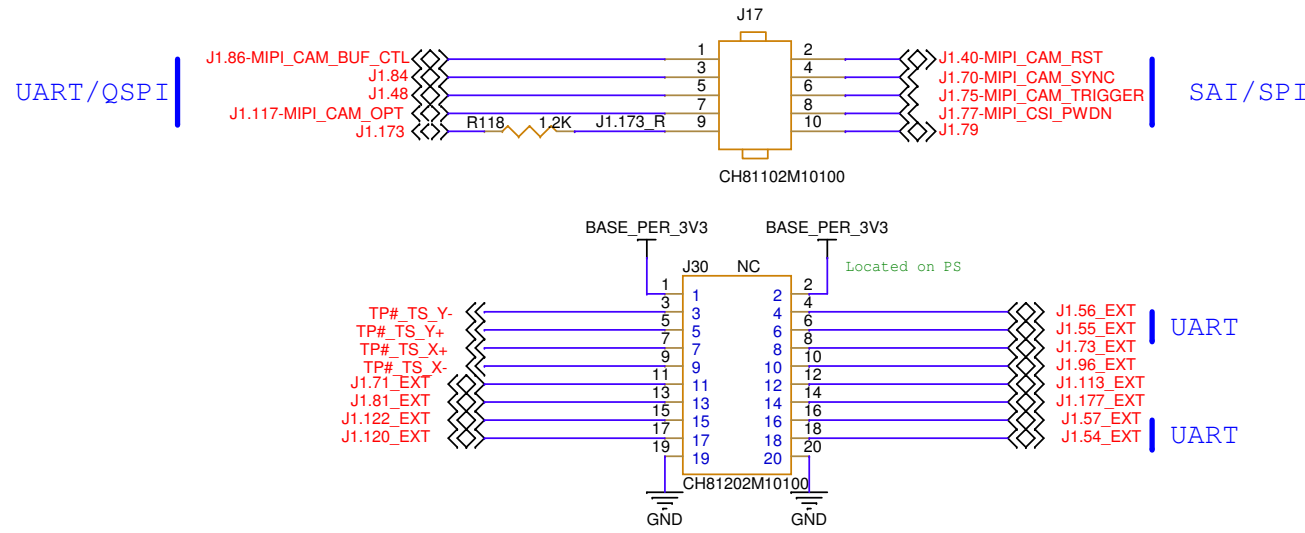


I2C_A has internal pulls in Camera buffer

I2C_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.

For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Headers arranged for partial compatible alternate function



COLD RESET ON WDOG_B EVENT for MX6/SOLO and 6UL SOMs

Listed above SOMs require short on headers to get "reboot" to function.

For all other watch dog looped on SOM

- | | | | |
|---------------|----|-------------------------|-----------|
| CB_WDOG_B | >> | Symphony Board reset | See J3.17 |
| J1.57_EXT | >> | SOM_6UL: PIN57 WDOG1_B | See J3.11 |
| PWM#B_CPT_INT | >> | MX6/SOLO: PIN68 WDOG1_B | See J18.1 |

USB#A Host VBUS power control

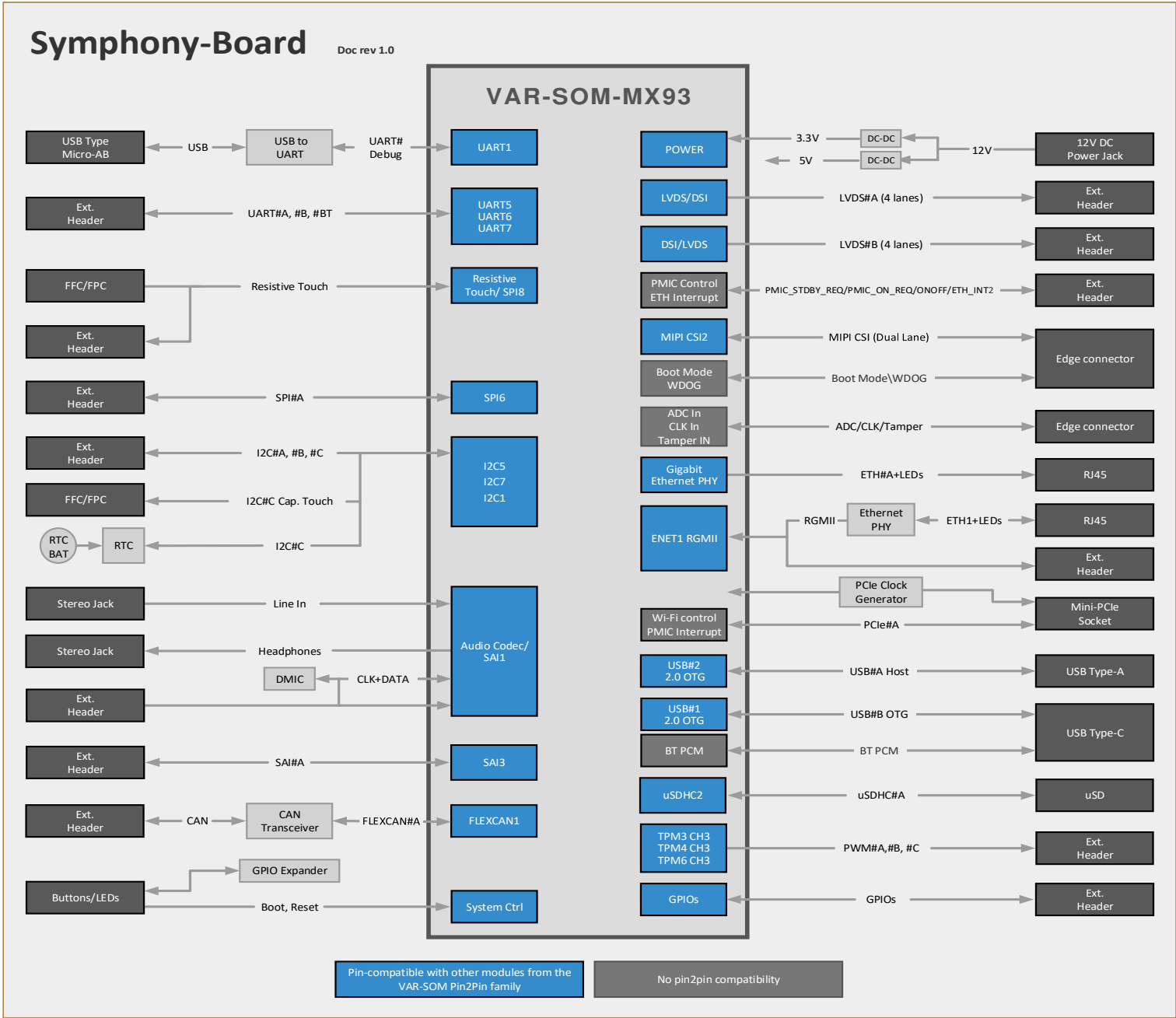
In order to control the USB#A HOST VBUS power a short is required:

- | | | | |
|----------------------|----|--------------------|-----------|
| CB-USB#A_HOST_PWR | >> | Symphony Board U22 | See J3.12 |
| J1.82-USB#A_HOST_PWR | >> | | See J3.18 |

For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS" located at: ftp://ftp.variscite.com/SOM_Compatibility

Title 14. Headers			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 12 of 24	

02. Block Diagram VAR-SOM-MX93



Title: 02. Block Diagram VAR-SOM-MX93			
Size: A3	Document Number: Symphony-Board	Project: Symphony-Board	Rev: 1.7D
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet: 21 of 24	

04. VAR-SOM-MX9x Connector

