



CONTENT

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Disclaimer:
Schematics are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.

Revision History

Document	Carrier	
1.0	1.0	Initial
1.1	1.1	Released
1.2	1.1	Updated Block Diagrams Added SH1 wire short symbol Updated Compatibility value for SOM pins 68,69,176 Updated SOM pin 22 net name Fixed U22.B1, C113.1 net name Fixed R1-R2,R35-R38 net name
1.3	1.2	Removed SH1 wire short, J1.68 routed to capacitive touch Changed R29 to C185 Changed R123,R127 to N.C. Added resistors R130-132 Removed ADC_1Inx alternate function from VAR-SOM-MX8 Symbol Updated PCIe resistor assembly note
1.4	1.2	Updated Parallel Camera/HDMI/DP Note Fixed ETH pin names VAR-SOM-MX8X Symbol
1.5	1.2A	Disconnected R129
1.6	1.2A	Added VAR-SOM-MX8M-MINI Block Diagram and Symbol PRE-RELEASE VERSION !!!!! Subject to change without notice
1.7	1.2B	Fixed VAR-SOM-MX8M-MINI Symbol Changed U29,U30,U31 to P/N: PPF2193 Changed R60 to 47K
1.8	1.2C	Update VAR-SOM-MX8M-MINI Symbol to V1.1 with side notes for v1.0B(Early access customers) Update VAR-SOM-MX8M-MINI Block Diagram POR circuitry fed by VCC_SOM: see U7 R60 R61 R40 R60 D5 Removed
1.9	1.2D	Raise VCC_3V3 to Nominal 3.39V for VAR-SOM-MX8M-MINI/NANO power up threshold voltage requirement of >3.35V
1.10	1.2E	Reference for new designs: (changes not implemented in V1.2 BRD) * Added x2 studs for heat plate support * Base_per_3v3 added slow rate limit * U7 (Base POR circuit) added CB_WDOG resistor assembly options * U29,U30,U31 - Added assembly note * VAR-SOM-MX8M-NANO pages added with symbol pinout * VAR-SOM-MX8 Connector update - added NC on /? assembly options * Power switch in OFF position discharge of Custom calls added * Ethernet magnetics - support two Mant- Pulse & UDE: - Base R445 LEDs matched to SOM behaviour - Base R445 LEDs matched to SOM behaviour
1.11	1.3	* Added VAR-SOM-MX8M-PLUS Preliminary Symbol and Block Diagram Added a 4th release version subject to change without notice * All C1210 capacitor footprint updated to C1210_v0 * MS1 to MS6 not assembled
1.12	1.3A	* ETH1 PHY clock filter U9 replaced with 49.9 Ohm R6503 resistor * Added design note for ETH1 switches U8 and U10.
1.13	1.4	* MS5 and MS6 location adopted to heatplate design - Layout * Update J1 Manufacturer P/N, NAME and footprint to present the assembled part * Replace PCIe AG caps on RX lines with 0 ohm resistors * Updated VAR-SOM-MX8M-PLUS Symbol pins 1 58 80, swap pins 41 43 and 84 147 * J19 Modify Camera connector orientation * Remove U8 U10 analog switches on ETH1 U9 revert to EM filter on RGMII_RX clock line * Added RN1 RN2 RN3 R151 R136 isolating stubs on ETH1 RGMII signals * U26 footprint updated to DS * Y1 C58 C67 updated - Support for VAR-SOM-6UL boot: - BOOT_MODE1 - R117 assembled - BOOT_MODE0 - Added PD R149 - USB4 PWR to HOST J23 always enabled - Remove R39 on pin J1.156 to support SOM-MX8MP 2nd MIPI-CSI Lane2 routing - J3 J30 pinout change
1.14	1.4A	* Support for VAR-SOM-MX8MP USB OTG - Changed U5.P4 Pull for board identification, U21.9 connected to GPIO: - Changed R43,R130,R106 to N.C. - Changed R44,R132 to Assembled * Changed Q4 P/N from: TPS27082L (EOL) to -> TPS27081A * Updated VAR-SOM-MX8M-PLUS Block Diagram, Symbol pins 36,38 names * Added notes for SOM pins 29,79,84
1.15	1.4A	Changes in v1.14/1.4A for R43,R44 were not implemented (part of board identification) and only appear in revision history; board identification implemented via EEPROM U5. Board identification required for OS to identify method of OTG ID used: PTN5150 or GPIO
1.16	1.5	* Modified VCC_3V3 to 3.35V nominal for all SOMs. For VAR-SOM-MX8M-MINI/NANO, power up threshold voltage requirement of >3.35V is implemented using Q10,R152 * Added note for VAR-SOM-MX8M-MINI/NANO pin 91
1.17	1.5	* Updated note for IC9B pull up resistors
1.18	1.5	* Updated note for PTN36043BXY chip
1.19	1.5A	* Q10 changed to ZN7002P.215 Transistor Q10 changed to ZN7002P to stabilize the SOM voltage in the OFF state. Old transistor leakage current (IDG) changed the feedback current and increased the SOM voltage. ZN7002P does not have SG diode that allowed IDSS to flow into the Gate * SOM Pin 84 Note changed
1.20	1.6	Ethernet PHY replaced to ADIN1300 R22,R23,R35,R36 assembled with Ferrite Bead C185 assembled with 10K resistor, R30 not assembled U2 changed to CBTLL02043B USB3 crossover switch changed to CBTLL02043B
1.21	1.6A	Due to EOL: U35 changed to NFL182T207H1A3D Due to allocation problems: U13 changed to SN65HVD232QDOR
1.22	1.6B	Due to allocation problems: U22,U29,U30,U31 changed to P/N: PPF2194
1.23	1.6C	Added VAR-SOM-AM62 Block Diagram and Symbol
1.24	1.7	Added VAR-SOM-MX93 Block Diagram and Symbol Temporary removed compatibility notes Added hand wired EXP_MDIO_EN line.
1.25	1.7A	Due to allocation problems: U22,U29,U30,U31 changed to P/N: PPF2193
1.26	1.7B	J29 changed to USB3090-30-A
1.27	1.7C	Due to allocation problems: U2,U54 changed to P/N: TC7PC08215MT
1.28	1.7D	C14, C15, C16, C17 Are NC due to compatibility issues with VAR-SOM-MX93 Rev 2.0, WBE Assembly option.
1.29	1.7D	Added VAR-SOM-MX91 Block Diagram and Symbol

For cross probing between SOM symbol and the specific SOM Connector used, set the "Implementation" property value in SOM port symbol to one of the following:

1. VAR-SOM-MX6
2. VAR-SOM-MX8
3. VAR-SOM-MX8X
4. VAR-SOM-MX8M-MINI
5. VAR-SOM-MX8M-NANO
6. VAR-SOM-MX8M-PLUS
7. VAR-SOM-MX93
8. VAR-SOM-MX91
9. VAR-SOM-AM62

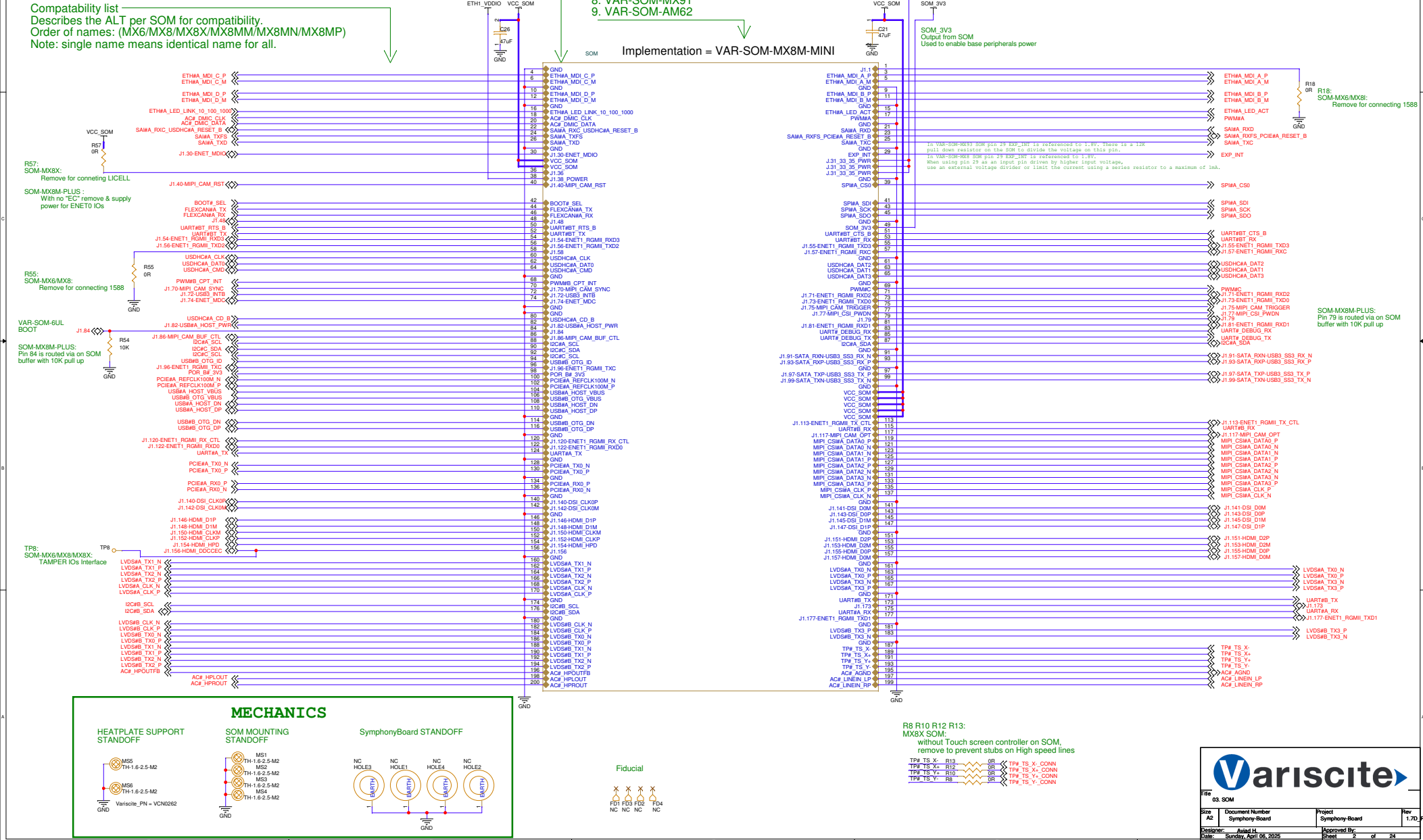
For complete alternate function per pin and specific SOM:
please refer to "VAR-SOMs Compatibility and Pinout.XLS" located at:
ftp://ftp.variscite.com/SOM_Compatibility

OFF PAGE CONNECTOR INDEX:

1. Function# :Interface common to ALL SOMs
2. J1.xxx-Function :Interface common to certain SOMs or Used for carrier board common function
3. J1.xxx :No common interface

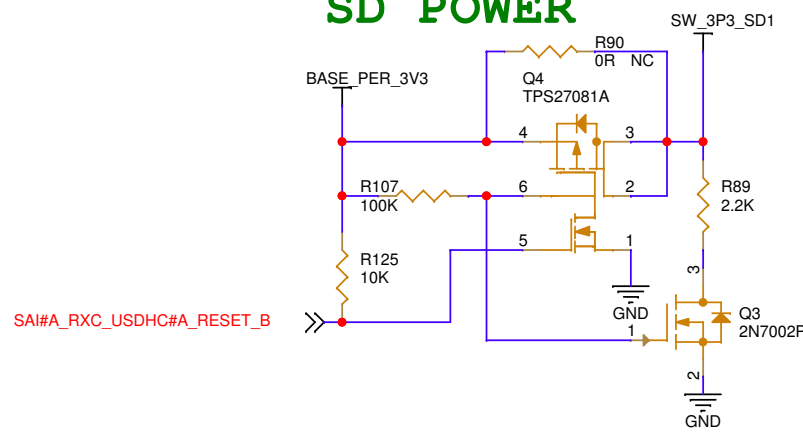
Compatibility list

Describes the ALT per SOM for compatibility.
Order of names: (MX6/MX8/MX8X/MX8MM/MX8MP)
Note: single name means identical name for all.

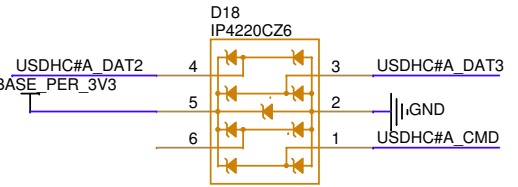
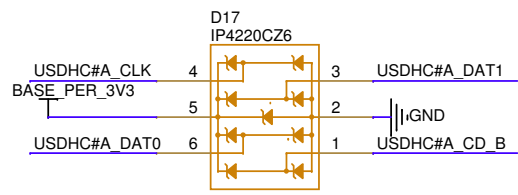
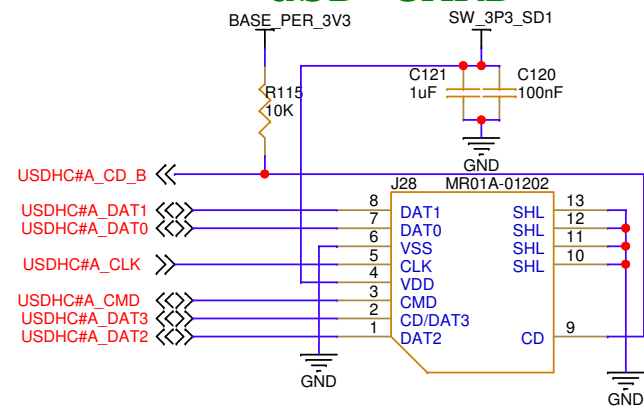


06. uSD, Audio, CAN

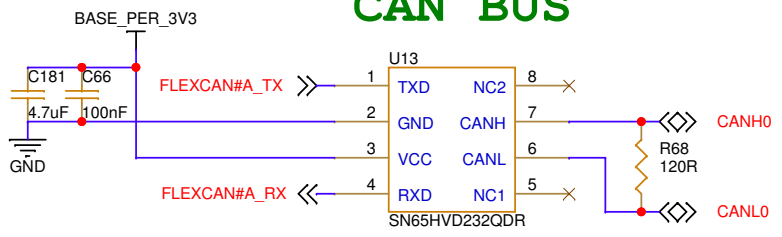
SD POWER



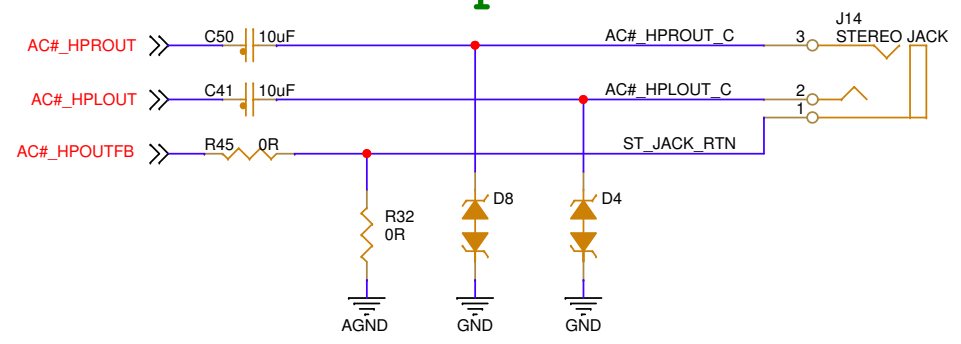
uSD CARD



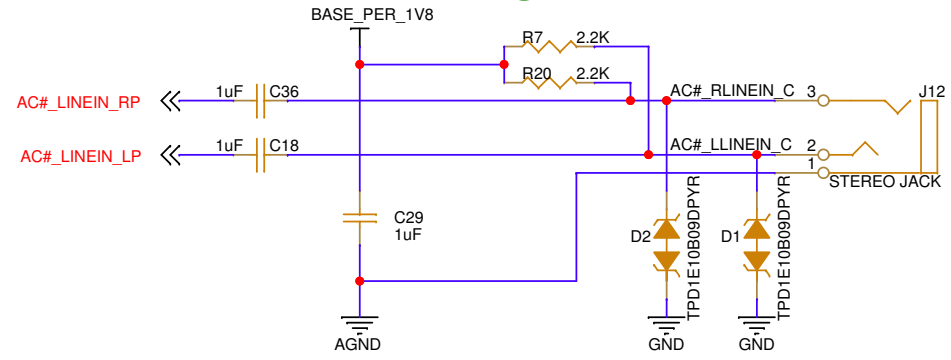
CAN BUS



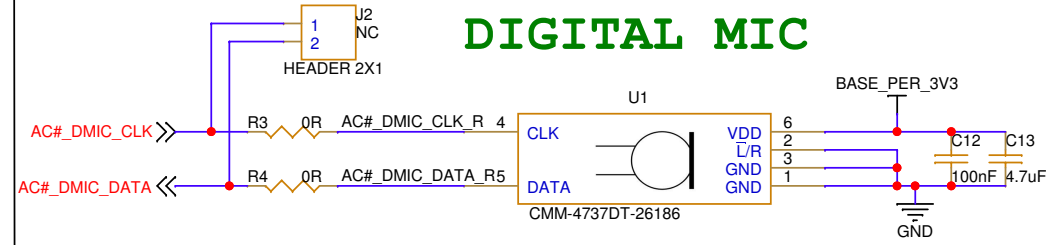
Headphones



Line In

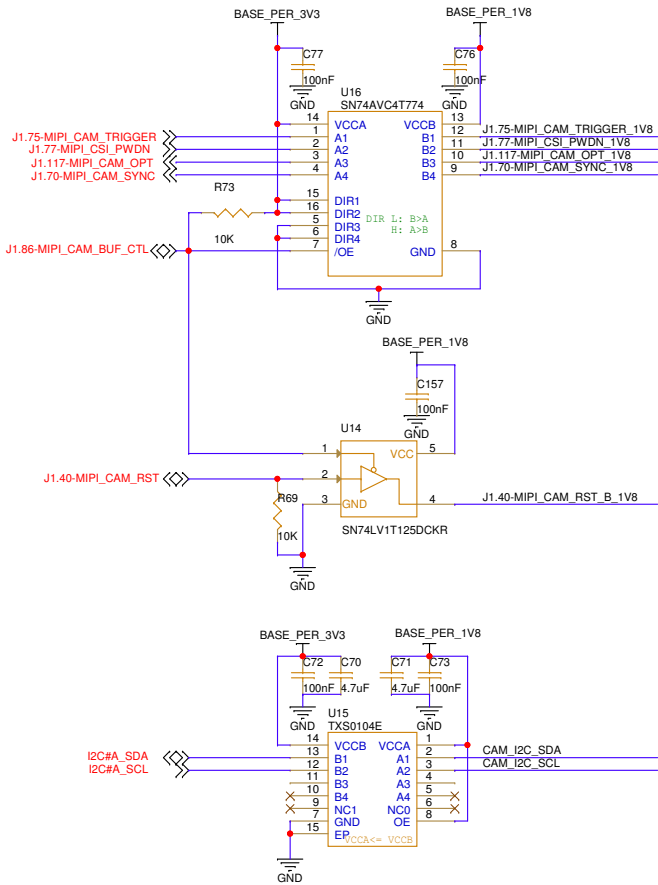


DIGITAL MIC

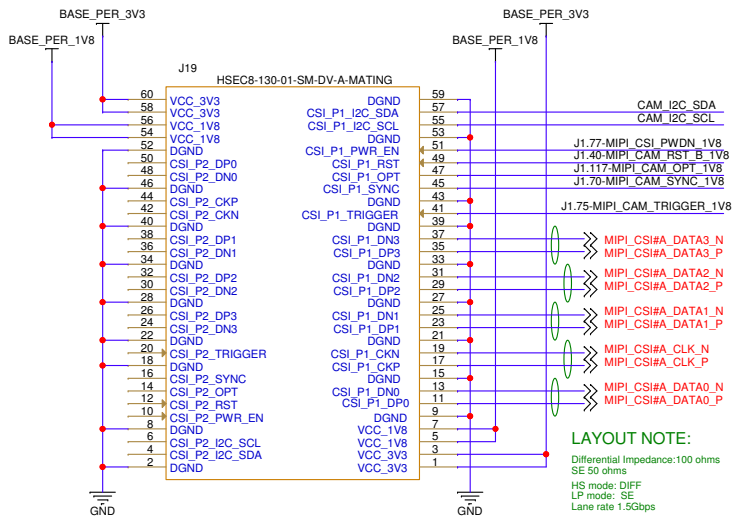


Title 06. uSD, Audio, CAN			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D
Designer: Aviad H.		Approved By:	
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07. Camera, HDMI, DP

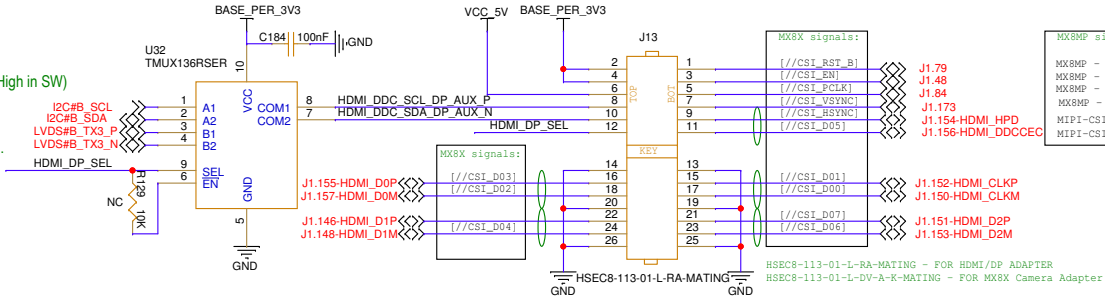


MIPI-CSI



Note:
MIPI CSI#A signals appears on bottom side of J19
as of SymphonyBoard V1.4.

J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI



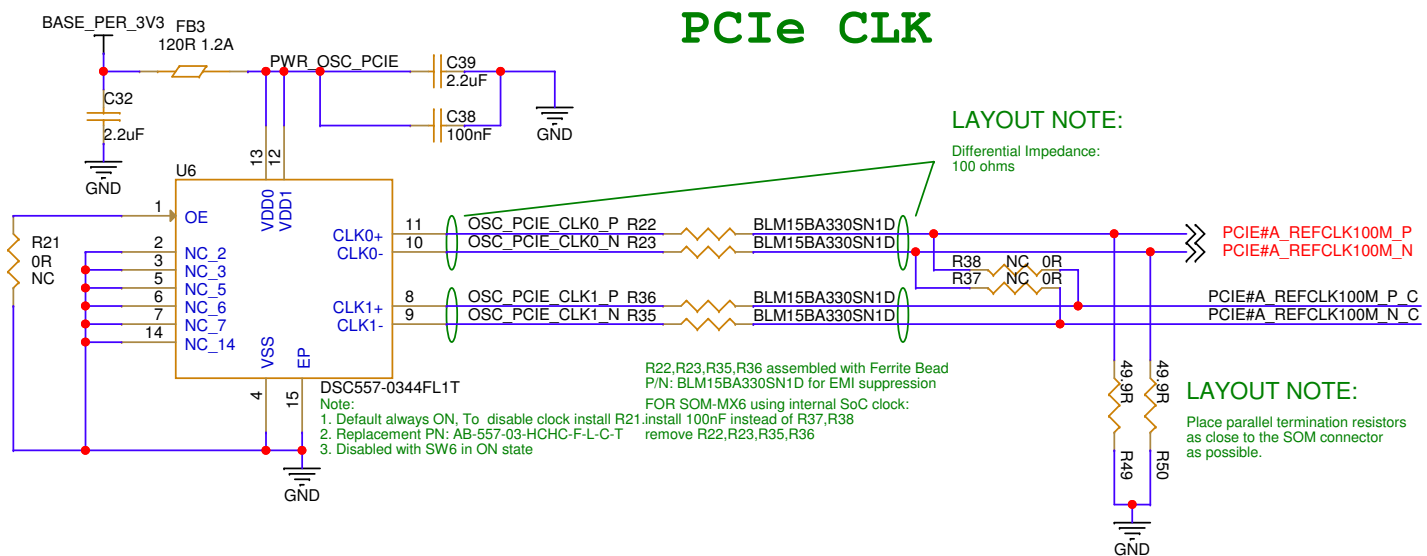
MX8MP signal note:
MX8MP - via 50mbps buffer on SOM
MX8MP - SOC IO
MX8MP - via 50mbps buffer on SOM
MX8MP - SOC IO
MIPI-CSI-D3_P diff. pair for MX8MP
MIPI-CSI-D3_N diff. pair for MX8MP



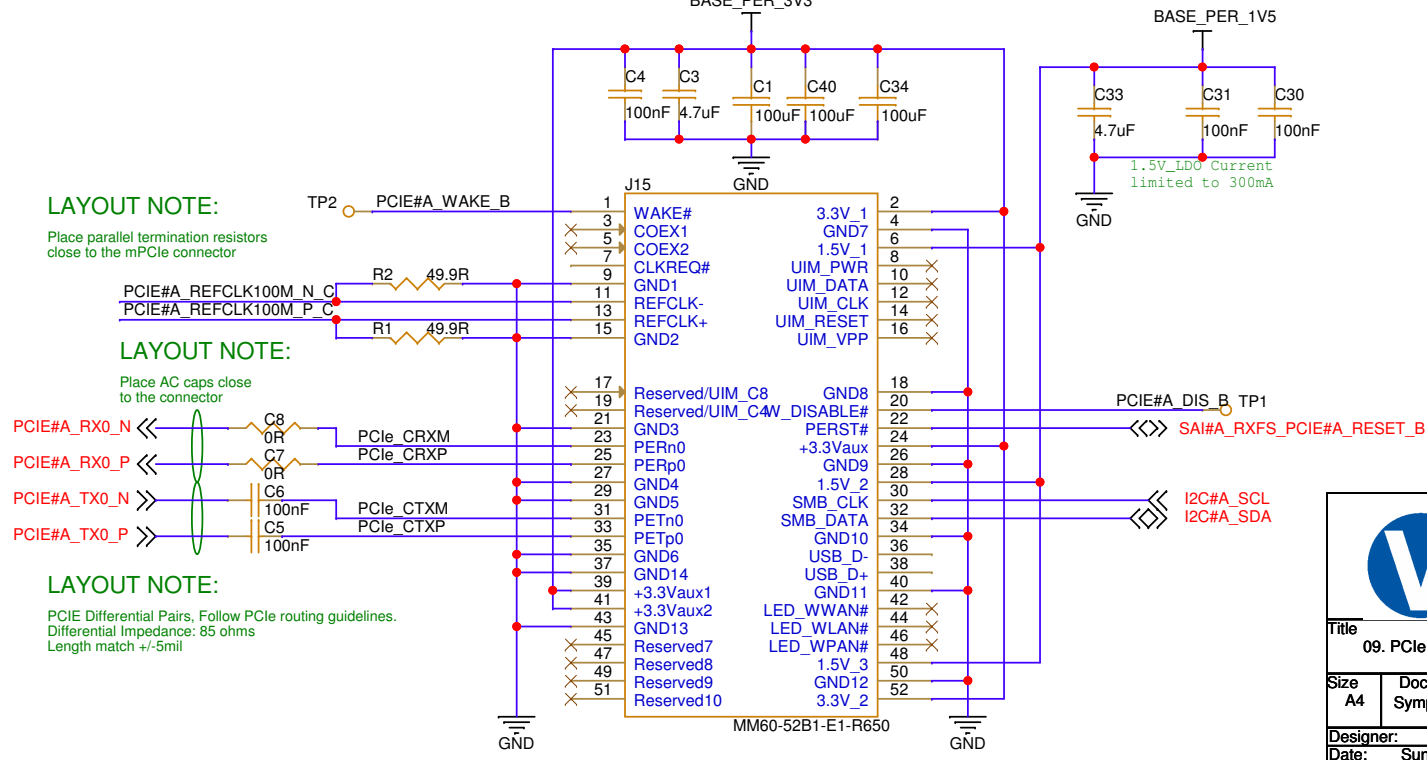
Title 07. Camera, HDMI, DP			
Size A3	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D_R1.29
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 5 of 24	

09. PCIe

PCIe CLK



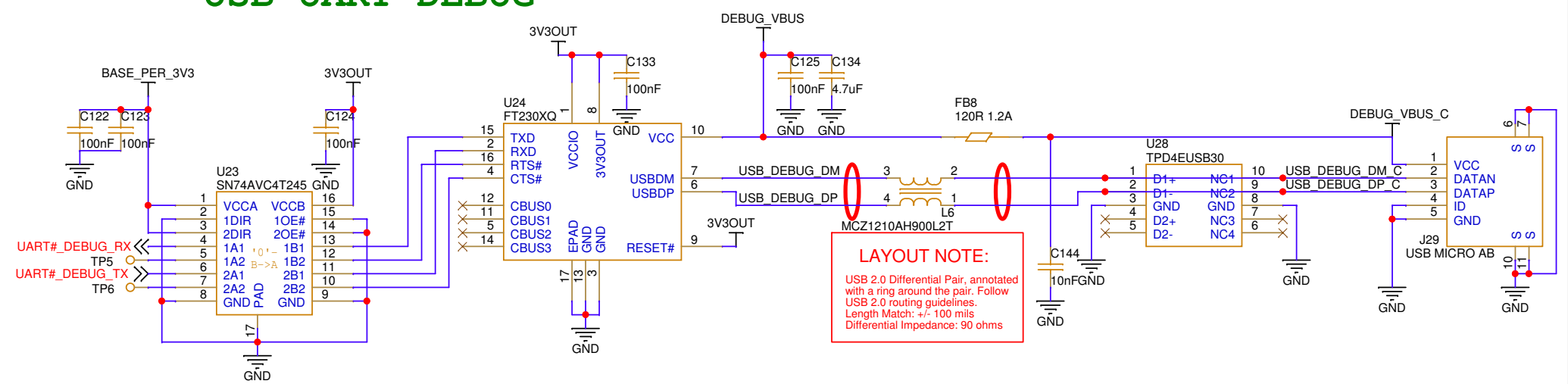
mPCIexp



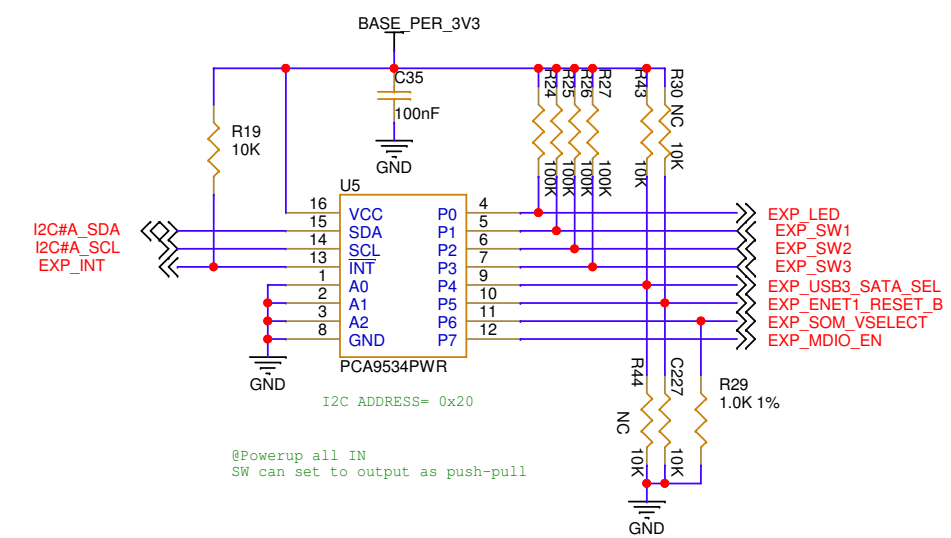
Title 09. PCIe			
Size A4	Document Number Symphony-Board	Project	Rev 1.7D_R1.2
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 7 of 24	

10. Debug, GPIO Exp, Buttons, LED

USB UART DEBUG

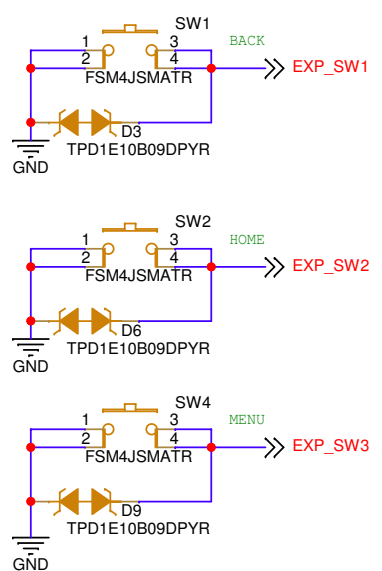


GPIO EXPANDER

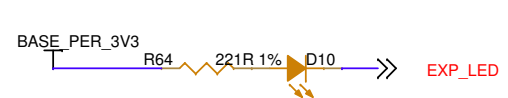


In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V.
When using pin 29 as an input pin driven by higher input voltage, use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

GP BUTTON



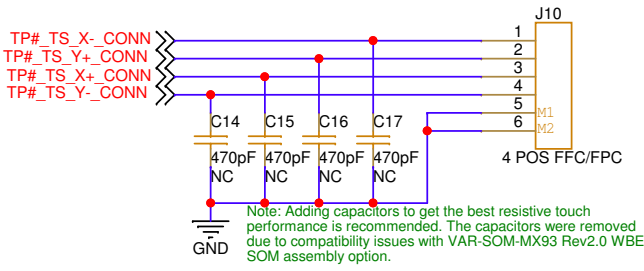
GP LED



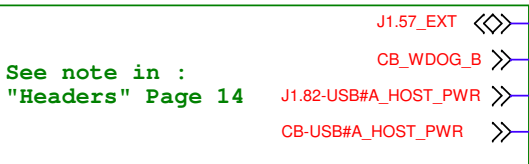
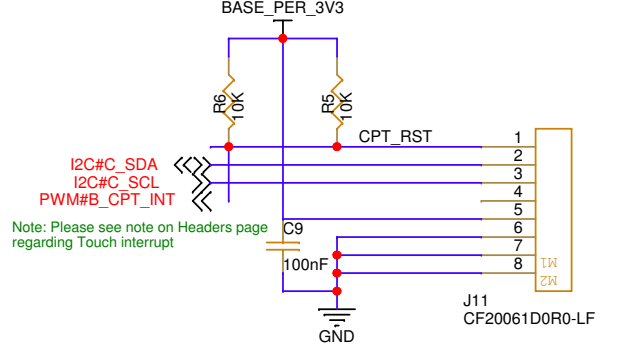
Title 10. Debug, GPIO Exp, Buttons, LED			
Size A4	Document Number Symphony-Board	Project	Rev 1.7D_R1.2
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 8 of 24	

11. LVDS, DSI, Touch

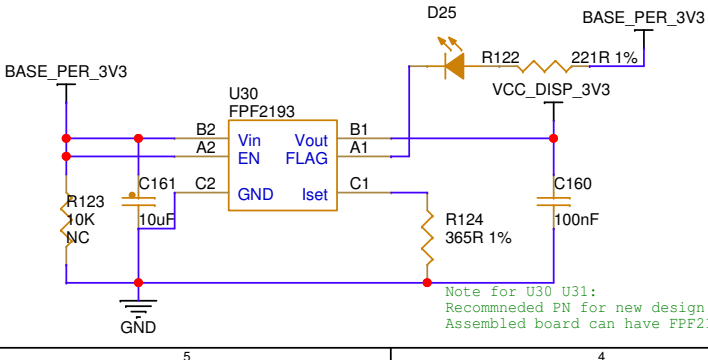
RESISTIVE TOUCH



CAPACITIVE TOUCH



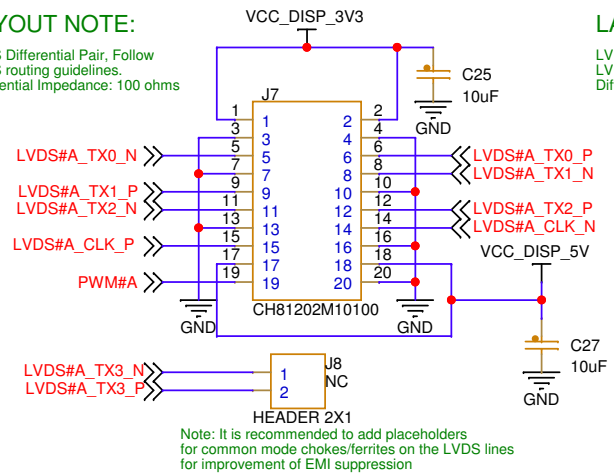
Short circuit protection



LVDS DISPLAY A

LAYOUT NOTE:

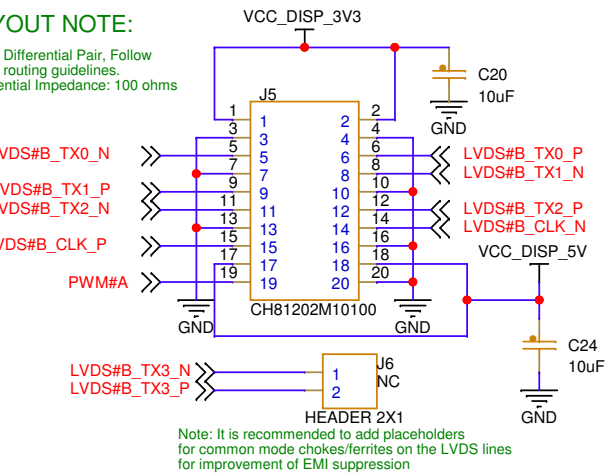
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms



LVDS DISPLAY B

LAYOUT NOTE:

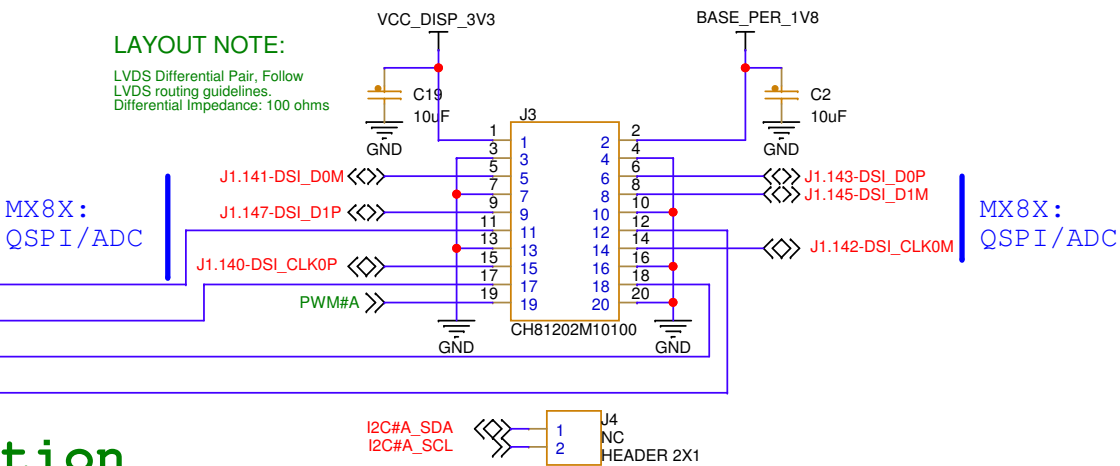
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms



MIPI DSI DISPLAY

LAYOUT NOTE:

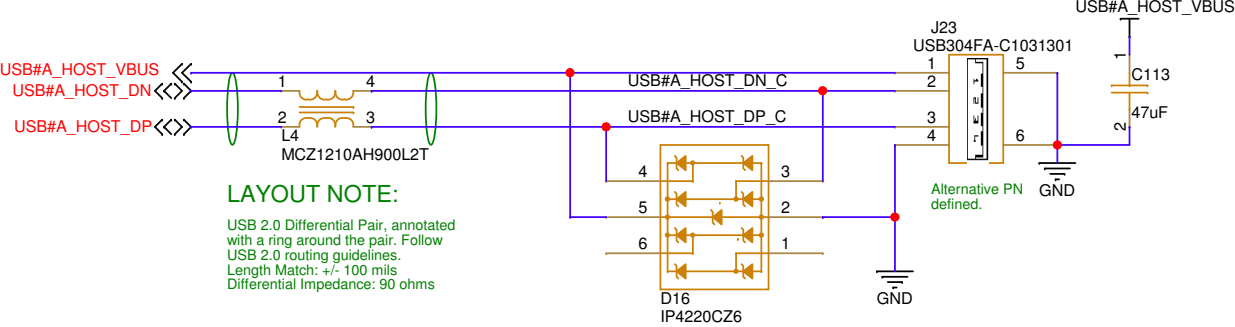
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms



Title 11. LVDS, DSI, Touch			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D_R
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 9 of 24	

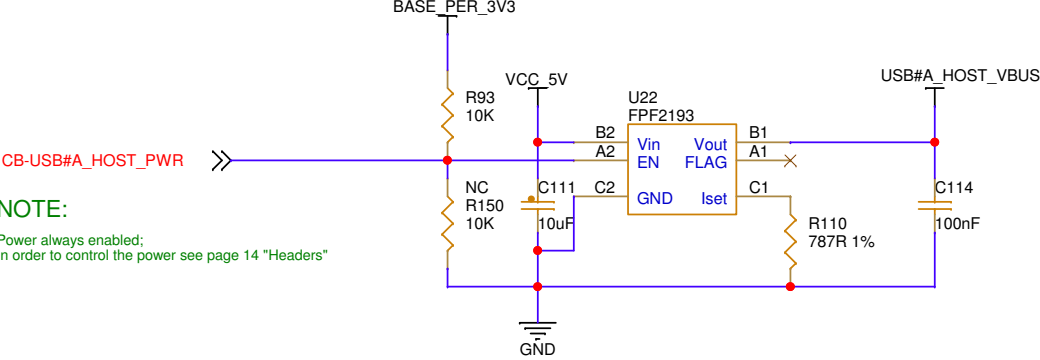
12. USB2 Host


USB2 Host



LAYOUT NOTE:
USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines. Length Match: +/- 100 mils Differential Impedance: 90 ohms

NOTE:
Power always enabled;
In order to control the power see page 14 "Headers"



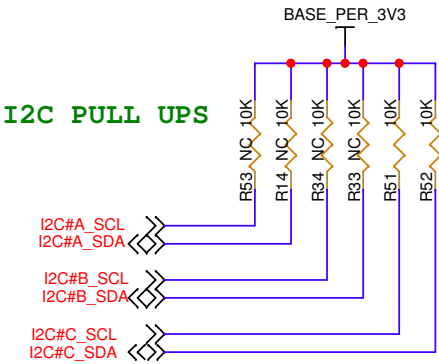
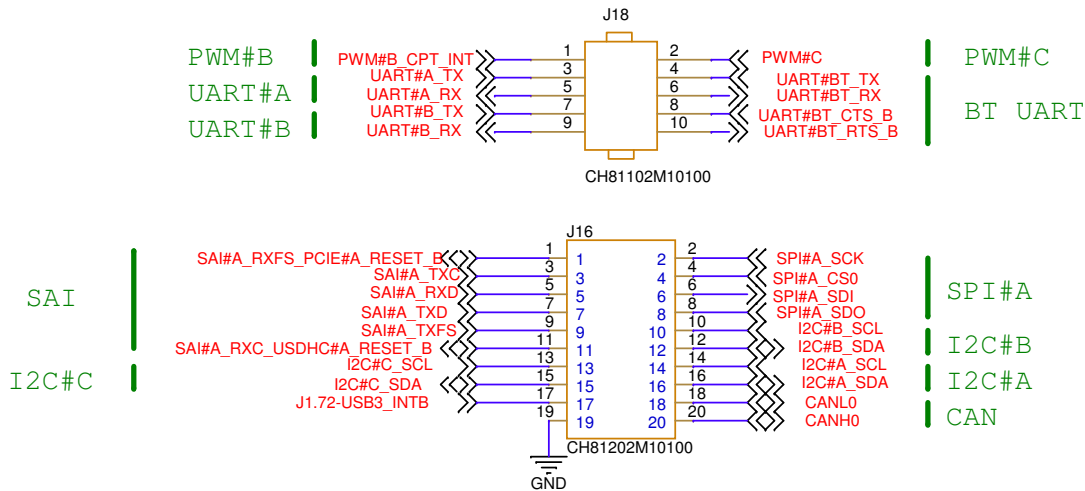


12. USB2 Host

Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D_R
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 10 of 24	

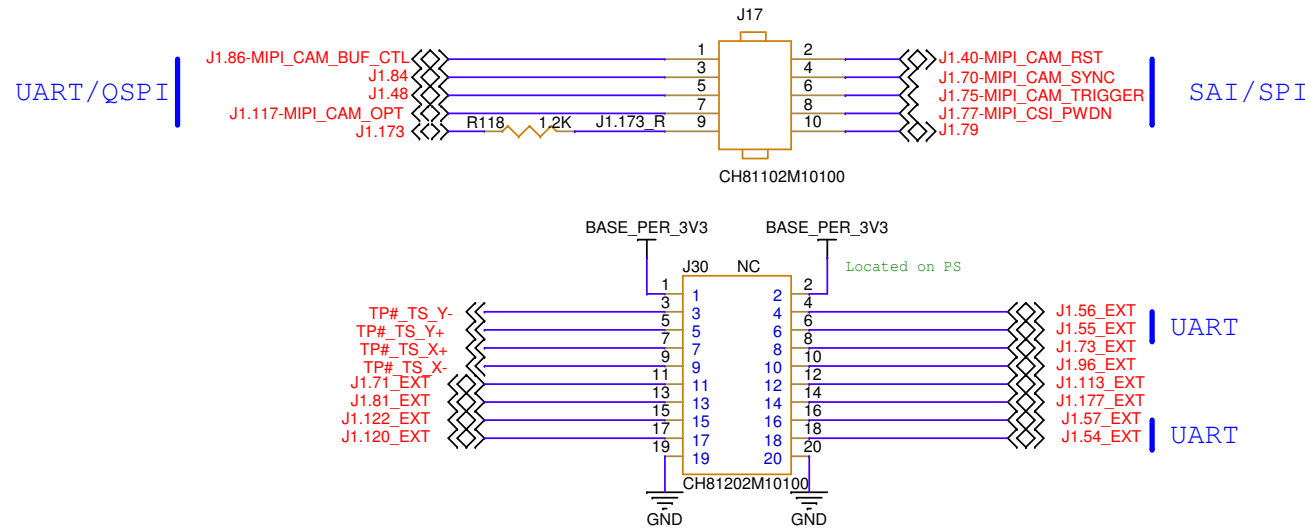
14. Headers

Headers arranged for compatible alternate function



I2C_A has internal pulls in Camera buffer
I2C_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.
For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Headers arranged for partial compatible alternate function



COLD RESET ON WDOG_B EVENT for MX6/SOLO and 6UL SOMs

Listed above SOMs require short on headers to get "reboot" to function.
For all other watch dog looped on SOM

- CB_WDOG_B >> Symphony Board reset See J3.17
- J1.57_EXT >> SOM_6UL: PIN57 WDOG1_B See J3.11
- PWM#B_CPT_INT >> MX6/SOLO: PIN68 WDOG1_B See J18.1

USB#A Host VBUS power control

In order to control the USB#A HOST VBUS power a short is required:

- CB-USB#A_HOST_PWR >> Symphony Board U22 See J3.12
- J1.82-USB#A_HOST_PWR >> control input See J3.18

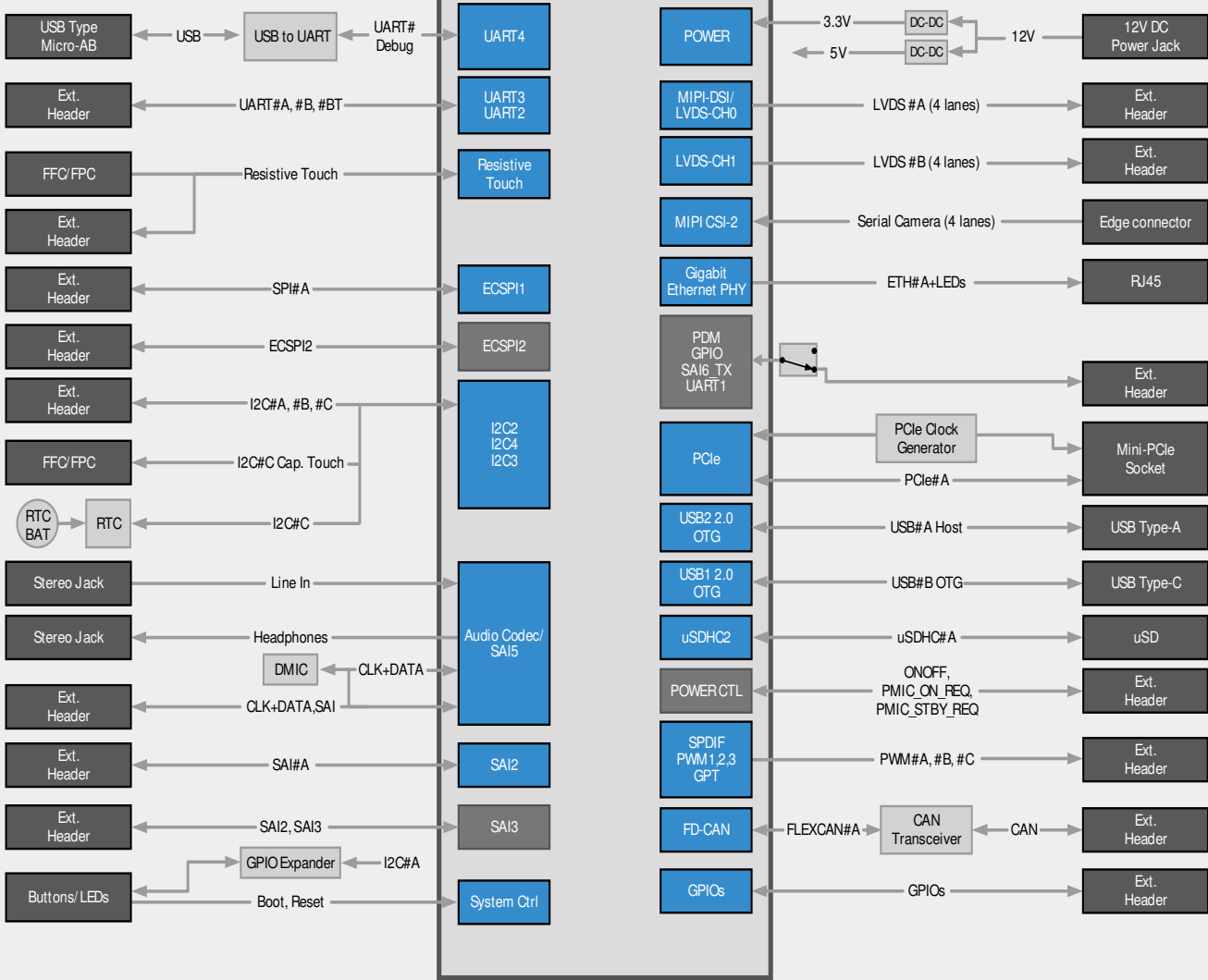
For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS" located at:
ftp://ftp.variscite.com/SOM_Compatibility

Title 14. Headers			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 12 of 24	

Symphony-Board

Doc rev 1.1

VAR-SOM-MX8M-MINI



Pin2pin with additional VAR-SOM products.
Please check pin-list document for details

Not Compatible



Title 02. Block Diagram VAR-SOM-MX8M-MINI			
Size A3	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 17 of 24	

04. VAR-SOM-MX8M-MINI Connector



PIN NAMING MNEMONICS:

- Prefix number of "/" denotes alternate function number; none is ALT0=PAD name
- Prefix denotes pin connected to a configurable module on SOM; E.g. with "EC" pin ENET_TD3////GPIO1_IO18*/ETH_TRX0_P source is Ethernet PHY
- Prefix points to an alternate function optionally used or shared on SOM; Verify with SOM datasheet before using this pin;

SETUP NOTES FOR VAR-SOM-MX8M-MINI:

ESP_ENET_SEL - Set to Header
Pin 71, 80 10v1 levels running from WCC_S22 set on SOM;

File 04. VAR-SOM-MX8M-MINI Connector

Size	Document Number	Project	Rev
A0	Symphony-Board	Symphony-Board	70_R1

Designer: Anand H. Approved By: _____
Date: Sunday, April 06, 2025 Sheet 18 of 24