01. Cover

VAR-SP8CustomBoard

Variscite

CONTENT

Disclaimer:

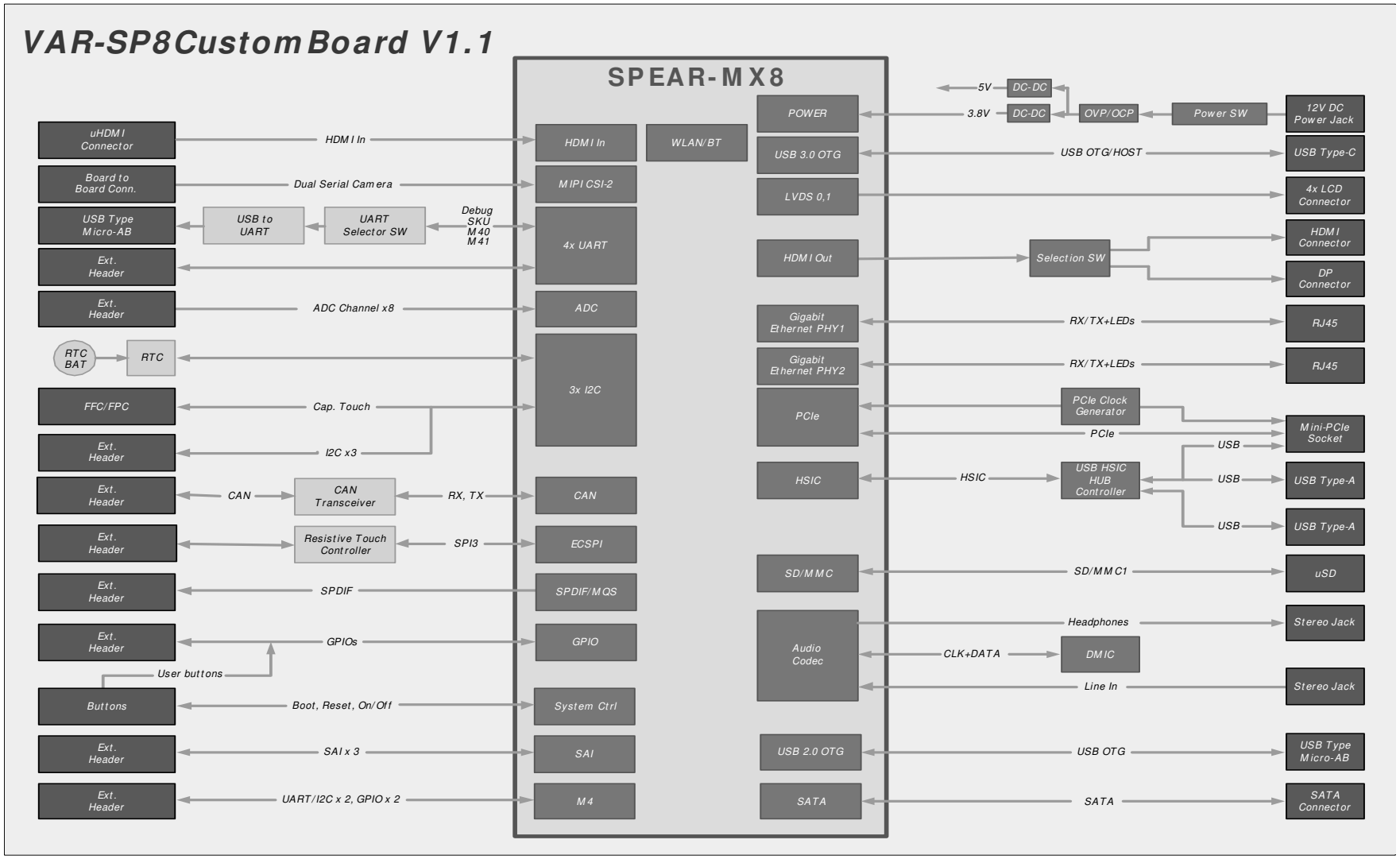
Revision History

Document	Carrier	
1.0	1.0	INITIAL
1.1	1.1	1) Power supplies changed to 12V in and 6A output 2) SOM power in pins were added in place of ground. 3) 2 Additional GPIO pins routed to MIPI-CSI2 edge connector
1.2	1.1A	1) RS422 RX_EN line routed to GPIO 2) Power Jack J43 changed to 2mm instead of 2.5mm
1.3	1.2	1) New layout. All previous changes implemented 2) Change SATA lines to 100 Ohms differential 3) M40_GPIO0_01 line moved to support PCI clock disable 4) HDMI_RX0_HPD pull up added 5) U31, U41 Note added.
1.4	1.3	1) U34 changed to PTN36043ABXY. 2) HDMI Out port section changed (replaced HDMI companion chip with simple ESD devices) 3) U31, U41 changed to FPF2193 4) R0402, C0402, TPD4EUSB30, SDC224-A Footprints changed 5) R0603, R1210, MHCI05030-6R8M-R8 Footprints changed 6) MA2SD290GL changed to BAS70JFILM 7) Q2 changed to TPS27081A 8) Optional resistor R92 Removed 9) R91 Changed to 49.9R 10) UART Selection table updated for easier understanding
1.5	1.3	1) J1.27, J1.29, J4.47 Pin names updated to correct GPIO number 2) ETH1 Bypass function names updated on J3 3) DSI_CLK_P and DSI_CLK_N swapped on J1 and J20
1.6	1.3	1) U34 changed to PTN36043BXY to reflect actual assembly 2) U34 EOL Note added
1.7	1.3A	1) HDMI_RX section is NC due to NXP PCN 202012002I 2) MLB section not supported due to NXP PCN 202012002I
1.8	1.3A	1) J3.20 & J3.22 pin names swapped to be consistent with the datasheet.

Variscite

Title: 01. Cover			
Size: A3	Document Number: VAR-SP8CustomBoard	Project: VAR-SP8CustomBoard	Rev: 1.3A
Designer: Leonid S.		Approved By:	
Date: Thursday, May 25, 2023		Sheet 1 of 15	

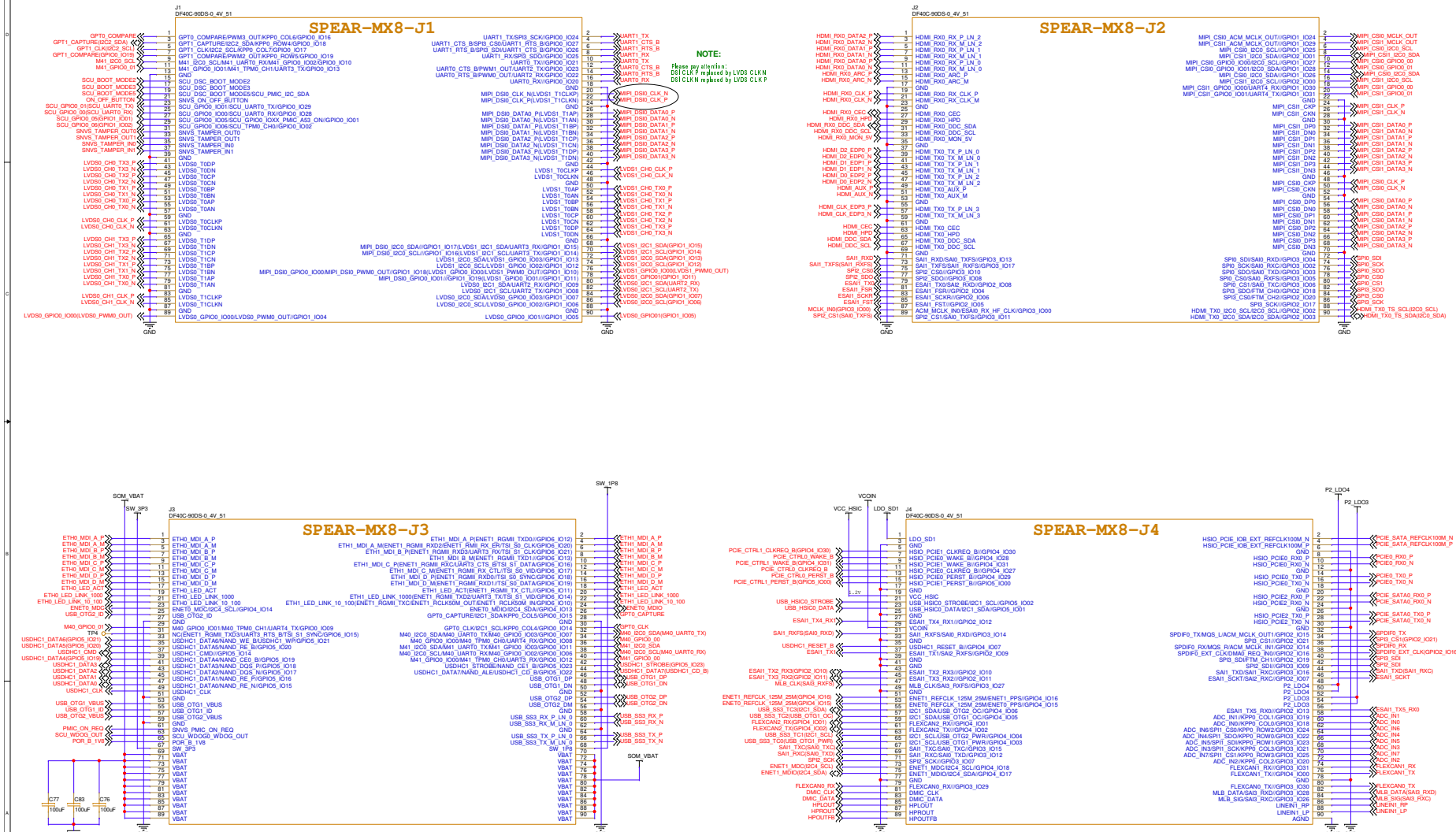
02. Block Diagram



Variscite

Title: 02. Block Diagram			
Size: A3	Document Number: VAR-SP8CustomBoard	Project: VAR-SP8CustomBoard	Rev: 1.3A
Designer: Leonid S.		Approved By:	
Date: Monday, January 25, 2021		Sheet 2 of 15	

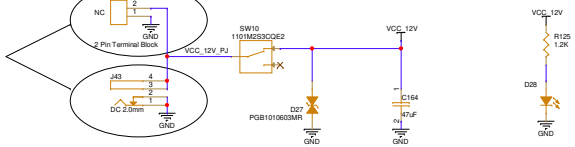
03.SPEAR-MX8



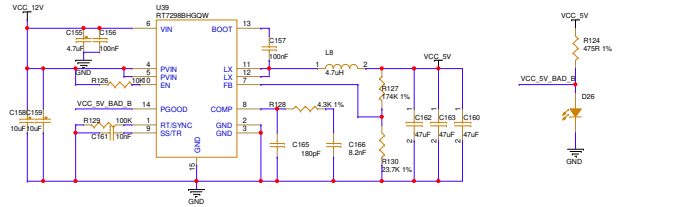
Title	03.SPEAR-MX8		
Size: A2	Document Number	Project	Rev: 1.3A
Designer:	Leopold S.	Approved By:	
Date:	Thursday, May 25, 2023	Sheet 3 of 15	

04. Power,Mechanics,RTC,Board ID

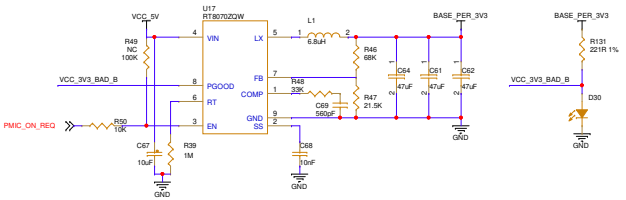
DC-IN - 12V



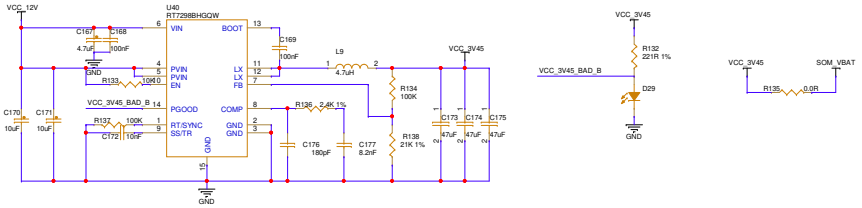
5V/6A FROM PWR JACK



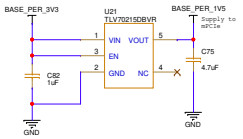
3.3V/3A FROM 5V BASE BOARD POWER



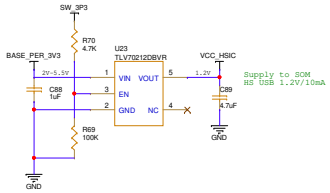
3.45V/6A FROM PWR JACK



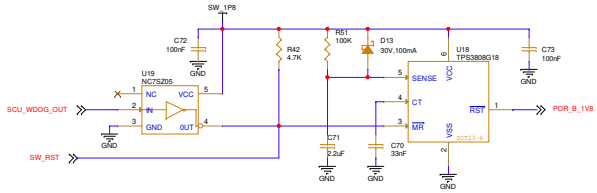
1.5V/0.3A BASE



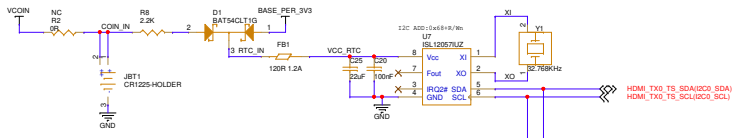
SOM VCC_HSIC



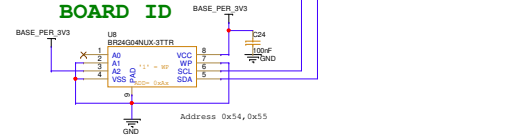
RESET & WATCHDOG



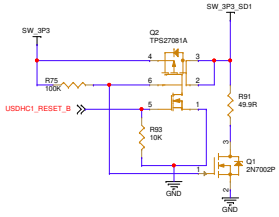
RTC BATTERY



BOARD ID



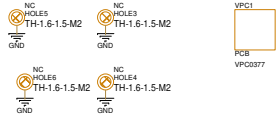
SD POWER



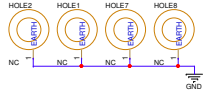
MECHANICS

SOM MOUNTING STANDOFF

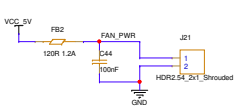
Place on TOP

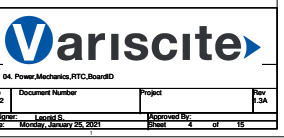


CHASSIS HOLES



FAN : 5V/0.2A

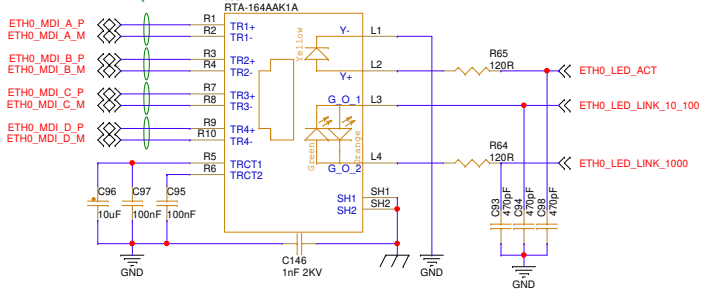




05. ETH, uSD, AUDIO,CAN,RS422

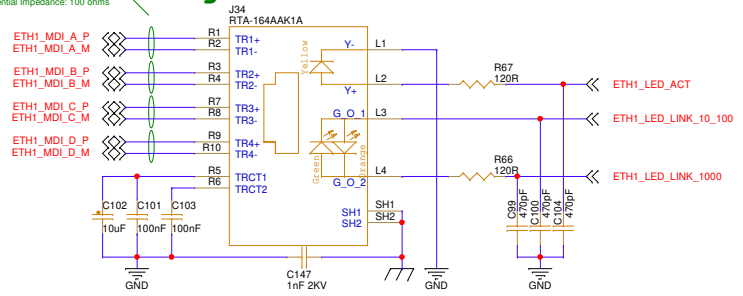
Gigabit Ethernet1

LAYOUT NOTE:
Giga Ethernet Differential Pair, Follow Giga Ethernet routing guidelines.
Differential Impedance: 100 ohms

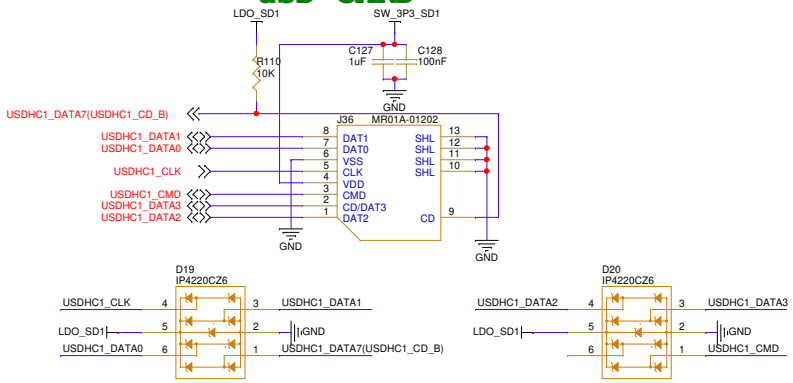


Gigabit Ethernet2

LAYOUT NOTE:
Giga Ethernet Differential Pair, Follow Giga Ethernet routing guidelines.
Differential Impedance: 100 ohms



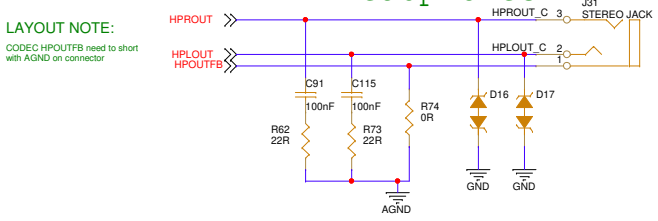
uSD CARD



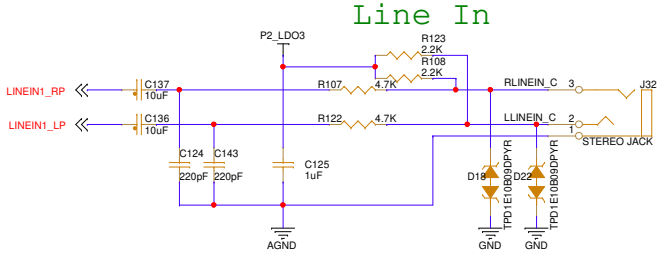
AUDIO

Headphones

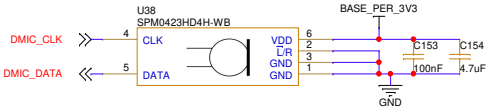
LAYOUT NOTE:
CODEC HPOUTFB need to short with AGND on connector



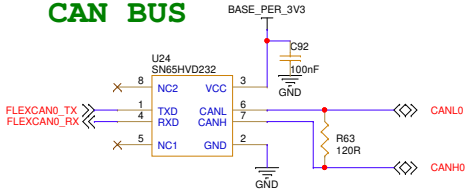
Line In



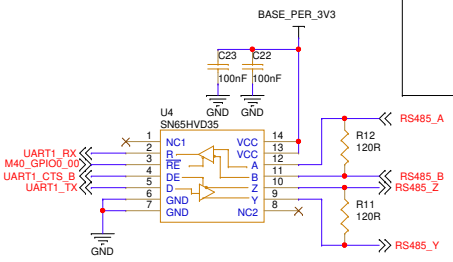
DIGITAL MIC



CAN BUS



RS-422 TRX

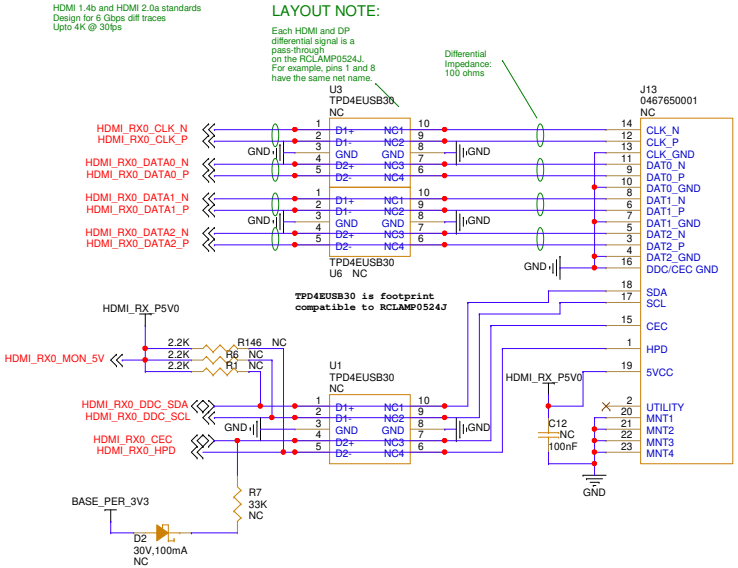


Variscite

Title: 05. ETH, uSD, AUDIO,CAN,RS422			
Size: A3	Document Number: VAR-SP8CustomBoard	Project: VAR-SP8CustomBoard	Rev: 1.3A
Designer: Leonid S.		Approved By:	
Date: Monday, January 25, 2021		Sheet 5 of 15	

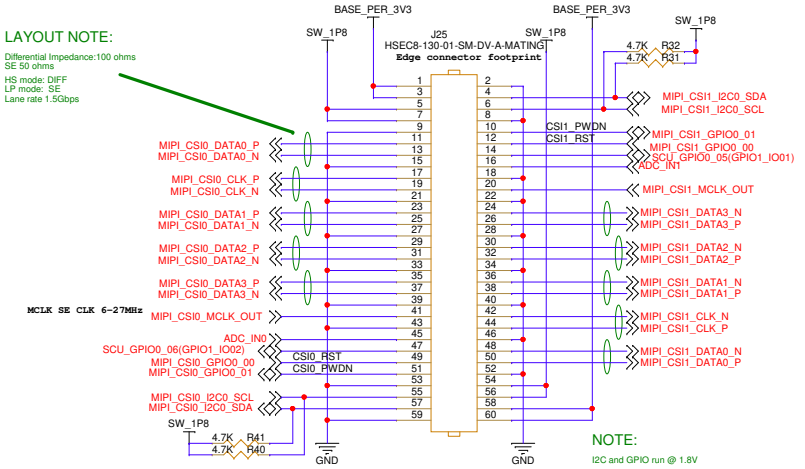
06. CAMERA, HDMI IN

uHDMI IN PORT
NOT SUPPORTED DUE TO NXP PCN 202012002I



MIPI-CSI0 + MIPI-CSI1

Connects to Variscite Custom MIPI-CSI2 Cam Board
Plug in 180deg to test second interface as 4 lanes



Variscite

Title: 06. CAMERA, HDMI IN			
Size: A3	Document Number: VAR-SP8CustomBoard	Project: VAR-SP8CustomBoard	Rev: 1.3A
Designer: Leonid S.		Approved By: Leonid S.	
Date: Monday, January 25, 2021		Sheet 6 of 15	

07. HDMI, eDP Out

DP PORT

LAYOUT NOTE:
Differential Impedance: 100 ohms

LAYOUT NOTE:
Differential Impedance: 100 ohms

BASE_PER_3V3

U10 TPD4E02B04
U11 TPD4E02B04
U12 TPD4E02B04

EDP_D0_P
EDP_D0_N
EDP_D1_P
EDP_D1_N
EDP_D2_P
EDP_D2_N
EDP_D3_P
EDP_D3_N
EDP_AUX_P
EDP_AUX_N
EDP_HPD

R147 100K
C56 100nF
C50 100nF
C48 100nF
R27 1M
R25 1M

CONFIG1
CONFIG2

J22 DP1RD20JQ1R400
LANE 0 _P
GND
LANE 0 _N
LANE 1 _P
GND
LANE 1 _N
LANE 2 _P
GND
LANE 2 _N
LANE 3 _P
GND
LANE 3 _N
CONFIG1
CONFIG2
AUX CH _P
GND
AUX CH _N
HOT PLUG_DET
3.3V RETURN
3.3V
MECH1
MECH2
MECH3
MECH4

HDMI/eDP/DP SWITCH

BASE_PER_3V3

C47 1uF
C39 100nF
C49 100nF
R24 100K

LAYOUT NOTE:
Differential Impedance: 100 ohms

U9 PI3WVR12412ZHE

VDD3
VDD2
VDD1
GND1
GND2
GND3
GND_EP

D0+A
D0-A
D1+A
D1-A
D2+A
D2-A
D3+A
D3-A
SCL_A/AUX+_A
SDA_A/AUX-_A
HPD_A

D0+B
D0-B
D1+B
D1-B
D2+B
D2-B
D3+B
D3-B
SCL_B/AUX+_B
SDA_B/AUX-_B
HPD_B

HDMI_D2_EDP0_P
HDMI_D2_EDP0_N
HDMI_D1_EDP1_P
HDMI_D1_EDP1_N
HDMI_D0_EDP2_P
HDMI_D0_EDP2_N
HDMI_CLK_EDP3_P
HDMI_CLK_EDP3_N
HDMI_AUX_N
HDMI_AUX_P
PCIE_CTRL0_CLKREQ_B
HDMI_HPD

C27 100nF HDMID2_EDP0_P
C26 100nF HDMID2_EDP0_N
C36 100nF HDMID1_EDP1_P
C35 100nF HDMID1_EDP1_N
C38 100nF HDMID0_EDP2_P
C37 100nF HDMID0_EDP2_N
C46 100nF HDMICLK_EDP3_P
C45 100nF HDMICLK_EDP3_N

D0+
D0-
D1+
D1-
D2+
D2-
D3+
D3-
SDA/AUX-
SCL/AUX+
DDC/AUX_HPD_SEL
GPU_SEL
HPD
OE

LAYOUT NOTE:
Differential Impedance: 100 ohms

R15 R14 R17 R16 R21 R20 R23 R22 R148
604R 604R 604R 604R 604R 604R 604R 604R 1M

C186 1uF

Note : HDMI pull down must not be applied until VDD_PHY_1V8 is up.
Implemtation uses fact that BASE_PER_3V3 rises after all SOM power rails are up.
At boot time GPIO drives U57 switch to A state.

IMPORTANT:
Please pay attention:
DP Lane 0 is HDMI Lane 2
DP Lane 2 is HDMI Lane 0

HDMI OUT PORT

HDMI_5V_CON

R151 2.2K
R150 2.2K

LAYOUT NOTE:
Differential Impedance: 100 ohms

U43 TPD4E02B04
U44 TPD4E02B04
U45 TPD4E02B04

HDMI_D2_P
HDMI_D2_N
HDMI_D1_P
HDMI_D1_N
HDMI_D0_P
HDMI_D0_N
HDMI_CK_P
HDMI_CK_N
HDMI_DDC_SCL
HDMI_DDC_SDA
HDMI_CEC
HDMI_HPD_CON
HDMI_UTIL_CON

J19 HDMI CONN
+5V
DAT2+
DAT2-
DAT1+
DAT1-
DAT0+
DAT0-
CLK+
CLK-
SCL
SDA
CEC
DDC/CEC GND
DET
NC
SHLD
DAT2_S
DAT1_S
DAT0_S
CLK_S
MTG1
MTG2
MTG3
MTG4

C28 2.2uF

D34 TPD1E10B09DPYR
D35 TPD1E10B09DPYR

HDMI POWER

BASE_PER_3V3

D33 30V,100mA
R152 27K

HDMI_CEC
HDMI_DDC_SCL
HDMI_DDC_SDA

VCC_5V
HDMI_5V_CON

U42 FPF2193
B2 A2 Vin EN GND C2
Vout FLAG Iset B1 A1 C1

C187 1uF
C185 100nF
R149 4.7K

Current Limit Typ 0.117A

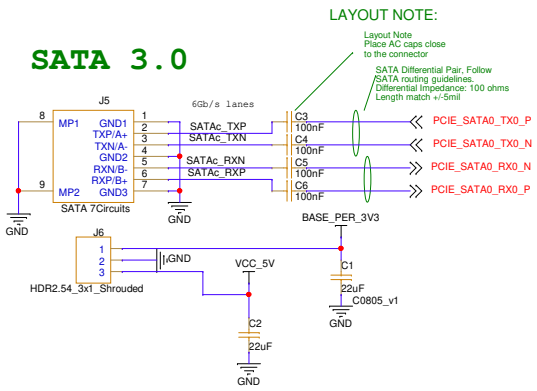
GND

Variscite

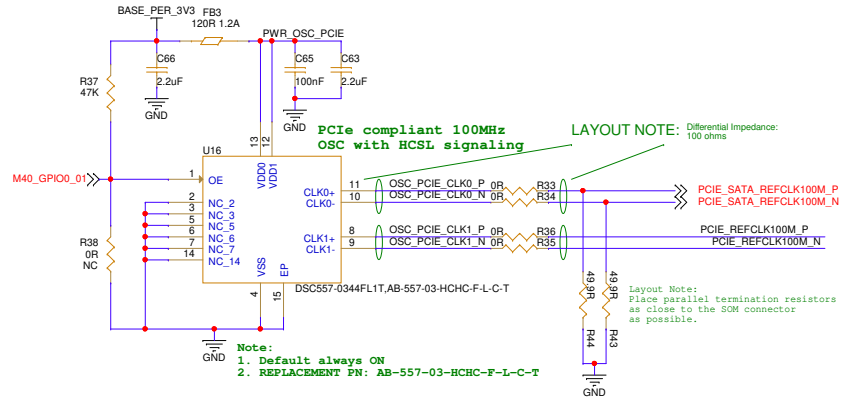
Title	07. HDMI, eDP Out		
Size A3	Document Number VAR-SP8CustomBoard	Project VAR-SP8CustomBoard	Rev 1.3A
Designer: Leonid S.		Approved By: Leonid S.	
Date: Monday, January 25, 2021		Sheet 7 of 15	

08. PCIe, uSATA

SATA 3.0

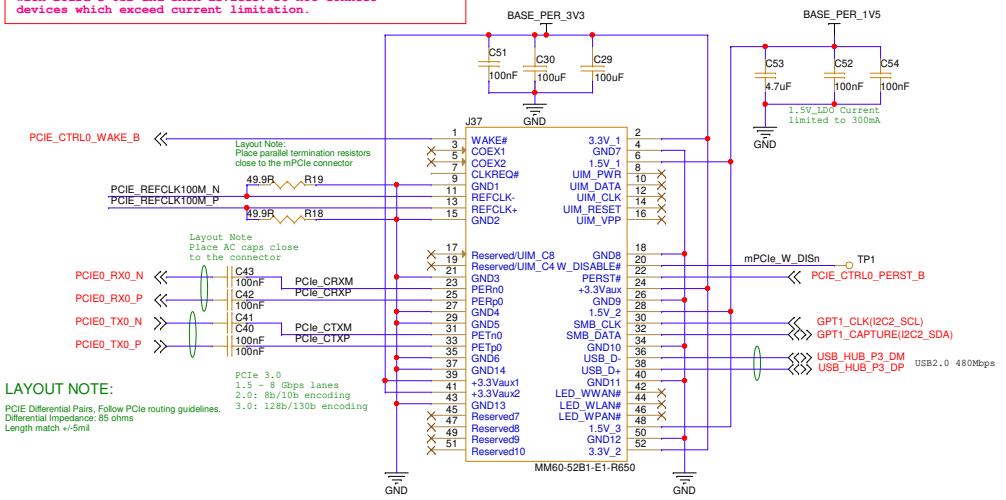


PCIe CLK DIST.



mPCIexp

Customboard 5V power supply is limited to 3A, shared with Board's USB and SATA devices. Do not connect devices which exceed current limitation.

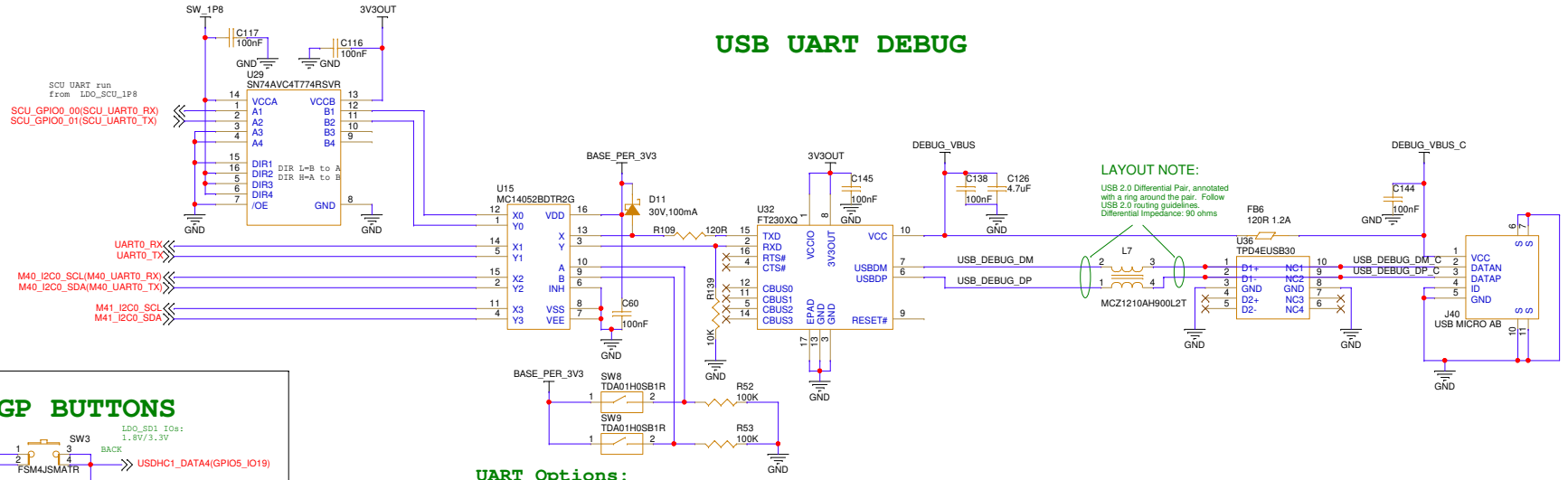


Variscite

Title: 08. PCIe, uSATA			
Size: A3	Document Number: VAR-SP8CustomBoard	Project:	Rev: 1.3A
Designer: Leonid S.		Approved By: Leonid S.	
Date: Monday, January 25, 2021		Sheet 8 of 15	

09. DEBUG UART, BOOT, LEDs, SWs

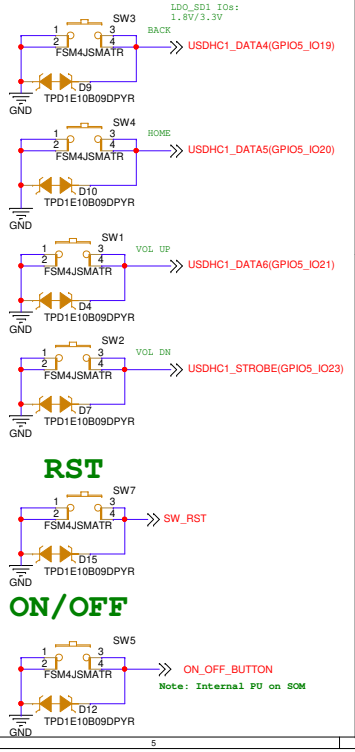
USB UART DEBUG



UART Options:

SW9	SW8	
OFF	OFF	SKU Uart
OFF	ON	DEBUG Uart
ON	OFF	M4 – 1 Uart
ON	ON	M4 – 2 Uart

GP BUTTONS



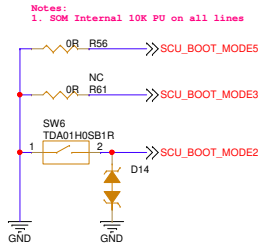
RST

ON/OFF

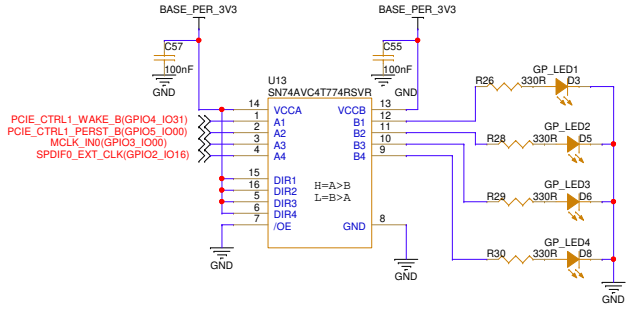
SOM BOOTSTRP

Boot Options:
(bit order 5-3-2)

0-0-0	: Fuse
0-0-1	: Serial
0-1-0	: eMMC
0-1-1	: SD
1-0-0	: SATA



GP LEDS

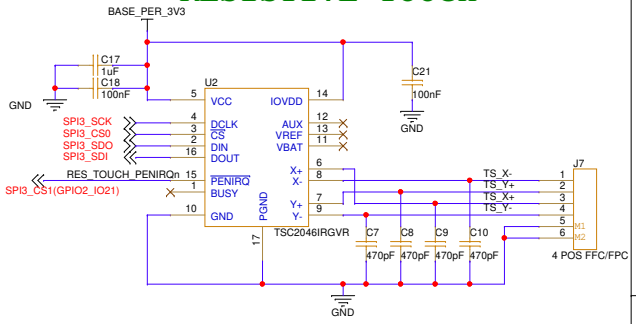


Variscite

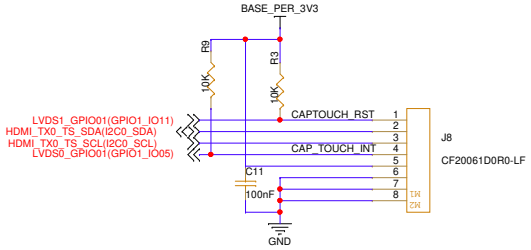
Title: 09. DEBUG UART, BOOT, LEDs, SWs			
Size: A3	Document Number: VAR-SP8CustomBoard	Project:	Rev: 1.3A
Designer: Leonid S.		Approved By: Leonid S.	
Date: Monday, January 25, 2021		Sheet 9 of 15	

10. LVDS, TOUCH

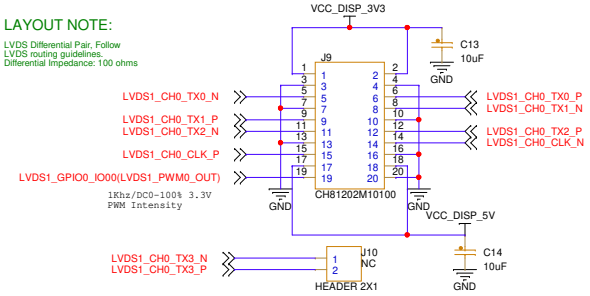
RESISTIVE TOUCH



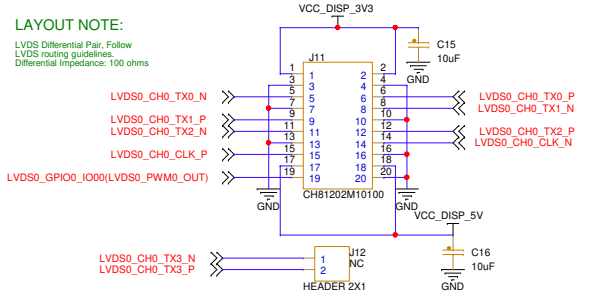
CAPACITIVE TOUCH



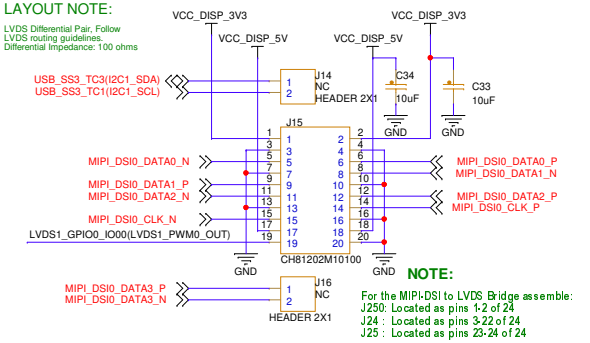
LVDS DISPLAY1 CH0



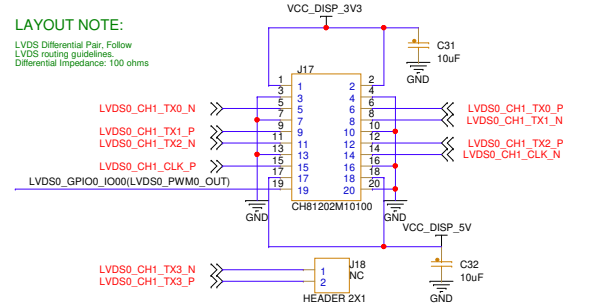
LVDS DISPLAY0 CH0



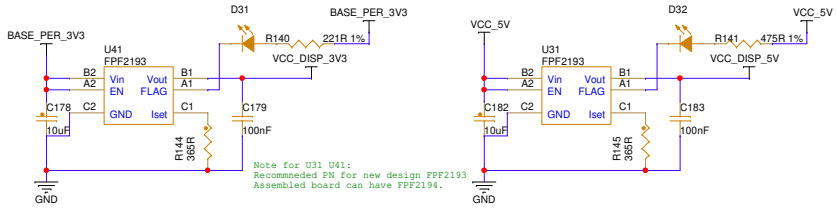
MIPI DSI DISPLAY



LVDS DISPLAY0 CH1



Short circuit protection



Remarks

LVDS CAN BE MUX'd VIA RES SEL WITH DSI CHANNELS Lane rate: 80 Mbps to 1.5 Gbps

LVDS display running w/3 lanes referred as miniLVDS

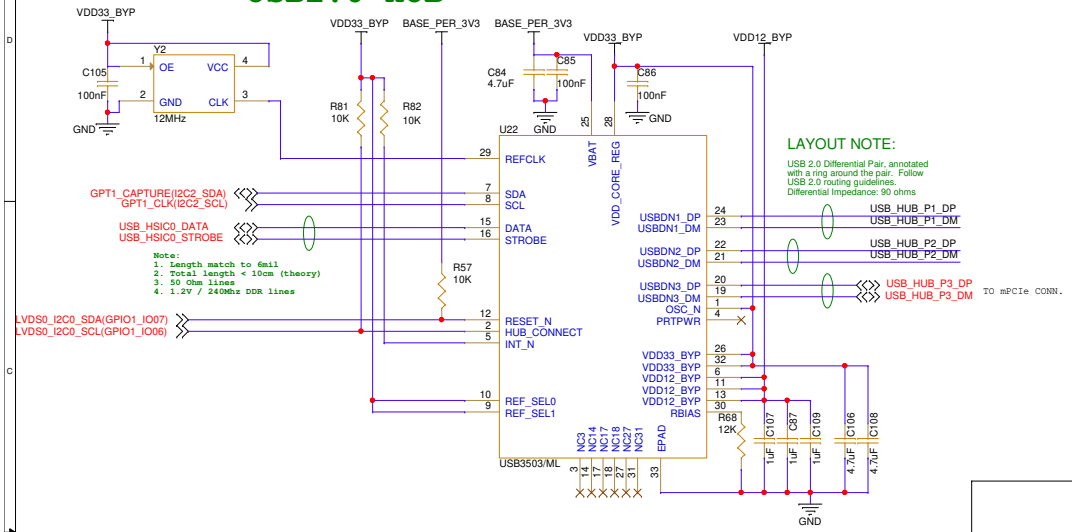
LCD: GKTW70SDAE4SE 5V/0.45A 3.3V/0.17A

Variscite

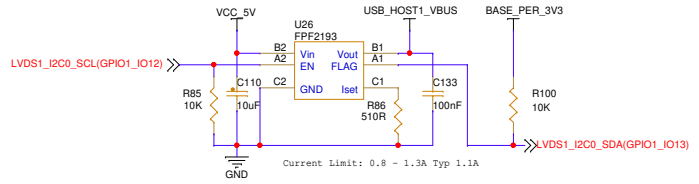
Title: 10. LVDS, TOUCH			
Size: A3	Document Number: VAR-SP8CustomBoard	Project: VAR-SP8CustomBoard	Rev: 1.3A
Designer: Leonid S.		Approved By:	
Date: Monday, January 25, 2021		Sheet 10 of 15	

11. USB 2 HOST, USB 2 OTG

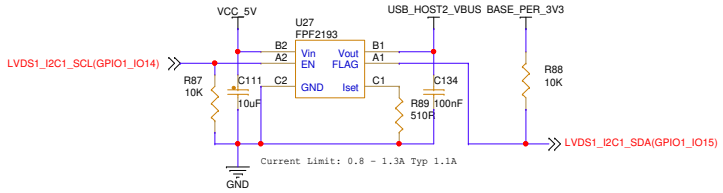
USB2.0 HUB



USB HOST1 PWR

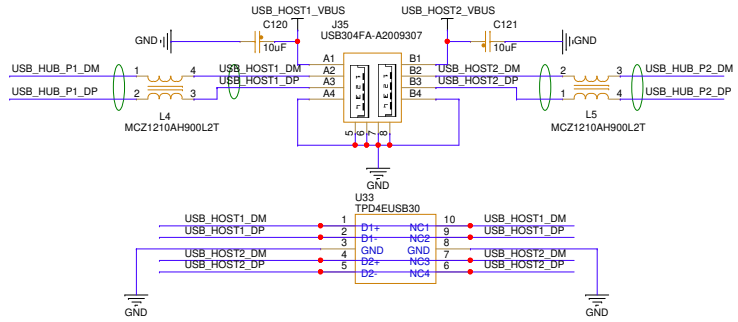


USB HOST2 PWR

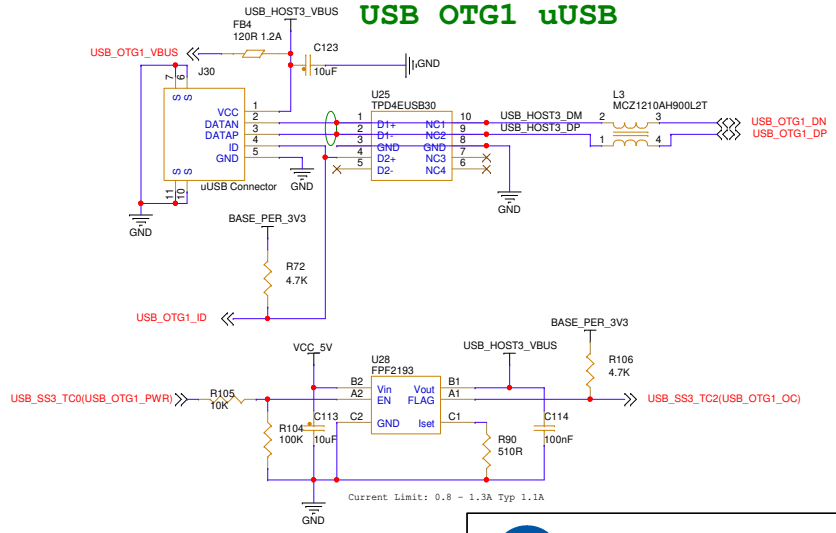


USB HOST1

USB HOST2



USB OTG1 uUSB

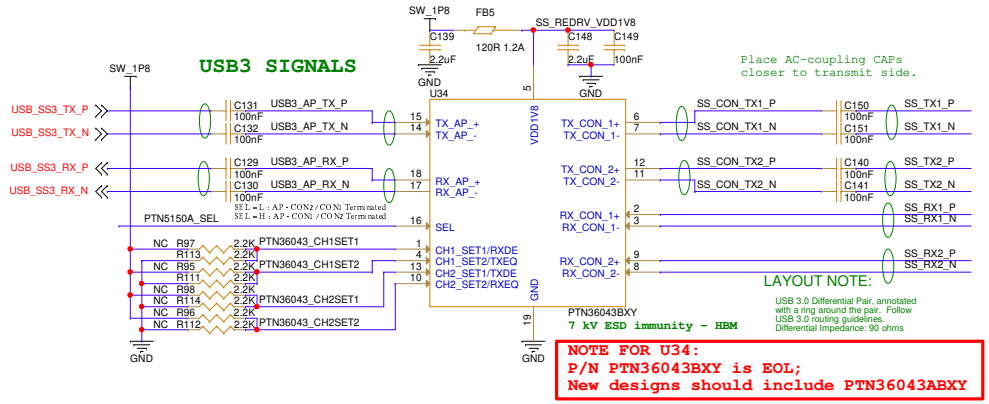


Variscite

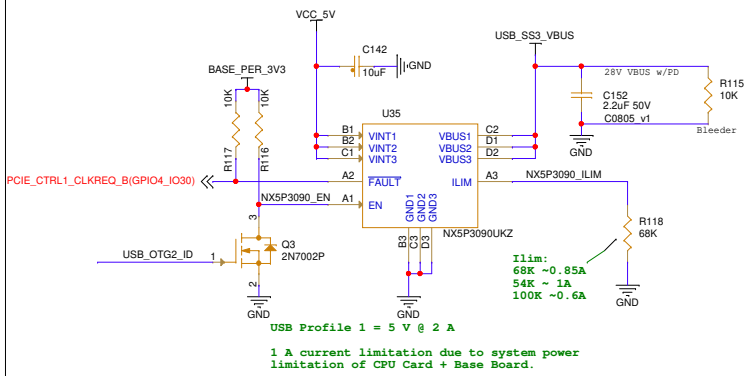
Title: 11. USB 2 HOST, USB 2 OTG			
Size: A3	Document Number: VAR-SP8CustomBoard	Project: VAR-SP8CustomBoard	Rev: 1.3A
Designer: Leonid S.		Approved By:	
Date: Monday, January 25, 2021		Sheet 11 of 15	

12. USB 3

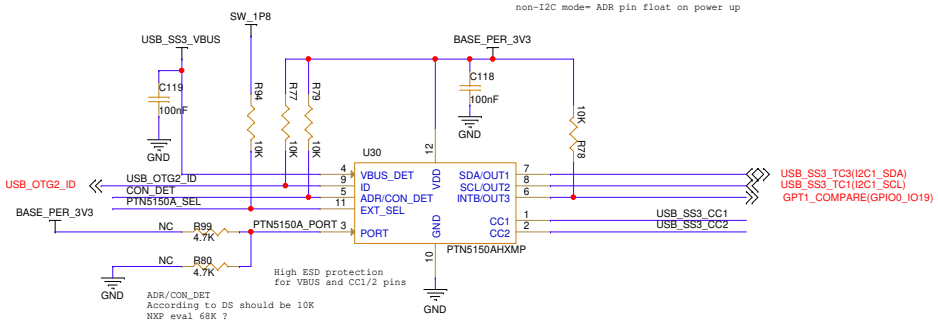
USB TYPE C CIRCUITRY



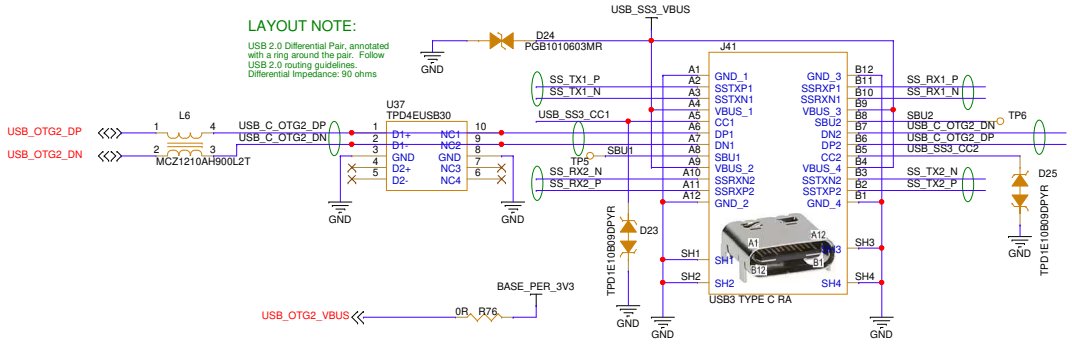
5V Source Load Switch



Config Channel Logic Detection & Indication of Plug Orientation



USB TYPE C

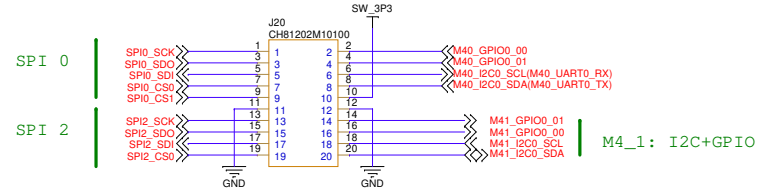


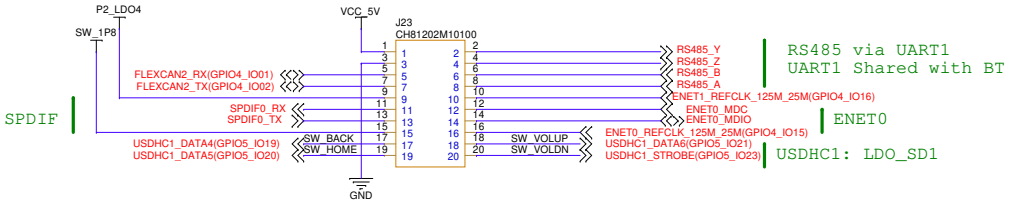
Variscite

Title: 12. USB 3			
Size: A3	Document Number: VAR-SP8CustomBoard	Project: VAR-SP8CustomBoard	Rev: 1.3A
Designer: Leonid S.		Approved By:	
Date: Monday, January 25, 2021		Sheet 12 of 15	

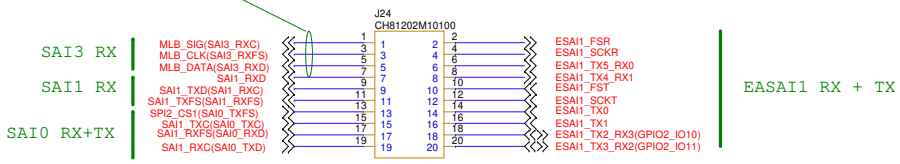
13. Headers

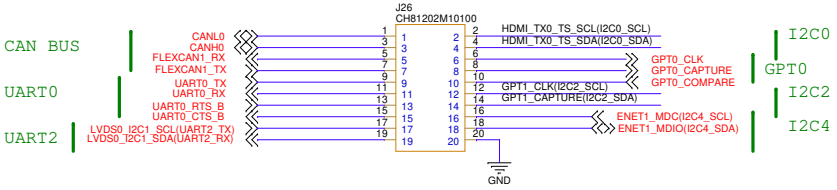
3.3V HEADERS



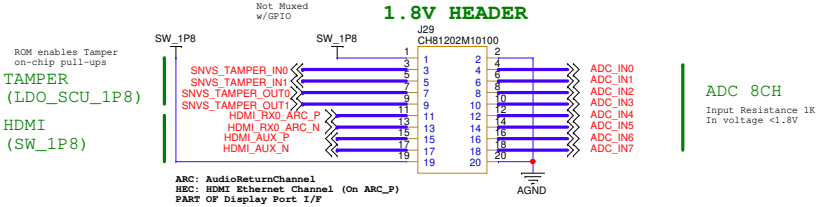


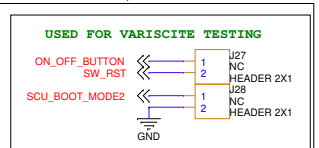
MLB NOT SUPPORTED
DUE TO NXP PCN 202012002I

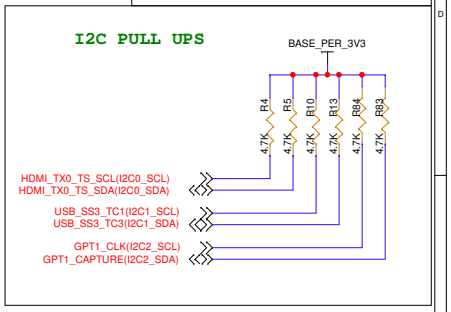




1.8V HEADER







Variscite

Title: 13. Headers			
Size: A3	Document Number: VAR-SP8CustomBoard	Project: VAR-SP8CustomBoard	Rev: 1.3A
Designer: Leonid S.		Approved By:	
Date: Monday, January 25, 2021		Sheet 13 of 15	

14. PINMUX J1 & J2

	ALT0	ALT1	ALT2	ALT3	CB_FUNCTION	
GPT0_COMPARE	LSIO.GPT0.COMPARE	LSIO.PWM3.OUT	LSIO.GPIO0.IO16	LSIO.KPP0.COL6		SOM J1
GPT1_CLK(I2C2_SCL)	LSIO.GPT1.CLK	DMA.I2C2.SCL	LSIO.KPP0.COL7	LSIO.GPIO0.IO17		
GPT1_COMPARE(GPIO0_IO19)	LSIO.GPT1.COMPARE	LSIO.PWM2.OUT	LSIO.KPP0.ROW5	LSIO.GPIO0.IO19		
M41_I2C0_SCL	M41.I2C0.SCL	M41.UART0.RX	M41.GPIO0.IO02	LSIO.GPIO0.IO10		
M41_GPIO0_01	M41.GPIO0.IO01	M41.TPM0.CH1	DMA.UART3.TX	LSIO.GPIO0.IO13		
GPT1_CAPTURE(I2C2_SDA)	LSIO.GPT1.CAPTURE	DMA.I2C2.SDA	LSIO.KPP0.ROW4	LSIO.GPIO0.IO18		
SCU_BOOT_MODE5	SCU.DSC.BOOT.MODE5	SCU.PMIC.I2C.SDA				
SCU_GPIO0_01(SCU_UART0_TX)	SCU.GPIO0.IO01	SCU.UART0.TX		LSIO.GPIO0.IO29		
SCU_GPIO0_00(SCU_UART0_RX)	SCU.GPIO0.IO00	SCU.UART0.RX		LSIO.GPIO0.IO28		
SCU_GPIO0_05(GPIO1_IO01)	SCU.GPIO0.IO05	SCU.GPIO0.IOXX.PMIC.A53.ON		LSIO.GPIO1.IO01		
SCU_GPIO0_06(GPIO1_IO02)	SCU.GPIO0.IO06	SCU.TPM0.CH0		LSIO.GPIO1.IO02		
UART1_TX	DMA.UART1.TX	DMA.SPI3.SCK		LSIO.GPIO0.IO24		
UART1_CTS_B	DMA.UART1.CTS.B	DMA.SPI3.CS0	DMA.UART1.RTS.B	LSIO.GPIO0.IO27		
UART1_RTS_B	DMA.UART1.RTS.B	DMA.SPI3.SDI	DMA.UART1.CTS.B	LSIO.GPIO0.IO26		
UART1_RX	DMA.UART1.RX	DMA.SPI3.SDO		LSIO.GPIO0.IO25		
UART0_TX	DMA.UART0.TX			LSIO.GPIO0.IO21		
UART0_CTS_B	DMA.UART0.CTS.B	LSIO.PWM1.OUT	DMA.UART2.TX	LSIO.GPIO0.IO23		
UART0_RTS_B	DMA.UART0.RTS.B	LSIO.PWM0.OUT	DMA.UART2.RX	LSIO.GPIO0.IO22		
UART0_RX	DMA.UART0.RX			LSIO.GPIO0.IO20		
LVDS1_I2C1_SDA(GPIO1_IO15)	LVDS1.I2C1.SDA	DMA.UART3.RX		LSIO.GPIO1.IO15	USB_HOST2_OCSn	
LVDS1_I2C1_SCL(GPIO1_IO14)	LVDS1.I2C1.SCL	DMA.UART3.TX		LSIO.GPIO1.IO14	USB_HOST2_PWR_EN	
LVDS1_I2C0_SDA(GPIO1_IO13)	LVDS1.I2C0.SDA	LVDS1.GPIO0.IO03		LSIO.GPIO1.IO13	USB_HOST1_OCSn	
LVDS1_I2C0_SCL(GPIO1_IO12)	LVDS1.I2C0.SCL	LVDS1.GPIO0.IO02		LSIO.GPIO1.IO12	USB_HOST1_PWR_EN	
LVDS1_GPIO0_IO00(LVDS1_PWM0_OUT)	LVDS1.GPIO0.IO00	LVDS1.PWM0.OUT		LSIO.GPIO1.IO10		
LVDS1_GPIO01(GPIO1_IO11)	LVDS1.GPIO0.IO01			LSIO.GPIO1.IO11	CAPTOUCH_RST	
LVDS0_I2C1_SDA(UART2_RX)	LVDS0.I2C1.SDA	DMA.UART2.RX		LSIO.GPIO1.IO09		
LVDS0_I2C1_SCL(UART2_TX)	LVDS0.I2C1.SCL	DMA.UART2.TX		LSIO.GPIO1.IO08		
LVDS0_I2C0_SDA(GPIO1_IO07)	LVDS0.I2C0.SDA	LVDS0.GPIO0.IO03		LSIO.GPIO1.IO07	USB_HUB_RESET_N	
LVDS0_I2C0_SCL(GPIO1_IO06)	LVDS0.I2C0.SCL	LVDS0.GPIO0.IO02		LSIO.GPIO1.IO06	USB_HUB_CONNECT	
LVDS0_GPIO01(GPIO1_IO05)	LVDS0.GPIO0.IO01			LSIO.GPIO1.IO05	CAP_TOUCH_INT	
LVDS0_GPIO0_IO00(LVDS0_PWM0_OUT)	LVDS0.GPIO0.IO00	LVDS0.PWM0.OUT		LSIO.GPIO1.IO04		
SAI1_RXD	AUD.SAI1.RXD	AUD.SAI0.TXFS		LSIO.GPIO3.IO13		SOM J2
SAI1_TXFS(SAI1_RXFS)	AUD.SAI1.TXFS	AUD.SAI1.RXFS		LSIO.GPIO3.IO17		
SPI2_CS0	DMA.SPI2.CS0			LSIO.GPIO3.IO10		
SPI2_SDO	DMA.SPI2.SDO			LSIO.GPIO3.IO08		
ESAI1_TX0	AUD.ESAI1.TX0	AUD.SAI2.RXD		LSIO.GPIO2.IO08		
ESAI1_FSR	AUD.ESAI1.FSR			LSIO.GPIO2.IO04		
ESAI1_SCKR	AUD.ESAI1.SCKR			LSIO.GPIO2.IO06		
ESAI1_FST	AUD.ESAI1.FST			LSIO.GPIO2.IO05		
SPI2_CS1(SAI0_TXFS)	DMA.SPI2.CS1	AUD.SAI0.TXFS		LSIO.GPIO3.IO11		
MCLK_IN0(GPIO3_IO00)	AUD.ACM.MCLK.IN0	AUD.ESAI0.RX.HF.CLK		LSIO.GPIO3.IO00	GP_LED3	
MIPI_CSI0_MCLK_OUT	MIPI.CSI0.ACM.MCLK.OUT			LSIO.GPIO1.IO24		
MIPI_CSI1_MCLK_OUT	MIPI.CSI1.ACM.MCLK.OUT			LSIO.GPIO1.IO29		
MIPI_CSI0_I2C0_SCL	MIPI.CSI0.I2C0.SCL			LSIO.GPIO1.IO25		
MIPI_CSI1_I2C0_SDA	MIPI.CSI1.I2C0.SDA			LSIO.GPIO2.IO01		
MIPI_CSI0_GPIO0_00	MIPI.CSI0.GPIO0.IO00	DMA.I2C0.SCL		LSIO.GPIO1.IO27	CSI0_RST	
MIPI_CSI0_GPIO0_01	MIPI.CSI0.GPIO0.IO01	DMA.I2C0.SDA		LSIO.GPIO1.IO28	CSI0_PWDN	
MIPI_CSI0_I2C0_SDA	MIPI.CSI0.I2C0.SDA			LSIO.GPIO1.IO26		
MIPI_CSI1_I2C0_SCL	MIPI.CSI1.I2C0.SCL			LSIO.GPIO2.IO00		
MIPI_CSI1_GPIO0_00	MIPI.CSI1.GPIO0.IO00	DMA.UART4.RX		LSIO.GPIO1.IO30	CSI1_RST	
MIPI_CSI1_GPIO0_01	MIPI.CSI1.GPIO0.IO01	DMA.UART4.TX		LSIO.GPIO1.IO31	CSI1_PWDN	
SPI0_SDI	DMA.SPI0.SDI	AUD.SAI0.RXD		LSIO.GPIO3.IO04		
SPI0_SCK	DMA.SPI0.SCK	AUD.SAI0.RXC		LSIO.GPIO3.IO02		
SPI0_SDO	DMA.SPI0.SDO	AUD.SAI0.TXD		LSIO.GPIO3.IO03		
SPI0_CS0	DMA.SPI0.CS0	AUD.SAI0.RXFS		LSIO.GPIO3.IO05		
SPI0_CS1	DMA.SPI0.CS1	AUD.SAI0.TXC		LSIO.GPIO3.IO06		
SPI3_SDO	DMA.SPI3.SDO	DMA.FTM.CH0		LSIO.GPIO2.IO18	RES_TOUCH_SPI	
SPI3_CS0	DMA.SPI3.CS0	DMA.FTM.CH2		LSIO.GPIO2.IO20	RES_TOUCH_SPI	
SPI3_SCK	DMA.SPI3.SCK			LSIO.GPIO2.IO17	RES_TOUCH_SPI	
HDMI_TX0_TS_SCL(I2C0_SCL)	HDMI.TX0.I2C0.SCL	DMA.I2C0.SCL		LSIO.GPIO2.IO02		
HDMI_TX0_TS_SDA(I2C0_SDA)	HDMI.TX0.I2C0.SDA	DMA.I2C0.SDA		LSIO.GPIO2.IO03		

Variscite

Title: 14. PINMUX J1 & J2			
Size: A3	Document Number: VAR-SP8CustomBoard	Project: VAR-SP8CustomBoard	Rev: 1.3A
Designer: Leonid S.		Approved By:	
Date: Monday, January 25, 2021		Sheet 14 of 15	

15. PINMUX J3 & J4

	ALT0	ALT1	ALT2	ALT3	CB_FUNCTION	
ENET0_MDC	ENET0.MDC	DMA.I2C4.S		LSIO.GPIO4.IO14		SOM J3
M40_GPIO0_01	M40.GPIO0.IO01	M40.TPM0.CH1	DMA.UART4.TX	LSIO.GPIO0.IO09		
USDHC1_CMD	USDHC1.CMD			LSIO.GPIO5.IO14		
USDHC1_DATA0	USDHC1.DATA0	NAND.RE.N		LSIO.GPIO5.IO15		
USDHC1_DATA1	USDHC1.DATA1	NAND.RE.P		LSIO.GPIO5.IO16		
USDHC1_DATA2	USDHC1.DATA2	NAND.DQS.N		LSIO.GPIO5.IO17		
USDHC1_DATA3	USDHC1.DATA3	NAND.DQS.P		LSIO.GPIO5.IO18		
USDHC1_DATA4(GPIO5_IO19)	USDHC1.DATA4	NAND.CE0.B		LSIO.GPIO5.IO19	SW_BACK	
USDHC1_DATA5(GPIO5_IO20)	USDHC1.DATA5	NAND.RE.B		LSIO.GPIO5.IO20	SW_HOME	
USDHC1_DATA6(GPIO5_IO21)	USDHC1.DATA6	NAND.WE.B	USDHC1.WP	LSIO.GPIO5.IO21	SW_VOLUP	
	CONN.ENET0.MDIO	DMA.I2C4.SDA		LSIO.GPIO4.IO13		
ENET0_MDIO	LSIO.GPT0.CAPTURE	DMA.I2C1.SDA	LSIO.KPP0.COL5	LSIO.GPIO0.IO15		
GPT0_CAPTURE	LSIO.GPT0.CLK	DMA.I2C1.SCL	LSIO.KPP0.COL4	LSIO.GPIO0.IO14		
GPT0_CLK	M40.I2C0.SDA	M40.UART0.TX	M40.GPIO0.IO03	LSIO.GPIO0.IO07		
M40_I2C0_SDA(M40_UART0_TX)	M40.GPIO0.IO00	M40.TPM0.CH0	DMA.UART4.RX	LSIO.GPIO0.IO08		
M40_GPIO0_00	M41.I2C0.SDA	M41.UART0.TX	M41.GPIO0.IO03	LSIO.GPIO0.IO11		
M41_I2C0_SDA	M40.I2C0.SCL	M40.UART0.RX	M40.GPIO0.IO02	LSIO.GPIO0.IO06		
M40_I2C0_SCL(M40_UART0_RX)	M41.GPIO0.IO00	M41.TPM0.CH0	DMA.UART3.RX	LSIO.GPIO0.IO12		
M41_GPIO0_00	CONN.USDHC1.STROBE	CONN.NAND.CE1.B		LSIO.GPIO5.IO23	SW_VOLDN	
USDHC1_STROBE(GPIO5_IO23)	CONN.USDHC1.DATA7	CONN.NAND.ALE	CONN.USDHC1.CD.B	LSIO.GPIO5.IO22		
USDHC1_DATA7(USDHC1_CD_B)						
SPDIF0_TX	AUD.SPDIF0.TX	AUD.MQS.L	AUD.ACM.MCLK.OUT1	LSIO.GPIO2.IO15		SOM J4
SPI3_CS1(GPIO2_IO21)	DMA.SPI3.CS1			LSIO.GPIO2.IO21	RES_TOUCH_PENIRQn	
SPDIF0_RX	AUD.SPDIF0.RX	AUD.MQS.R	AUD.ACM.MCLK.IN1	LSIO.GPIO2.IO14		
SPDIF0_EXT_CLK(GPIO2_IO16)	AUD.SPDIF0.EXT.CLK	DMA.DMA0.REQ.IN0		LSIO.GPIO2.IO16	GP_LED4	
SPI3_SDI	DMA.SPI3.SDI	DMA.FTM.CH1		LSIO.GPIO2.IO19	RES_TOUCH_SPI	
SPI2_SDI	DMA.SPI2.SDI			LSIO.GPIO3.IO09		
SAI1_TXD(SAI1_RXC)	AUD.SAI1.TXD	AUD.SAI1.RXC		LSIO.GPIO3.IO16		
ESAI1_SCKT	AUD.ESAI1.SCKT	AUD.SAI2.RXC		LSIO.GPIO2.IO07		
	AUD.ESAI1.TX5.RX0			LSIO.GPIO2.IO13		
ESAI1_TX5_RX0	DMA.ADC.IN1		LSIO.KPP0.COL1	LSIO.GPIO3.IO19		
ADC_IN1	DMA.ADC.IN0		LSIO.KPP0.COL0	LSIO.GPIO3.IO18		
ADC_IN0	DMA.ADC.IN6	DMA.SPI1.CS0	LSIO.KPP0.ROW2	LSIO.GPIO3.IO24		
ADC_IN6	DMA.ADC.IN4	DMA.SPI1.SDO	LSIO.KPP0.ROW0	LSIO.GPIO3.IO22		
ADC_IN4	DMA.ADC.IN5	DMA.SPI1.SDI	LSIO.KPP0.ROW1	LSIO.GPIO3.IO23		
ADC_IN5	DMA.ADC.IN3	DMA.SPI1.SCK	LSIO.KPP0.COL3	LSIO.GPIO3.IO21		
ADC_IN3	DMA.ADC.IN7	DMA.SPI1.CS1	LSIO.KPP0.ROW3	LSIO.GPIO3.IO25		
ADC_IN7	DMA.ADC.IN2		LSIO.KPP0.COL2	LSIO.GPIO3.IO20		
ADC_IN2	DMA.FLEXCAN1.RX			LSIO.GPIO3.IO31		
FLEXCAN1_RX	DMA.FLEXCAN1.TX			LSIO.GPIO4.IO00		
FLEXCAN1_TX						
	DMA.FLEXCAN0.TX			LSIO.GPIO3.IO30		
FLEXCAN0_TX	MLB.DATA	AUD.SAI3.RXD		LSIO.GPIO3.IO28		
MLB_DATA(SAI3_RXD)	CONN.MLB.SIG	AUD.SAI3.RXC		LSIO.GPIO3.IO26		
MLB_SIG(SAI3_RXC)						
	HSIO.PCIE1.CLKREQ.B			LSIO.GPIO4.IO30		
PCIE_CTRL1_CLKREQ_B(GPIO4_IO30)	HSIO.PCIE0.WAKE.B			LSIO.GPIO4.IO28		
PCIE_CTRL0_WAKE_B	HSIO.PCIE1.WAKE.B			LSIO.GPIO4.IO31	GP_LED1	
PCIE_CTRL1_WAKE_B(GPIO4_IO31)						
	HSIO.PCIE0.CLKREQ.B			LSIO.GPIO4.IO27		
PCIE_CTRL0_CLKREQ_B	HSIO.PCIE0.PERST.B			LSIO.GPIO4.IO29		
PCIE_CTRL0_PERST_B	HSIO.PCIE1.PERST.B			LSIO.GPIO5.IO00	GP_LED2	
PCIE_CTRL1_PERST_B(GPIO5_IO00)						
	USB.HSIC0.STROBE	DMA.I2C1.SCL		LSIO.GPIO5.IO02		
USB_HSIC0_STROBE	USB.HSIC0.DATA	DMA.I2C1.SDA		LSIO.GPIO5.IO01		
USB_HSIC0_DATA						
	AUD.ESAI1.TX4.RX1			LSIO.GPIO2.IO12		
ESAI1_TX4_RX1						
	AUD.SAI1.RXFS	AUD.SAI0.RXD		LSIO.GPIO3.IO14		
SAI1_RXFS(SAI0_RXD)						
	USDHC1.RESET.B			LSIO.GPIO4.IO07		
USDHC1_RESET_B	AUD.ESAI1.TX1	AUD.SAI2.RXFS		LSIO.GPIO2.IO09		
ESAI1_TX1						
	AUD.ESAI1.TX2.RX3			LSIO.GPIO2.IO10	BC_GPIO1	
ESAI1_TX2_RX3(GPIO2_IO10)	AUD.ESAI1.TX3.RX2			LSIO.GPIO2.IO11	BC_GPIO2	
ESAI1_TX3_RX2(GPIO2_IO11)	MLB.CLK	AUD.SAI3.RXFS		LSIO.GPIO3.IO27		
MLB_CLK(SAI3_RXFS)						
	ENET1.REFCLK.125M.25M	ENET1.PPS		LSIO.GPIO4.IO16		
ENET1_REFCLK_125M_25M(GPIO4_IO16)	ENET0.REFCLK.125M.25M	ENET0.PPS		LSIO.GPIO4.IO15		
ENET0_REFCLK_125M_25M(GPIO4_IO15)	DMA.I2C1.SDA	USB.OTG2.OC		LSIO.GPIO4.IO06		
USB_SS3_TC3(I2C1_SDA)	DMA.I2C1.SDA	USB.OTG1.OC		LSIO.GPIO4.IO05		
USB_SS3_TC2(USB_OTG1_OC)	DMA.FLEXCAN2.RX			LSIO.GPIO4.IO01	BC_GPIO3	
FLEXCAN2_RX(GPIO4_IO01)	DMA.FLEXCAN2.TX			LSIO.GPIO4.IO02	BC_GPIO4	
FLEXCAN2_TX(GPIO4_IO02)	DMA.I2C1.SCL	USB.OTG2.PWR		LSIO.GPIO4.IO04		
USB_SS3_TC1(I2C1_SCL)	DMA.I2C1.SCL	USB.OTG1.PWR		LSIO.GPIO4.IO03		
USB_SS3_TC0(USB_OTG1_PWR)	AUD.SAI1.TXC	AUD.SAI0.TXC		LSIO.GPIO3.IO15		
SAI1_TXC(SAI0_TXC)	AUD.SAI1.RXC	AUD.SAI0.TXD		LSIO.GPIO3.IO12		
SAI1_RXC(SAI0_TXD)	DMA.SPI2.SCK			LSIO.GPIO3.IO07		
SPI2_SCK	ENET1.MDC	DMA.I2C4.SCL		LSIO.GPIO4.IO18		
ENET1_MDC(I2C4_SCL)	ENET1.MDIO	DMA.I2C4.SDA		LSIO.GPIO4.IO17		
ENET1_MDIO(I2C4_SDA)						
	DMA.FLEXCAN0.RX			LSIO.GPIO3.IO29		
FLEXCAN0_RX						

Variscite

Title: 15. PINMUX J3 & J4			
Size: A3	Document Number: VAR-SP8CustomBoard	Project: VAR-SP8CustomBoard	Rev: 1.3A
Designer: Leonid S.		Approved By:	
Date: Monday, January 25, 2021		Sheet 15 of 15	