MPU Comparison Table: i.MX 8 Series and Layerscape®

i.MX applications processors and Layerscape processors are Arm®-based solutions ranging from single to multicore SoCs for automotive, industrial and IoT applications requiring scalability, high-performance and low-power capabilities.

Features	i.MX 8	i.MX 8X	i.MX 8M	i.MX 8M Mini	i.MX 8M Nano	i.MX 8M Plus	Layerscape LS1028A	Layerscape LS1012A
CPU (Arm Cortex®-A) @ Max Frequency	(8QuadMax) 2 x Arm Cortex-A72 @ 1.6 GHz and 4 x Cortex-A53 @ 1.2 GHz (8QuadPlus) 1 x Cortex-A72 @ 1.6 GHz and 4 x Cortex-A53 @ 1.2 GHz	(8QuadXPlus) 4 x Cortex-A35 @ 1.2 GHz (8DualXPlus) 2 x Cortex-A35 @ 1.2 GHz (8DualX) 2 x Cortex-A35 @ 1.2 GHz	(Quad) 4 x Cortex-A53 @ 1.5 GHz (Dual) 2 x Cortex-A53 @ 1.5 GHz (QuadLite) 4 x Cortex-A53 @ 1.5 GHz	(Quad/QuadLite) 4 x Cortex-A53 @ 1.8 GHz (Dual/DualLite) 2 x Cortex-A53 @ 1.8 GHz (Solo/SoloLite) 1 x Cortex-A53 @ 1.8 GHz	(Quad/QuadLite) 4 x Cortex-A53 @ 1.5 GHz (Dual/DualLite) 2 x Cortex-A53 @ 1.5 GHz (Solo/SoloLite) 1 x Cortex-A53 @ 1.5 GHz	(Quad/QuadLite) 4 x Cortex-A53 @ 1.8 GHz (Dual) 2 x Cortex-A53 @ 1.8 GHz	(LS1028A/27A) 2 x Cortex-A72 @ 1.5 GHz (LS1018A/17A) 1 x Cortex-A72 @ 1.5 GHz	1 x Cortex-A53 @ 1 GHz
I/D-Cache (Cortex-A), L2 Cache, On-chip RAM (OCRAM)	32 KB/32 KB L1 (Parity), 2 x 1 MB L2 (ECC), 256 KB OCRAM	32 KB/32 KB L1 (Parity), 512 KB L2 (ECC), 256 KB OCRAM	32 KB/32 KB L1 (ECC), 1 MB L2 (ECC), 160 KB OCRAM	32 KB/32 KB L1 (ECC), 512 KB L2 (ECC), 256 KB OCRAM	32 KB/32 KB L1 (ECC), 512 KB L2 (ECC), 512 KB OCRAM	32 KB/32 KB L1 (ECC), 512 KB L2 (ECC), 612 KB OCRAM	48 KB/32 KB L1 (ECC), 1 MB L2 (ECC), 256 KB OCRAM	32 KB/32 KB L1 (ECC), 256 KB L2 (ECC), 128 KB OCRAM
CPU (Cortex-M)	2x 256 KB TCM (ECC)	1 x Cortex-M4 @ 266 MHz	1 x Cortex-M4 @ 266 MHz	1 x Cortex-M4 @ 400 MHz	1 x Cortex-M7 @ 750 MHz	1 x Cortex-M7 @ 800 MHz	No	No
Tightly coupled SRAM (Cortex-M)	2 x 2 KB TCM (ECC)	256 KB TCM (ECC)	256 KB TCM	256 KB TCM	256 KB TCM	256 KB TCM	No	No
External Memory Interfaces	2 x 64 LPDDR4-3200, 2 x Quad SPI or 1 x Octal SPI (XIP, FlexSPI), Raw NAND (SLC/MLC, BCH62)	1 x 32 LPDDR4-2400, DDR3L-1866 (ECC), 2 x Quad SPI or 1 x Octal SPI (XIP, FlexSPI), Raw NAND (SLC/MLC, BCH62); (8DualX) 1 x 16 LPDDR4-2400, DDR3L-1866 (no ECC)	1 X 32 LPDDR4-3200, DDR4-2400, DDR3L-1600, 2 x QuadSPI (XIP), Raw NAND (SLC/MLC, BCH62), 16/32-bit NOR	1 x 32 LPDDR4-3000, DDR4-2400, DDR3L-1600, 2 x QuadSPI (XIP), Raw NAND (SLC/MLC, BCH62), 16/32-bit NOR	1 x 16 LPDDR4-3200, DDR4-2400, DDR3L-1600, 2 x QuadSPI (XIP), Raw NAND (SLC/MLC, BCH62), 16/32-bit NOR	1 X 32 LPDDR4-4000, DDR4-3200, DDR3L-1600 (Inline ECC) 2 x QuadSPI (XIP) or 1 x OctalSPI (XIP), Raw NAND (SLC/MLC, BCH62), 16/32-bit NOR	1 x 32 DDR4-1600 (ECC), DDR3L-1600 (ECC) 1x XSPI (NOR, NAND), SATA	1 x 16-DDR3L-1300 , 1x QSPI (NOR)
Multimedia Card (eMMC)/ Secure Digital Controller (SDIO)	3 x eMMC 5.1/SD 3.0	2 x SD 3.0	2 x SD 3.0	3 x eMMC 5.1/SDIO 3.0	3 x eMMC 5.1/SDIO 3.0	3 x eMMC 5.1/SDIO 3.0	2 x eMMC 5.1/SD 3.0/SDIO	2 x eMMC 4.5/SD 3.0/SDIO
PCI Express®	1 x PCIe® 3.0 (2-lane)* and 2 x PCIe 3.0 (1-lane each), or 3 x PCIe 2.0 (1-lane each)* all with L1 low-power substate and PHY	1 x PCIe 3.0 with L1 low-power substate and PHY (1-lane)	2 x PCIe 2.0 with L1 low-power substate and PHY (1-lane)	1 x PCIe 2.0 with L1 low-power substate and PHY (1-lane)	No	1 x PCIe 3.0 with L1 low-power substate and PHY (1-lane)	2 x PCIe 3.0 RC and endpoint	1x PCIe 2.0 RC and endpoint
Hard Disk Drive Interface	1 x SATA with PHY (1-lane) instead of 1 x PCIe (2-lane)*	No	No	No	No	No	1 x SATA 3.0	1 x SATA 3.0
Display Interface	2 x MIPI-DSI (4-lanes each), 2 x LVDS, 1 x HDMI 2.0a/eDP 1.4/DP 1.3 with HDCP 2.2; Dual display processor with SafeAssure® certification	2 x MIPI-DSI/LVDS (4-lanes each) or 1 x 8-lane LVDS with combo PHY; 1 x parallel LCD (24-bit RGB); Display processor with SafeAssure certification	1 x HDMI 2.0b (ARC/eDP), 1 x MIPI-DSI (4-Lane)	1 x MIPI-DSI (4-Lane)	1 x MIPI-DSI (4-Lane)	1 x MIPI-DSI (4-lane), 1 x LVDS (4-or 8-lane), 1 x HDMI 2.0 a Tx (eARC) with PHY	(LS1028A/18A) 1 x eDP/DP	No
LCD Resolution	1 x UltraHD 4Kp60 display or up to 4 x independent FullHD 1080p60 displays	2 x 1080p, 1 x WVGA	1x 4Kp30 or 2x1080p60 or 1x1080p60 + 2x 720p60	1 x 1080p60	1 x 1080p60	1 x 4Kp30 or 2 x 1080p60 or 1 x 1080p60 + 2 x 720p60	(LS1028A/18A) 1 x 4K p60	No
Hardware Video Acceleration	4K H.265 decode, 1080p H.264 encode/decode	Up to 4Kp30 H.265* or 4Kp30 H.264 decode; 1080p30 H.264 encode	(Quad/Dual) up to 4Kp60 HEVC H.265, VP9 with HDR Dolby Vision(R) decode*; software encode on Cortex-A-53; (QuadLite) No hardware video acceleration	(Quad/Dual/Solo) 1080p60 HEVC/H.265, VP9, VP8, H.264 decode*; 1080p60 H.264, VP8 encode* (QuadLite/DualLite/SoloLite) No hardware video acceleration	No	(Quad/Dual) 1080p60 H.265, H.264, VP9, VP8 decode*; 1080p60 H.265, H.264 encode* (QuadLite) No hardware video acceleration	No	No
Digital Audio Interface	4 x SAI (2Tx + 4Rx external I²S lanes, 24-bit up to 192 KHz), 2 x ESAI/1 x MQS, 1 x S/PDIF Tx/Rx, 1 x ASRC	4 x SAI (2Tx + 2Rx external I²S lanes, 32-bit up to 192 KHz), 1 x ESAI/MQS, 1 x S/PDIF Tx/Rx, 2 x ASRC	5 x SAI (11Tx + 14Rx external I²S lanes): Each lane up to 24.576 MHz BCLK (32-bit, 2-ch. 384 KHz, up to 32-ch. TDM); DSD512; S/PDIF	5 x SAI (13Tx + 16Rx external I²S lanes): Each lane up to 24.576 MHz BCLK (32-bit, 2-ch. 384 KHz, up to 32-ch. TDM); DSD512 4Tx + 4Rx support 49.152 MHz BCLK for 768 KHz; 8-ch. PDM digital microphone input; S/PDIF Tx	5 x SAI (10Tx + 10Rx external I²S lanes): Each lane up to 49.152 MHz BCLK (32-bit, 2-ch. 768 KHz, up to 32-ch. TDM); DSD512; 8-ch. PDM digital microphone input; S/PDIF Tx/Rx; 32-ch 4-instance ASRC	6 x SAI (15Tx + 18Rx external I²S lanes): Each lane up to 49.152 MHz BCLK (32-bit, 2-ch. 768 KHz, up to 32-ch. TDM); DSD512; 8-ch. PDM digital micro phone in put; S/PDIF Tx/Rx; 3 -ch. 4-i nstance ASRC; ARC, eARC	6 x SAI/I²S	5 x SAI/I²S
Hardware 2D/3D Graphics Acceleration	2 x GC7000XSVX (8-shader each)* OpenGL® ES 3.2, Vulkan®, OpenCL™ 1.2; OpenVX™ 1.1 vision extensions; high-performance 2D Blit Engine	1 x GC7000Lite (4-shader)* OpenGL® ES 3.1, Vulkan®, OpenCL™ 1.2; high-performance 2D Blit Engine	1 x GC7000Lite (4-shader) OpenGL® ES 3.1, Vulkan®, OpenCL™ 1.2	1 x GCNanoUltra 3D (1 shader) OpenGL® ES 2.0, 1 x GC328 2D	(Quad/Dual/Solo) 1 x GC7000UltraLite (2 shaders) OpenGL® ES 3.1, Vulkan®, OpenCL™ 1.2 (QuadLite/DualLite/SoloLite) No hardware graphics acceleration	1 x GC7000UltraLite 3D GPU (2 shaders) OpenGL® ES 3.1, Vulkan,® OpenCL™ 1.2; GC520L 2D GPU	(LS1028A/18A) 1 x GC7000UltraLite 3D GPU (2 shaders) OpenGL® ES 3.1, OpenCL™ 1.2	No
Additional processor	Tensilica® HiFi 4 DSP with 338 KB OCRAM and 64 KB TCM	Tensilica HiFi 4 DSP with 448 KB OCRAM and 64 KB TCM	No	No	No	Machine Learning Accelerator* (2.3 TOPS); Tensilica HiFi 4 DSP with 256 KB OCRAM and 64 KB TCM	No	No
Camera Sensor Interface (CSI)	2 × MIPI-CSI (4-lanes each, 1.5 Gbit/lane), 1 × HDMI-RX HDMI 2.0a with HDCP 2.2	1 x MIPI-CSI (4-lanes, 1.5 Gbit/lane), 1 x 8/10-bit parallel CSI	2 x MIPI-CSI (4-Lane, 1.5 Gbit/lane)	1 x MIPI-CSI (4-Lane, 1.5 Gbit/lane)	1 x MIPI-CSI (4-Lane, 1.5 Gbit/lane)	2 x MIPI-CSI (4-Lane, 1.5 Gbit/lane); Dual camera ISP* (2x HC/1x 12 MP) HDR, dewarp	No	No
Universal Asynchronous Reciever/Transmitter (UART)	8 x UART (5 Mbit/s)	5 x UART (5Mbps)	4 x UART (5Mbps)	4 x UART (5Mbps)	4 x UART (5Mbps)	4 x UART (5Mbps)	8 x UART	2 x UART
Serial Peripheral Interface (SPI)/I²C	4 x SPI/5 x I²C high speed with DMA, or 8 x I²C low speed (no DMA)	4 x SPI/9 x I²C	3 x SPI/4 x I²C	3 x SPI/4 x I²C	3 x SPI/4 x I²C	3 x SPI/6 x I²C	3 x SPI/8 x I²C	1 x SPI/2 x I²C
USB Controller	1 × USB 3.0 with PHY (dual role), 1 × USB 2.0 with PHY (OTG), 1 x USB 2.0 with HSIC (host)	(8QuadXPlus/8DualXPlus) 1 × USB 3.0/2.0 with PHY (OTG), 1 × USB 2.0 with PHY (OTG); (8DualX) 2 x USB 2.0 with PHY (OTG)	2 x USB 3.0/2.0 (OTG) Type C with PHY	2 x USB 2.0 (OTG) with PHY	1 x USB 2.0 (OTG) with PHY	2 x USB 3.0/2.0 Type C with PHY	3 x USB 3.0/2.0 (OTG) with PHY	1 x USB 3.0/2.0 (OTG) with PHY, 1 x USB 2.0 with ULPI
Ethernet	2 × Gbit/s Ethernet with RGMII, IEEE 1588®, AVB (Audio Video Bridging, IEEE 802.1Qav)	(8QuadXPlus/8DualXPlus) 2 x Gbit/s Ethernet with RGMII, IEEE 1588, AVB (Audio Video Bridging, IEEE 802.1Qav); (8DualX) 1 x Gbps and 1 x 10/100 Ethernet	1 × Gbit/s Ethernet with energy-efficient Ethernet, IEEE 1588, AVB (Audio Video Bridging, IEEE 802.1Qav)	1 × Gbit/s Ethernet with energy-efficient Ethernet, IEEE 1588, AVB (Audio Video Bridging, IEEE 802.1Qav)	1 × Gbit/s Ethernet with energy-efficient Ethernet, IEEE 1588, AVB (Audio Video Bridging, IEEE 802.1Qav)	2 x Gbit/s Ethernet with IEEE 1588, AVB (Audio Video Bridging, IEEE 802.1Qav); 1x also with TSN	1 x 2.5/1 Gbit/s + TSN + IEEE 1588 1 x 1 Gbit/s + IEEE 1588 4 x 2.5/1 Gbit/s Switch + TSN + IEEE 1588	2 x 2.5/1 Gbit/s
CAN and Other Interface	3 x CAN FD, MLB 150	3 x CAN FD, MLB 25/50	No	No	No	2 x CAN FD	2 x CAN FD	No
Security	HAB secure boot, Arm TrustZone®, RNG, RSA up to 4096, AES-128/192/256, 3DES, ARC4, MD-5, SHA up to 512, flashless SHE, ECC, secure JTAG, 4 x tamper pins	HAB secure boot, TrustZone, RNG, RSA up to 4096, AES-128/192/256, 3DES, ARC4, MD-5, SHA up to 512, flashless SHE, ECC, secure JTAG, 10 x tamper pins	HAB secure boot, TrustZone, True RNG, RSA up to 4096, AES-128/192/256, 3DES, ARC4, MD-5, SHA up to 256, ECC, secure JTAG	HAB secure boot, TrustZone, True RNG, RSA up to 4096, AES-128/192/256, 3DES, ARC4, MD-5, SHA up to 256, ECC, secure JTAG	HAB secure boot, TrustZone, True RNG, RSA up to 4096, AES-128/192/256, 3DES, ARC4, MD-5, SHA up to 256, ECC, secure JTAG	HAB secure boot, TrustZone, True RNG, RSA up to 4096, AES-128/192/256, 3DES, ARC4, MD-5, SHA up to 256, ECC, secure JTAG	Trust Architecture, HAB secure boot, TrustZone, True RNG, RSA up to 4096, AES-128/192/256, 3DES, ARC4, MD-5, SHA up to 256, ECC, secure JTAG	Trust Architecture, HAB secure boot, TrustZone, True RNG, RSA up to 4096, AES-128/192/256, 3DES, ARC4, MD-5, SHA up to 256, ECC, secure JTAG
Timer	5 x general purpose, 2 x watchdog	5 x general purpose, 2 x watchdog	6 x general purpose, 3 x watchdog	6 x general purpose, 3 x watchdog	6 x general purpose, 3 x watchdog	6 x general purpose, 3 x watchdog	8 x general purpose, 3 x watchdog	8 x general purpose, 2 x watchdog
Real-Time Clock (RTC)	Secure RTC	Secure RTC	Secure RTC	Secure RTC	Secure RTC	Secure RTC	Secure RTC	Secure RTC
Pulse Width Modulation	8 x PWM	4 x PWM	4 x PWM	4 x PWM	4 x PWM	4 x PWM	8 x PWM	8 x PWM
ADC Channels	2 × 12-bit ADC (16-channel/4-channel)*	1 x 12-bit ADC (6-channel)*	Add LPC804 (32 KB flash, 12-ch. 12-bit ADC, 1x 10-bit DAC) via I²C	Add LPC804 (32 KB flash, 12-ch. 12-bit ADC, 1x 10-bit DAC) via I²C	Add LPC804 (32 KB flash, 12-ch. 12-bit ADC, 1x 10-bit DAC) via I²C	Add LPC804 (32 KB flash, 12-ch. 12-bit ADC, 1x 10-bit DAC) via I²C	Add LPC804 (32 KB flash, 12-ch. 12-bit ADC, 1x 10-bit DAC) via I²C	Add LPC804 (32 KB flash, 12-ch. 12-bit ADC, 1x 10-bit DAC) via I²C
Power Management	Dedicated I²C for PMIC interface, PMIC PF8200/8100	Dedicated I²C for PMIC interface, PMIC PF8200/8100	PMIC PF4210	PMIC PCA9450B	PMIC PCA9450B	PMIC PCA9450C	PMIC MC34VR500V9ES	PMIC MC34VR5100A1EP
Package	29 x 29 FC-PBGA 0.75 mm pitch	21 x 21 FC-PBGA 0.8 mm pitch, 17 x 17 FC-PBGA 0.8 mm pitch	17 x 17 FC-BGA (621) 0.65 mm pitch	14 x 14 FC-BGA 0.5 mm pitch (depopulated) *pin-compatible with i.MX 8M Nano 14 x 14 package	14 x 14 FC-BGA 0.5 mm pitch (depopulated) *pin-compatible with i.MX 8M Mini 14 x 14 package	15 x 15 FC-BGA 0.5 mm pitch (depopulated)	17 x 17 FC-PBGA 0.75 mm pitch	9.6 x 9.6 FC-LGA 0.5 mm pitch
Qualification and Junction Temperature Range*	Automotive -40 °C to +125 °C Industrial -40 °C to +105 °C	Automotive -40 °C to +125 °C Industrial -40 °C to +105 °C	Industrial -40 °C to +105 °C Consumer 0 °C to +95 °C	Industrial -40 °C to +105 °C Consumer 0 °C to +95 °C	Industrial -40 °C to +105 °C Consumer 0 °C to +95 °C	Industrial -40 °C to +105 °C Consumer 0 °C to +95 °C	Industrial -40 °C to +125 °C Automotive -40 °C to +105 °C (AEC Grade 3)	Industrial -40 °C to +105 °C
Process	28 nm FD-SOI	28 nm FD-SOI	28 nm HPC	14 nm LPC FinFET	14 nm LPC FinFET	14 nm LPC FinFET	28 nm HPM	28 nm HPM

General Note 1: Refer to IC documentation for specifications per processor.
General Note 2: The number of interfaces is dependent on the pin muxing.
* Some features vary across packages.
^ Performance dependent on application use case.
# Refer to IC documentation for DDR frequencies and further details.

www.nxp.com/imx8, www.nxp.com/ls1012a, www.nxp.com/ls1028a

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Please note: The product data sheets and reference manuals are your best source for the most current and detailed technical data on the i.MX applications processors and Layerscape processors you prefer. For documentation on i.MX applications processors, please visit **www.nxp.com/iMX**. For Layerscape processors, please visit **www.nxp.com/layerscape**. Share ideas, design tips and meet other i.MX fans at **community.nxp.com/community/imx**.

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