# VAR-DT8MCustomBoard

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## Revision History

| Document | Carrier | Description |
|---|---|---|
| 1.0 | 2.0 | Changes from DOC 1.9 Carrier 1.4D include:<br>* Optimisation for DART-MX8MP:<br>- Added external ethernet PHY<br>- Control IOs used on previous version over SAI1 now controlled via I2C expander<br>- Added DSI header option for DART-MX8MP stock item exposed pins; Pinout compatible to Symphony J7+J8<br>- Native USB ID usage added important note<br>- USB Type C active discharge replaced with bleeder<br>- USB Type C crossbar differential switch simplified.<br>- Removed DT8M NAND option<br>- Added QSPI header J41 - located in location of J25<br>- J27 & J28 pinout aligned to Symphony<br>- Added PD on J1.38 for BSP CustomV2.0 signal.<br>- Added additional CAN PHY on iMX8MP<br>- U44 footprint modified from SOIC to DFN<br>- SD card power switch modified<br>- Main power switch type align to Symphony<br>- DART-MX8M DP connector replaced with 40pin eDP REF. design<br>- HDMI path simplified<br>- PINMUX page deleted - reference to XLS<br>- Aded reference design for 12Mb/s CAN-FD transciever<br>- Added M.2. PCIe reference design<br>- Add option on bottom to route PCIe port 1 to M.2 connector<br>- Replace boot config drivers to 3state type<br>- Replace MCP2518 crystal to 40MHz and connect RX_INT<br>- Updated Block Diagrams<br>- VCC_SOM Increased to 3.8V (R145 changed to 18K)<br>- D9, C58 Removed. VCC_BASE_3V3 goes up just after NVCC_3V3 |
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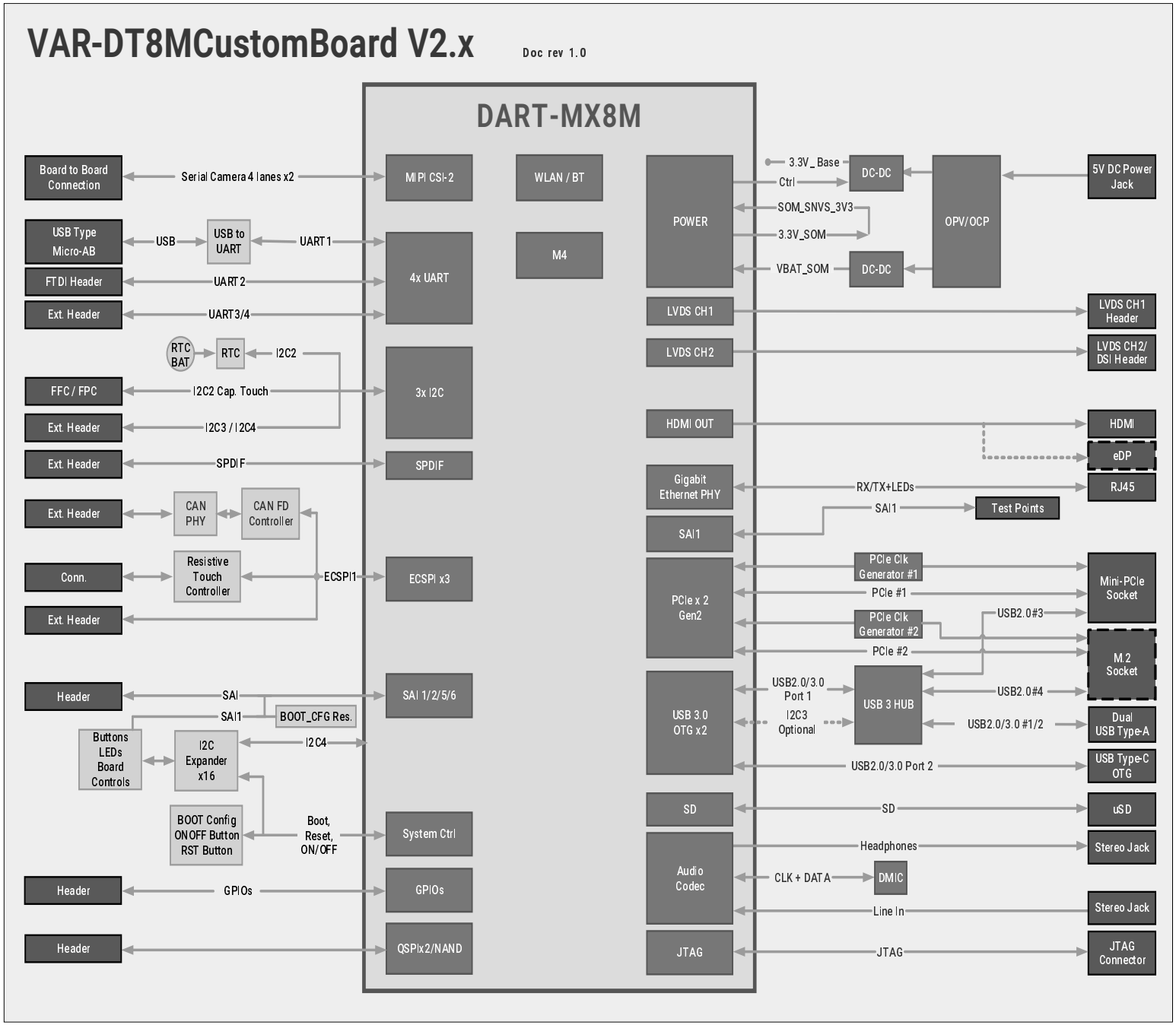
Title: 01. Cover

| Size | Document Number | Project | Rev |
|---|---|---|---|
| A3 | VAR-DT8MCustomBoard | VAR-DT8MCustomBoard | 2.0_R1.0 |

Designer: Leonid S.
Approved By:
Date: Monday, March 01, 2021
Sheet 1 of 17

# 02A. Block Diagram - DART-MX8M




**I2C BUS ADDRESS:**

I2C1: Internal to SOM

I2C2: PU - 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM
0x60 SOM - Int. power ctrl.
0x2D USB3 HUB
0xXX Header J12

I2C4: PU - 10K on U8
10K on custom
0x3C CSI P2 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

## Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

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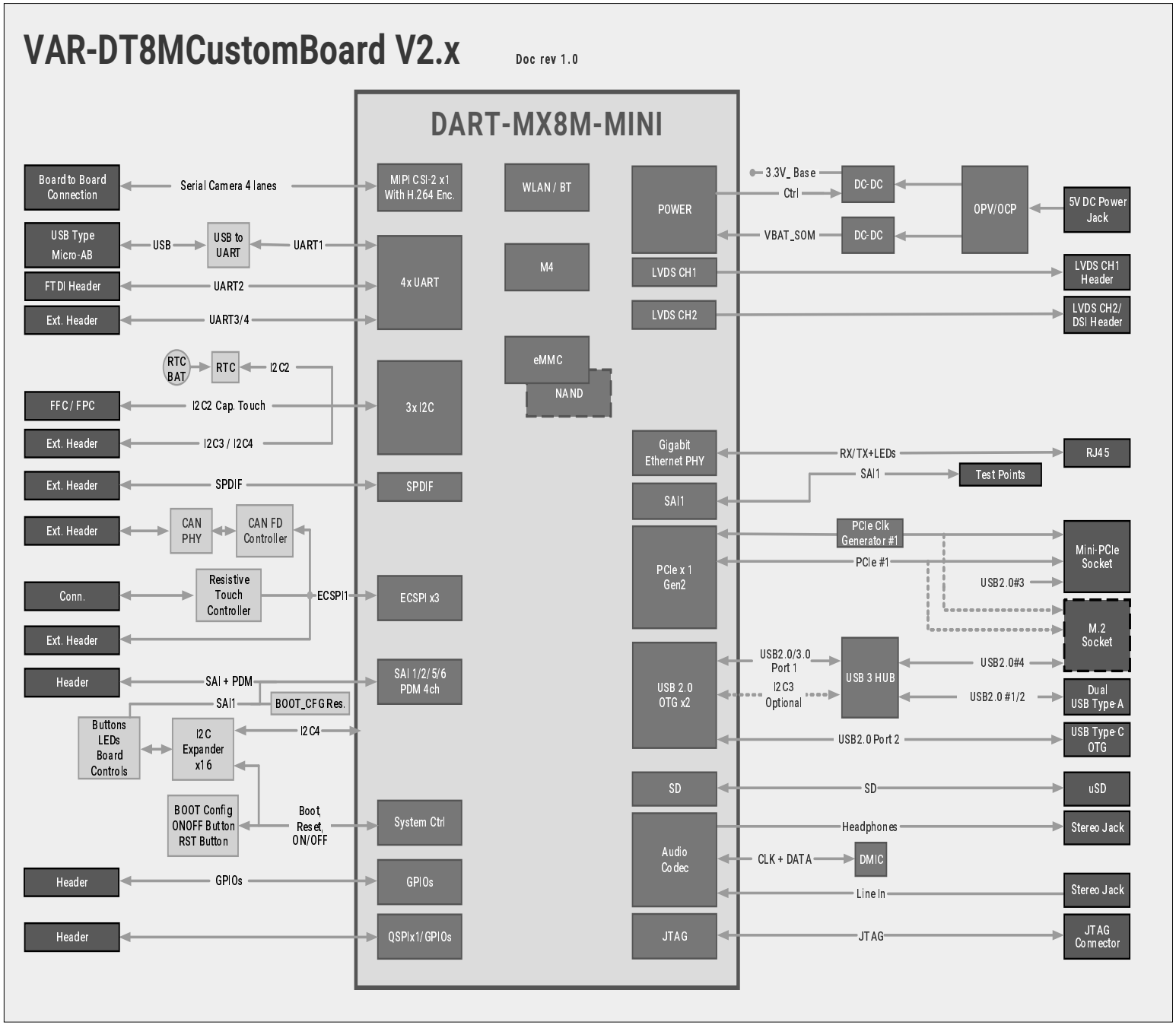
| | | | |
|---|---|---|---|
| Title: 02A. Block Diagram with DART-MX8M | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 2 of 17 | |

# 02B. Block Diagram - DART-MX8M-MINI




**I2C BUS ADDRESS:**

I2C1: Internal to SOM

I2C2: PU - 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM
0x1A SOM - Int. CODEC
0x2D USB3 HUB
0xXX Header J12

I2C4: PU - 10K on U8
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

## Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

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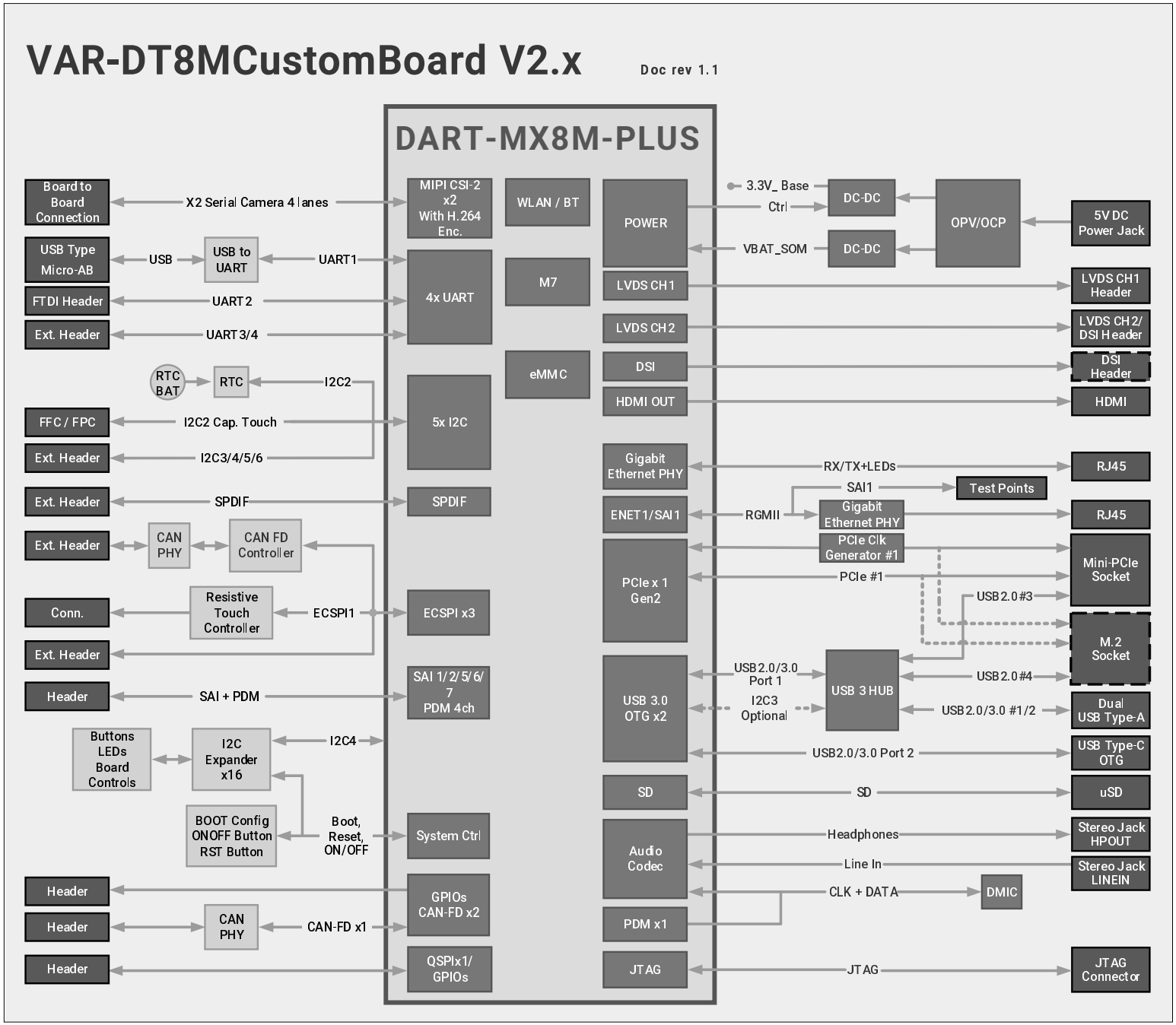
| | | | |
|---|---|---|---|
| Title: 02B. Block Diagram with DART-MX8M-MINI | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 3 of 17 | |

# 02C. Block Diagram - DART-MX8M-PLUS




**I2C BUS ADDRESS:**

I2C1: Internal to SOM

I2C2: PU - 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM

0x2D USB3 HUB
0xXX Header J12

I2C4: PU - 10K on U8
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

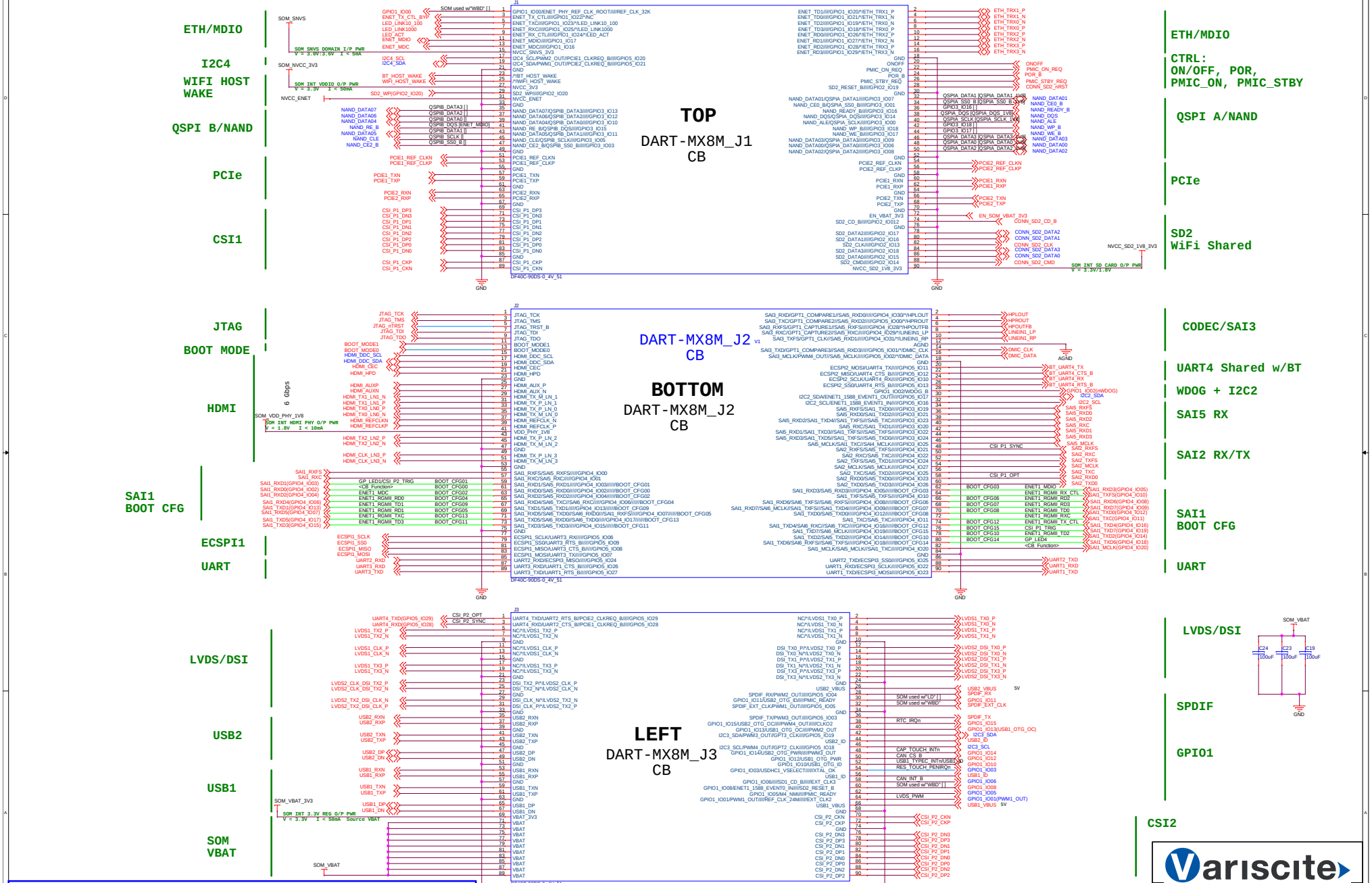
## Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

Variscite

| | | | |
|---|---|---|---|
| Title: 02B. Block Diagram with DART-MX8M-MINI | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 4 of 17 | |

# 03A - DART-MX8M Connectors




For complete alternate function per pin and specific SOM:
please refer to "DART_Compatibility_and_Pinout.XLS " located at:
ftp://ftp.variscite.com/DART_Compatibility

**Note: Pinname with /*/ prefix denotes a HW assy option.**

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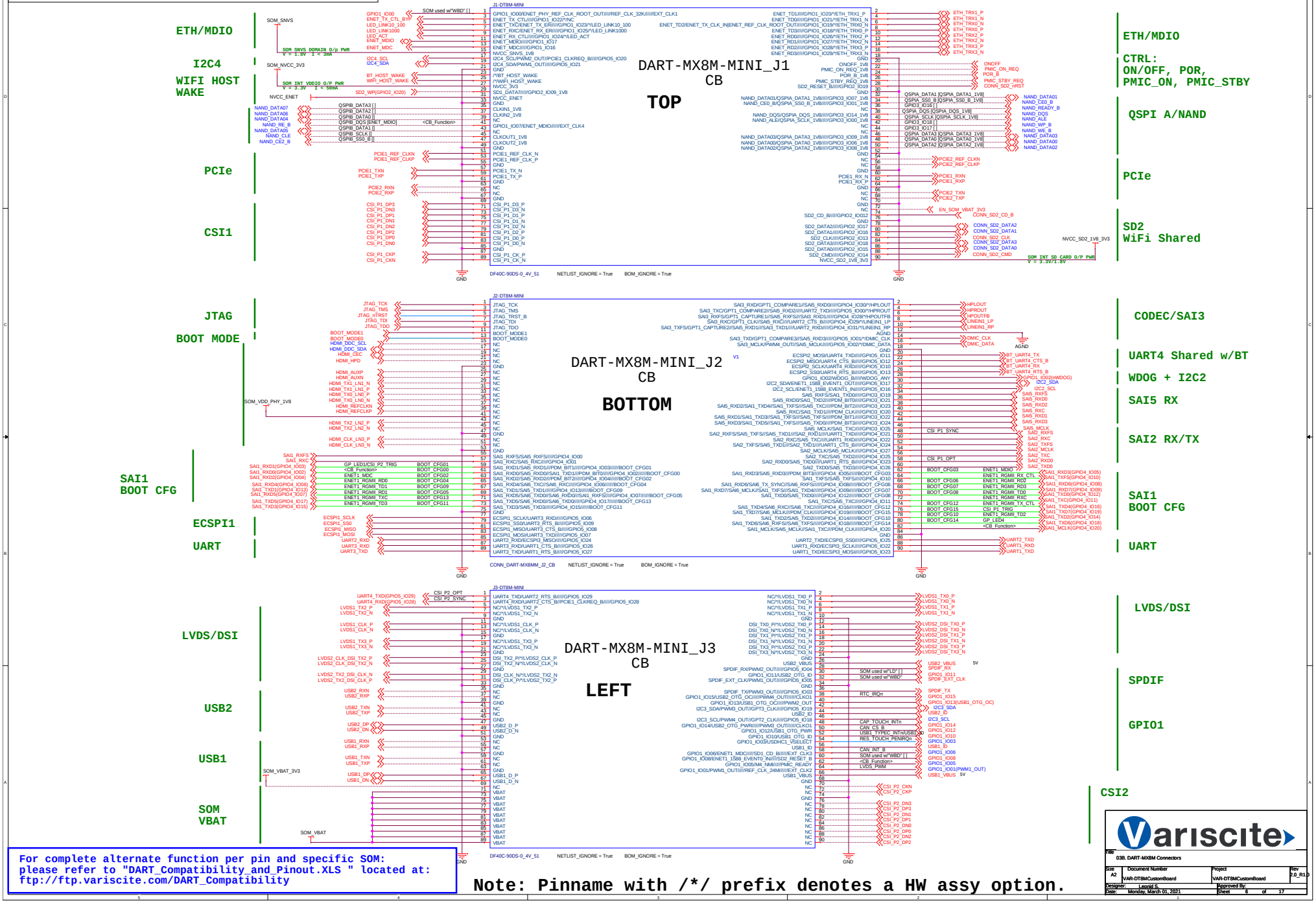
| | | | |
|---|---|---|---|
| Title: 03. DART-MX8M Connectors | | | |
| Size: A2 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 5 of 17 | |

# 03B - DART-MX8M-MINI Connectors

*** Dotted nets - Functionality differ from DART-MX8M. ***




For complete alternate function per pin and specific SOM:
please refer to "DART_Compatibility_and_Pinout.XLS " located at:
ftp://ftp.variscite.com/DART_Compatibility

Note: Pinname with /*/ prefix denotes a HW assy option.

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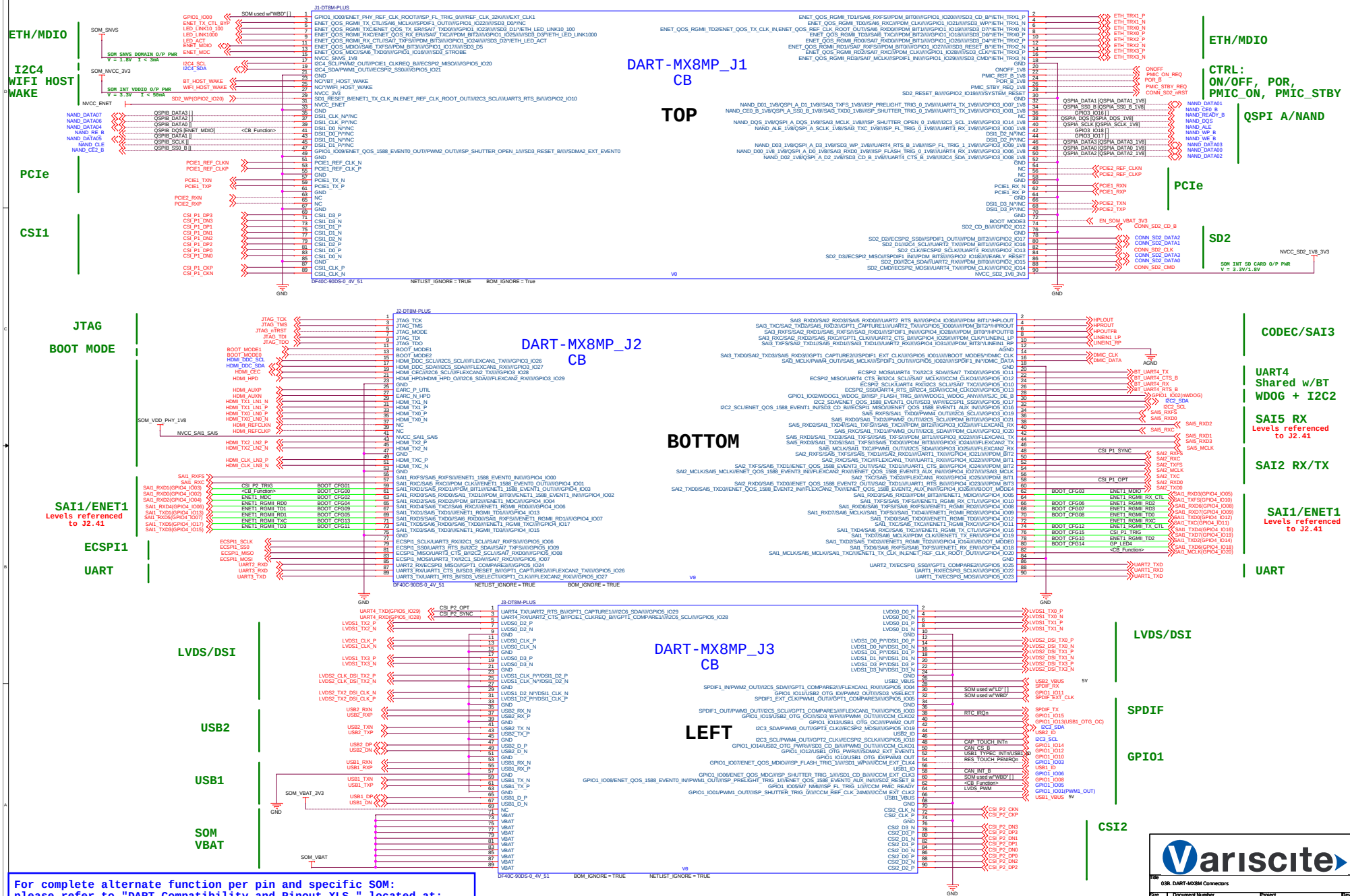
| | | | |
|---|---|---|---|
| Title: 03B. DART-MX8M Connectors | | | |
| Size: A2 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 6 of 17 | |

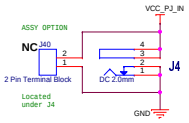
# 03C - DART-MX8M-PLUS Connectors

*** Dotted nets - Functionality differ from DART-MX8M. ***



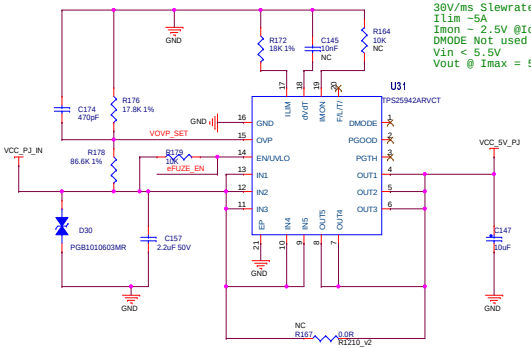
# 04. Power, RTC,Board ID

## 5VDC/4A POWER JACK

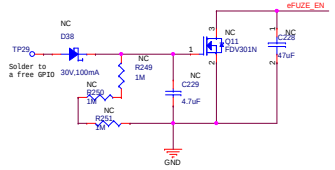



## PWR JACK 5V IN OVP/OCP

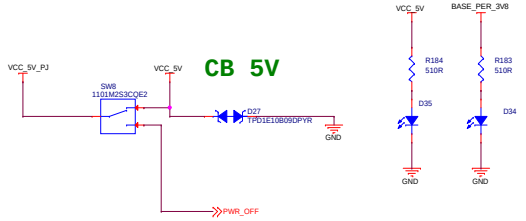
30V/ms Slewrate based on int. circuitry
Ilim ~5A
Imon ~ 2.5V @Iout=5A
DMODE Not used
Vin < 5.5V
Vout @ Imax = 5.2V



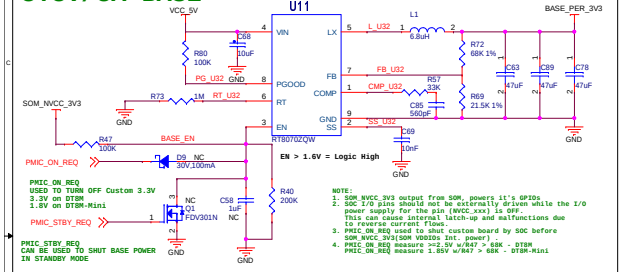

## Variscite Internal use circuit.



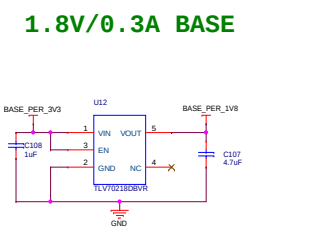

## POWER SW/(ON/OFF)



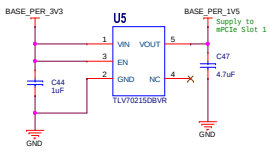

## 3.3V/3A BASE



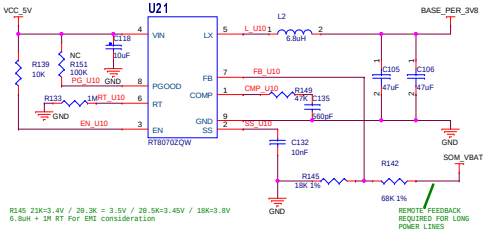

## 1.8V/0.3A BASE



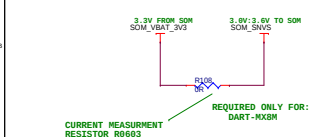

## 1.5V/0.3A #1 BASE



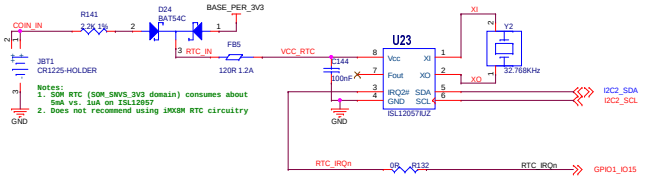

## 3.8V/3A FROM PWR JACK



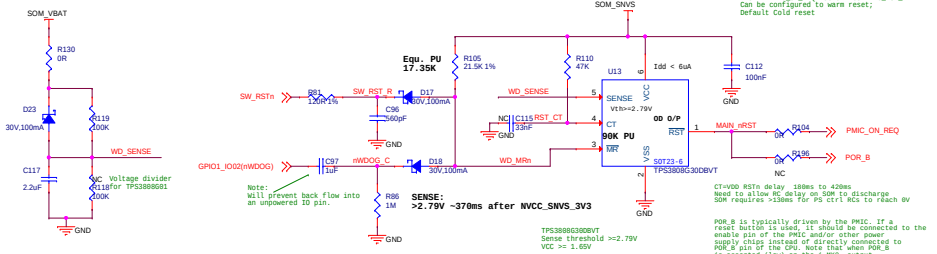

## SOM SNVS



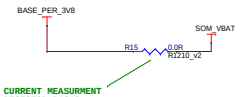

## RTC BATTERY



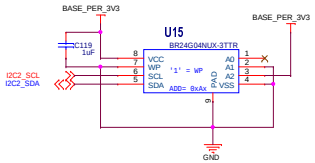

## RESET & WATCHDOG



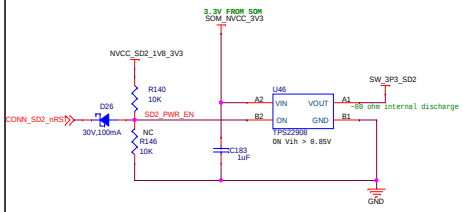

## SOM PWR



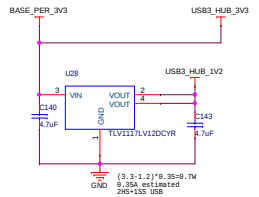

## BOARD ID



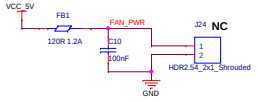

## SD POWER




## USB3 HUB POWER




## FAN : 5V/0.2A



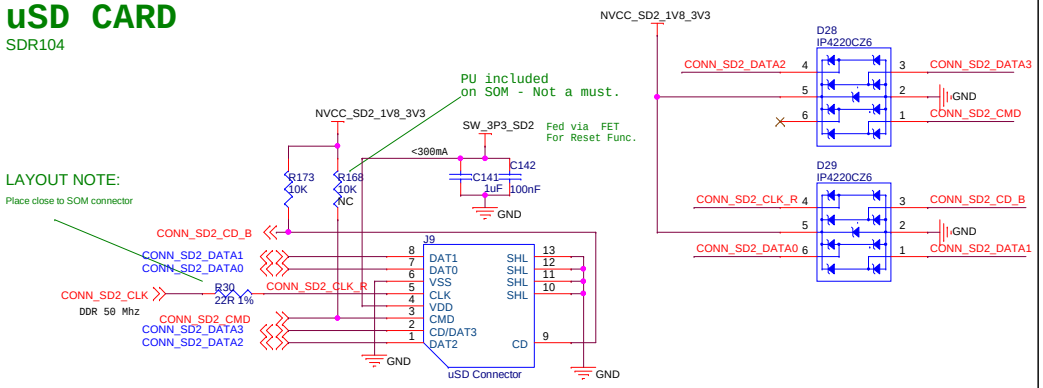

Variscite

| | | | |
|---|---|---|---|
| Title: 04. Power, RTC,Board ID | | | |
| Size: A2 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 8 of 17 | |

# 05. ETH, uSD, AUDIO, MIPI-CSI

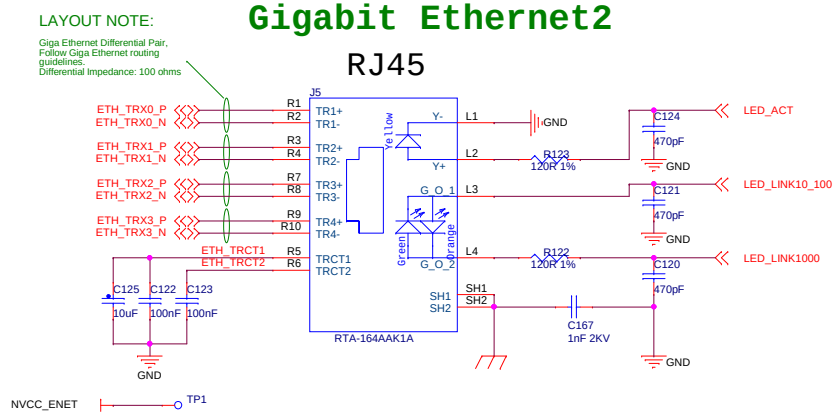
## uSD CARD

SDR104

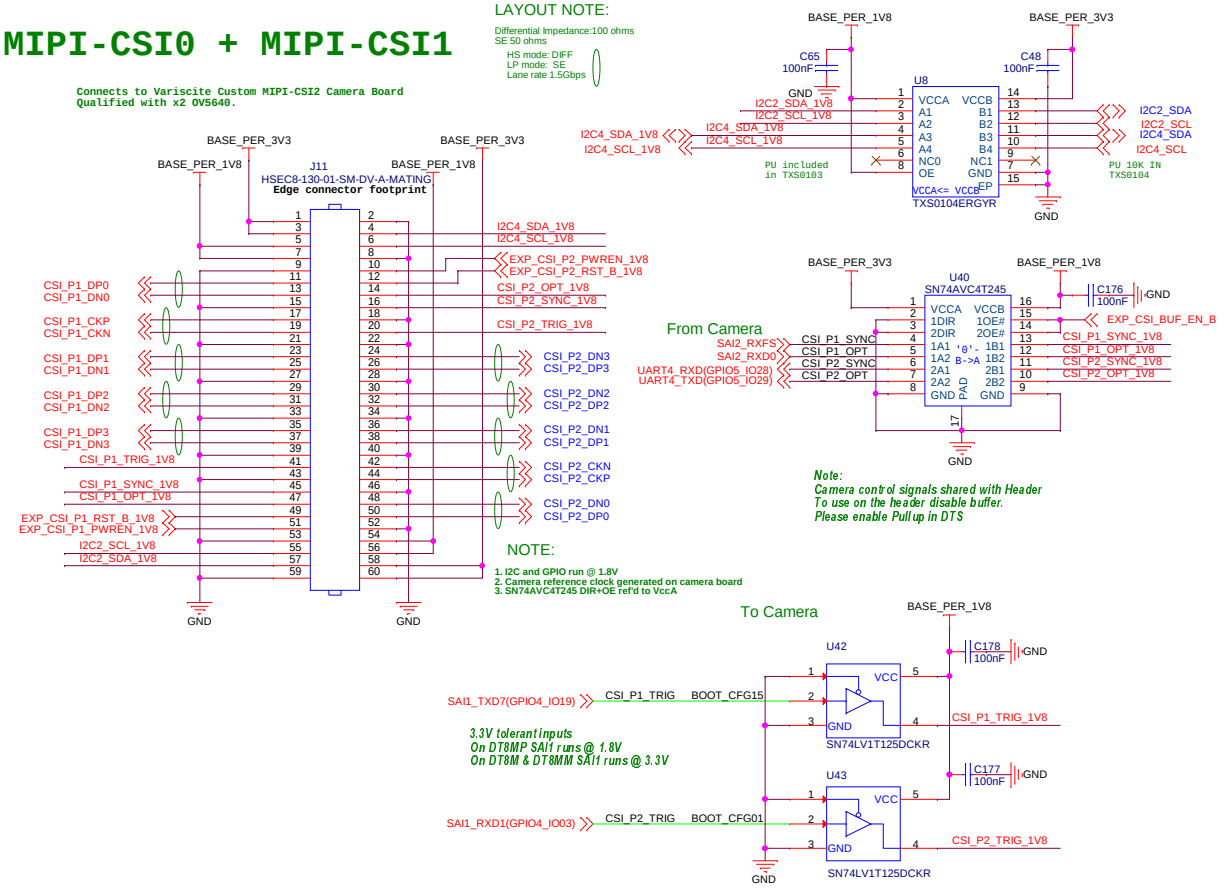



## Gigabit Ethernet2

RJ45

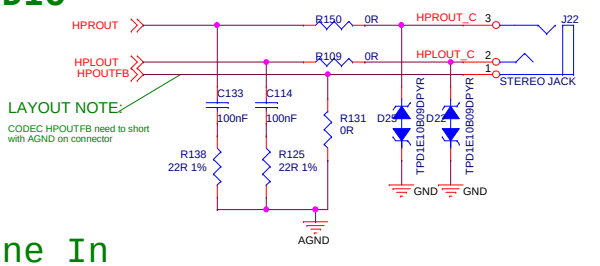



## MIPI-CSI0 + MIPI-CSI1

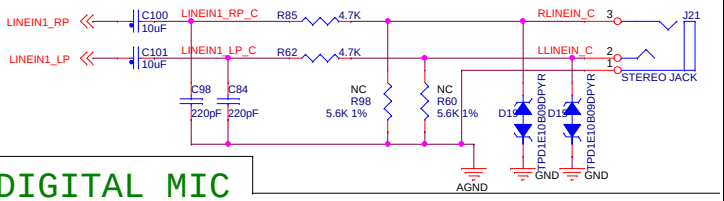



## AUDIO

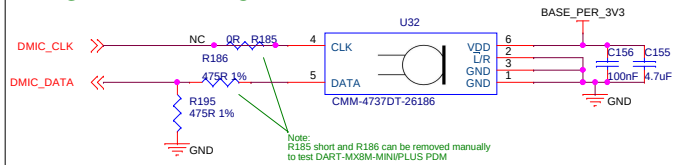
### Headphones




### Line In




### DIGITAL MIC

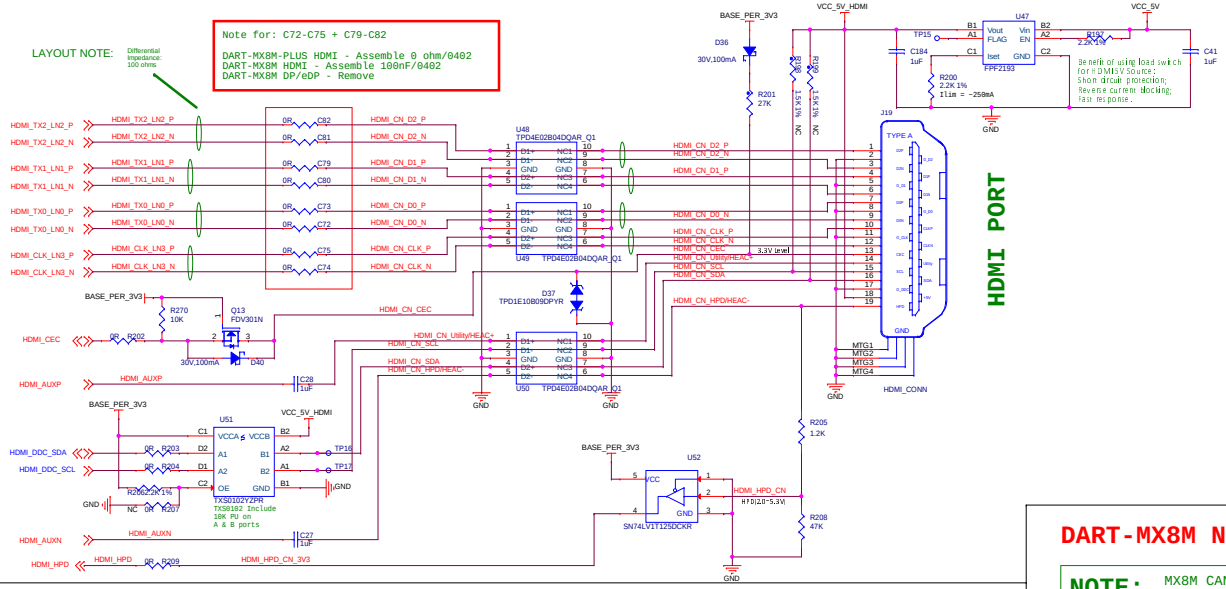



Variscite

| | | | |
|---|---|---|---|
| Title | 05. ETH, uSD, AUDIO, MIPI-CSI | | |
| Size | Document Number | Project | Rev |
| A3 | VAR-DT8MCustomBoard | VAR-DT8MCustomBoard | 2.0_R1.0 |
| Designer: | Leonid S. | Approved By: | |
| Date: | Monday, March 01, 2021 | Sheet 9 of 17 | |

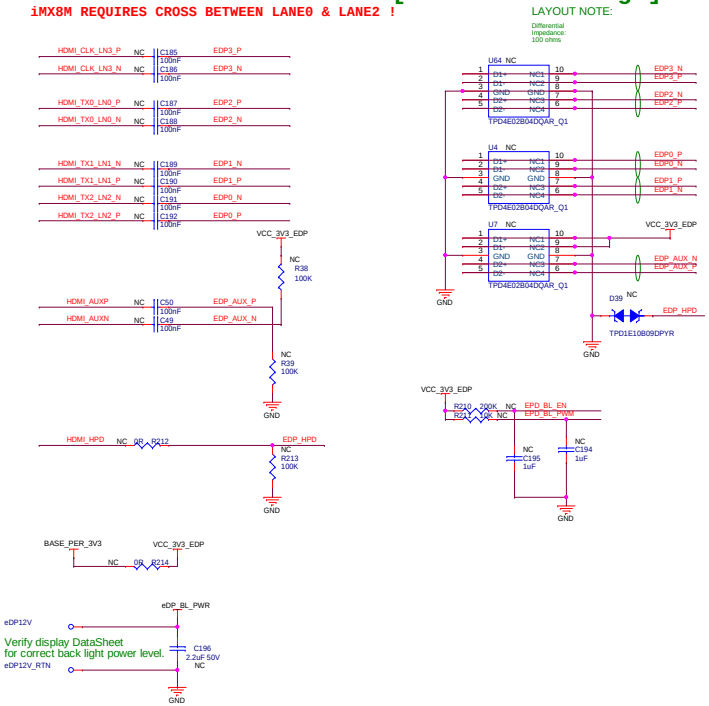
# 06. HDMI, eDP - DART-MX8M-PLUS Optimised

## HDMI PATH

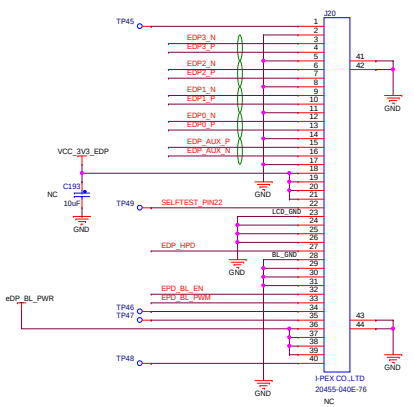



## DART-MX8M eDP/DP PATH - [Reference Design]

**iMX8M REQUIRES CROSS BETWEEN LANE0 & LANE2 !**




### 40 Pin eDP Connector



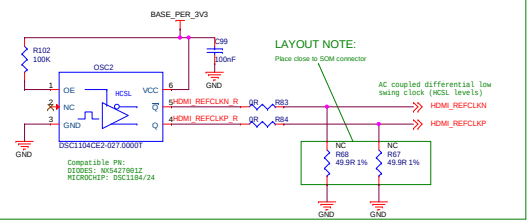

**eDP 40 Pin Connector**

**Board Connector: IPEX 20455-040E-76 (44 Pin)**
**Cable: IPEX 20453-040T-11 Assembly**
**Display Type: B156ZAN03.1 (H/W:0A)**

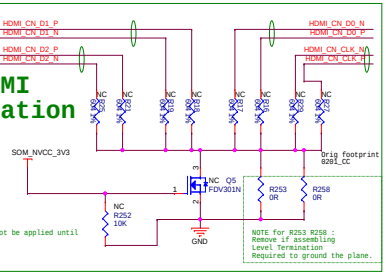
## DART-MX8M Notes and required circuitry:

**NOTE:** MX8M CAN CONNECT DIRECTLY TO :
HDMI_CN_SCL & HDMI_CN_SDA
HDMI_CN_CEC
HDMI_CN_HPD

### HDMI REFCLK




### DART-MX8M HDMI Level Termination




Variscite

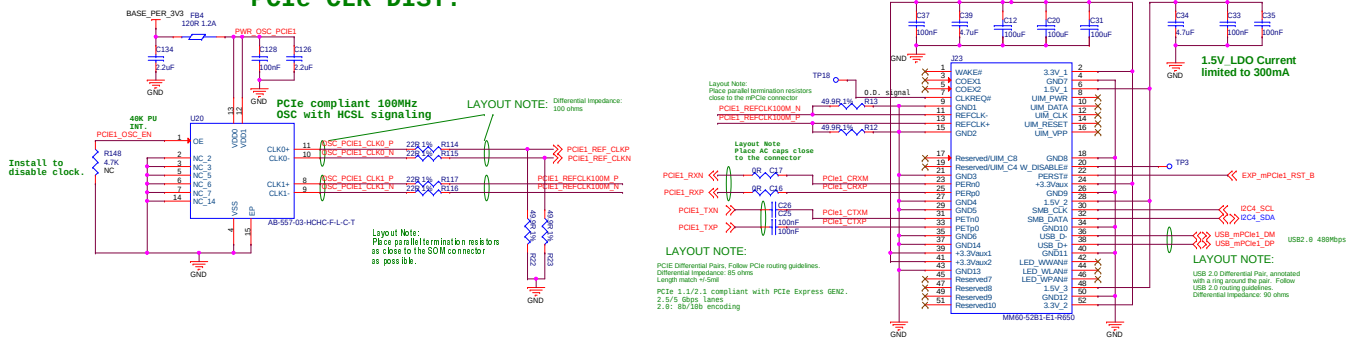
| | | | |
|---|---|---|---|
| Title: 06. HDMI , eDP | | | |
| Size: A2 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: <Approved By> | |
| Date: Monday, March 01, 2021 | | Sheet: 10 of 17 | |

# 07. PCIe, QSPI, MIPI-DSI, USB DEBUG

## mPCIexp CS

Customboard 5V power supply is limited to 3A, shared with Board's USB devices. Do not connect devices which exceed current limitation.

### PCIe CLK DIST.

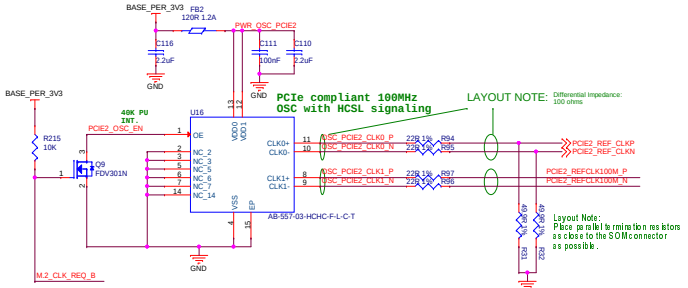


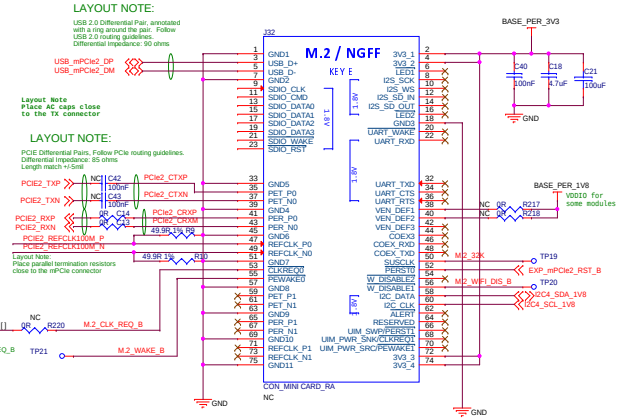




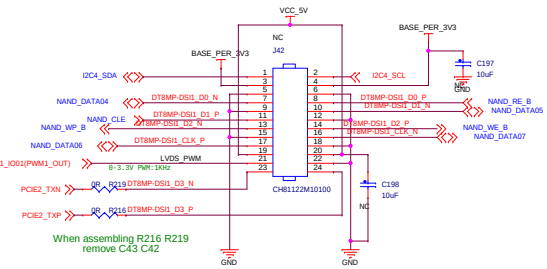
## M.2. ON PS - [Reference Design]

### PCIe CLK DIST.

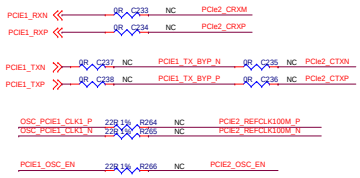



## DART-MX8MP MIPI-DSI ON PS Compatible to Symphony J7+J8




## PCIe1 TO M.2 PATH



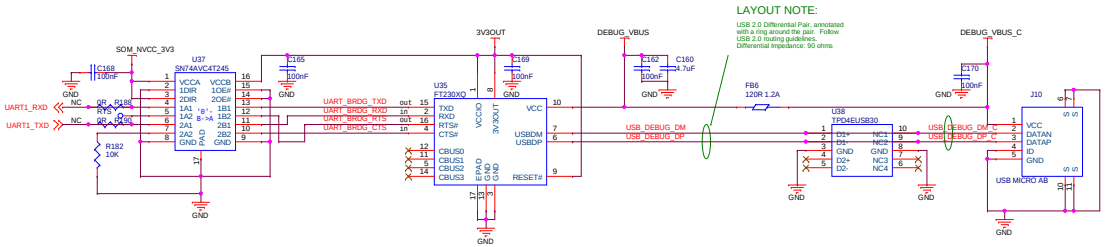
ASSY NOTE:
Customers requiring PCIe on DT8MP and DT8MM routed to M.2. connector (located on PS) should follow:

Remove
C16 C17 C26 C25 R116 R117 C13 C14 R96 R97

Assemble
C237 C238 (100nF)
C235 C236 (0 Ohm)
C233 C234 (0 Ohm)
R264 R265 (22 Ohm)

CLK_REQ_B path and enable not connected

## USB UART DEBUG

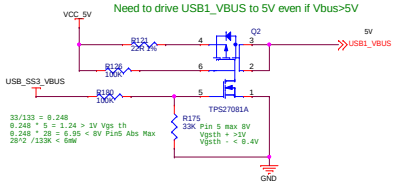



Variscite

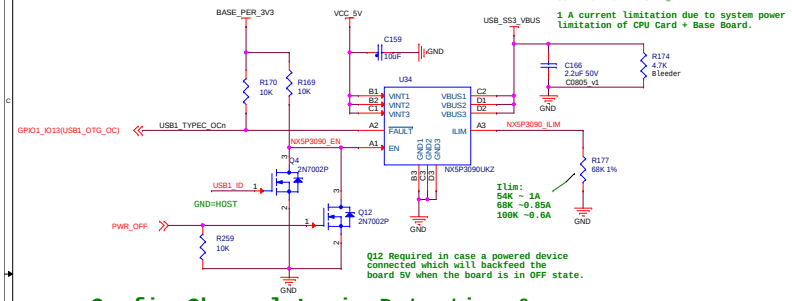
| | | | |
|---|---|---|---|
| Title: 07. PCIe, QSPI, MIPI-DSI, USB DEBUG | | | |
| Size: A2 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: <Approved By> | |
| Date: Monday, March 01, 2021 | | Sheet 11 of 17 | |

# 08. USB TYPE C, USB 3 HUB

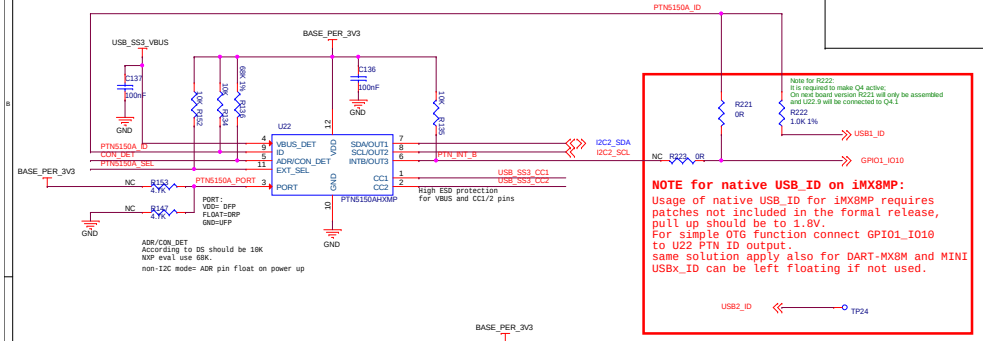
## USB#1 - DRP
## USB TYPE C




## 5V Source Load Switch



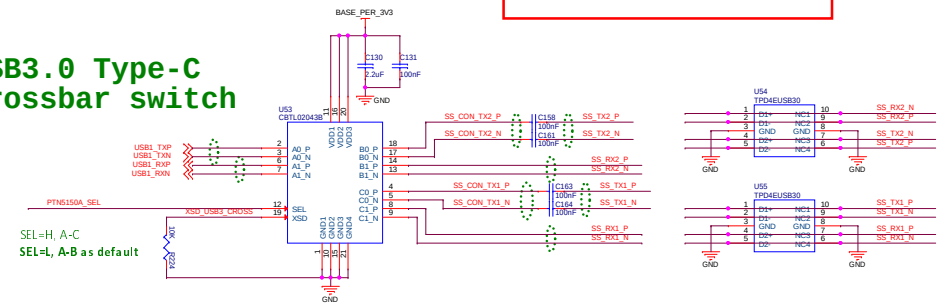

## Config Channel Logic Detection & Indication of Plug Orientation



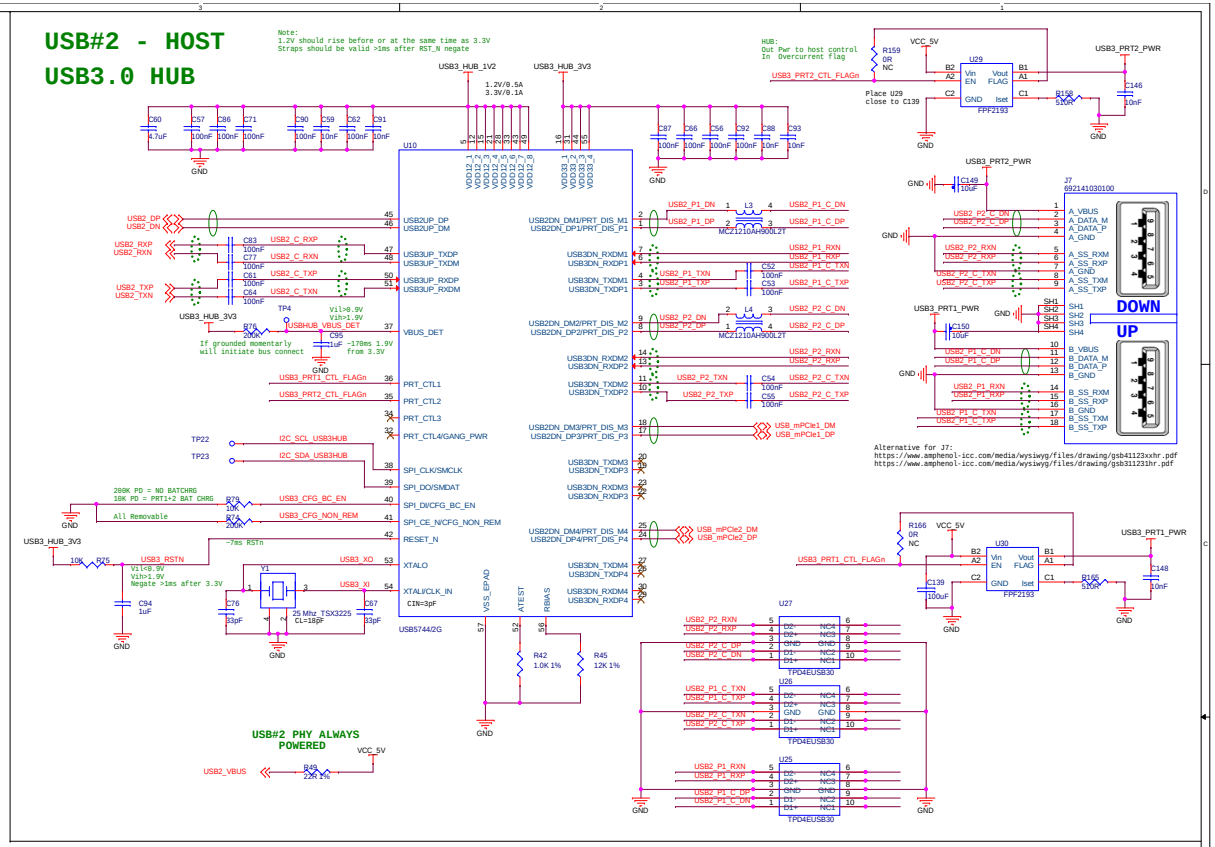




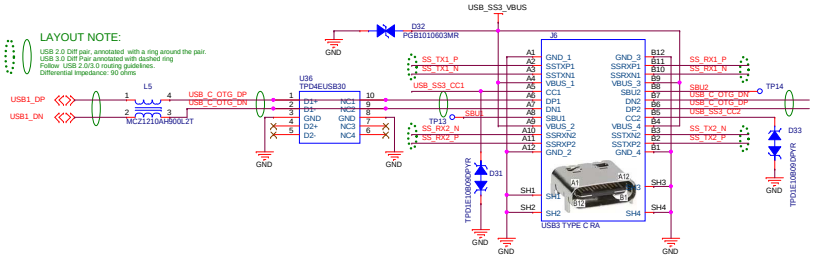
## USB3.0 Type-C crossbar switch




## USB#2 - HOST
## USB3.0 HUB




## LAYOUT NOTE:



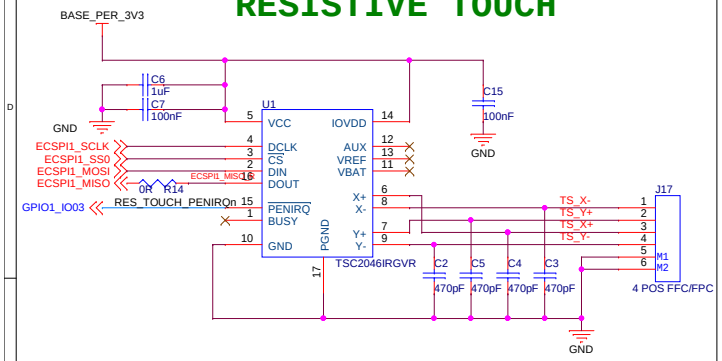

**Note:**
**VBUS active discharge replaced with bleeder**

Variscite

| | | | |
|---|---|---|---|
| Title: 08. USB TYPE C, USB3 HUB | | | |
| Size: A2 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Sunday, March 07, 2021 | | Sheet 12 of 17 | |

# 09. LVDS, TOUCH, JTAG, I2C EXP

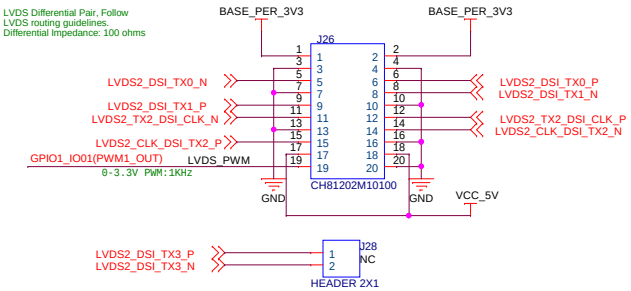
## RESISTIVE TOUCH




## LVDS CH1 DISPLAY

LAYOUT NOTE:

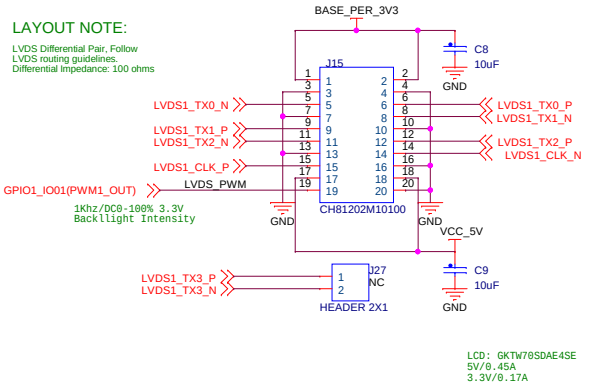
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms



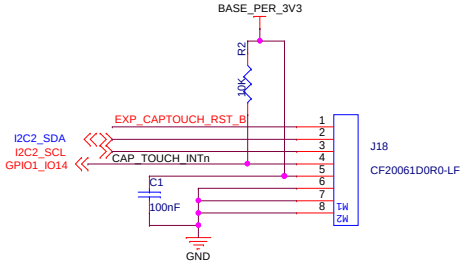

## LVDS DISPLAY CH0

LAYOUT NOTE:

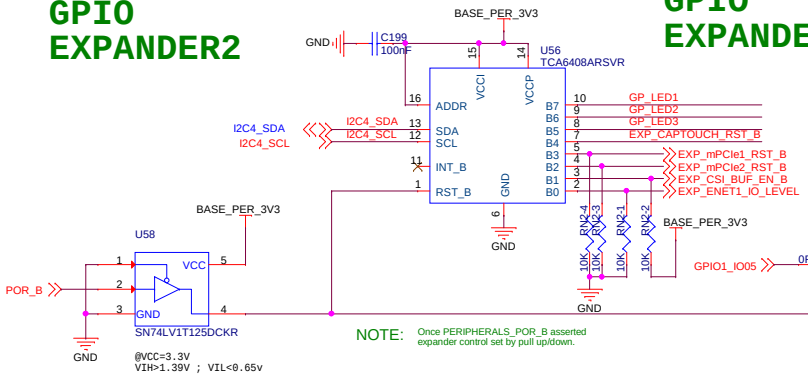
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms




## CAPACITIVE TOUCH

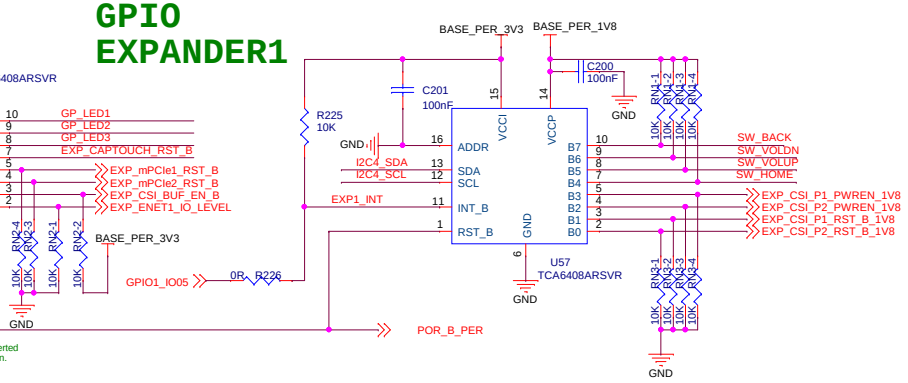



## GPIO EXPANDER2

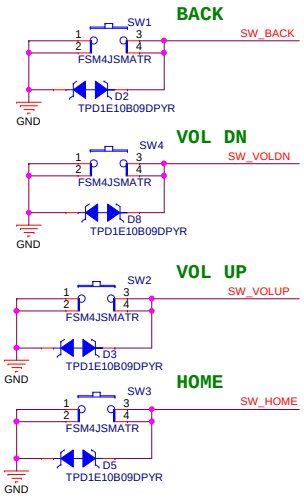



NOTE: Once PERIPHERALS_POR_B asserted expander control set by pull up/down.

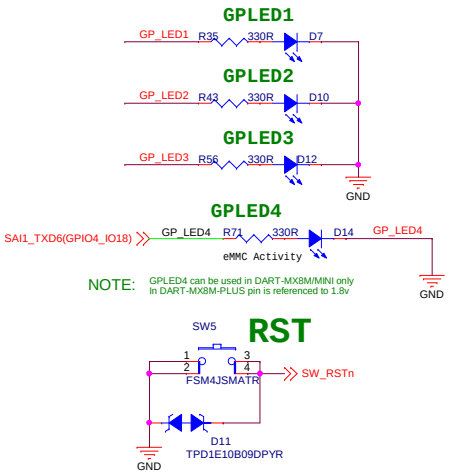
## GPIO EXPANDER1




## GP BUTTONS




## GP LEDS

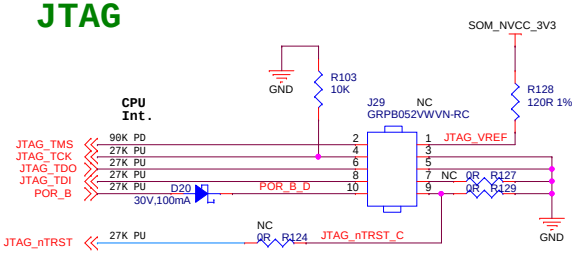



NOTE: GPLED4 can be used in DART-MX8M/MINI only In DART-MX8M-PLUS pin is referenced to 1.8v

## RST




## JTAG




NOTE: DT8MP JTAG_nTRST net connected to JTAG_MODE having 8.2K PD on SOM. Exposed for boundry scan.

**The new 10 pin smaller connector is now becoming an industry standard.**

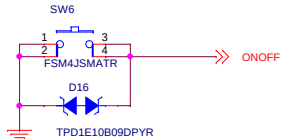
**The ARM DStream comes with a 10-pin connector. If you need a ribbon, they can be purhased at Digikey:**
**Samtec Inc MPN: FFSD-05-D-04.00-01-N**

**If you need to expand to a 20-pin connector for a different JTAG device, the expander board can also be purchased at Digikey:**
**Olimex LTD MPN: ARM-JTAG-20-10**

**https://www.digikey.com/products/en/development-boards-kits-programmers/accessories/783?k=JTAG%20adapter**

## ON/OFF

**PU Included on SOM**



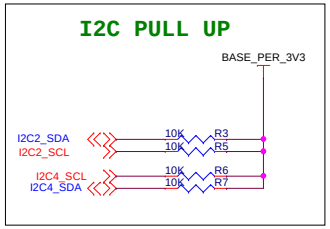

ONOFF: A brief connection to GND in OFF mode causes the internal power management state machine to change state to ON. In ON mode, a brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). An approximate 5 second or more connection to GND causes a forced OFF.

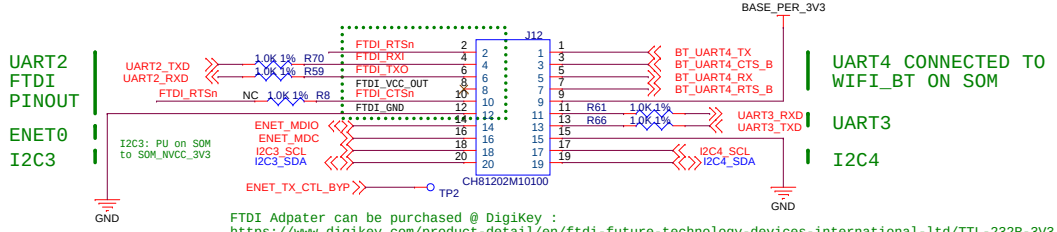
Not used leave NC

Variscite

| | | | |
|---|---|---|---|
| Title | 09. LVDS, TOUCH, JTAG, I2C EXP | | |
| Size A3 | Document Number VAR-DT8MCustomBoard | Project VAR-DT8MCustomBoard | Rev 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 13 of 17 | |

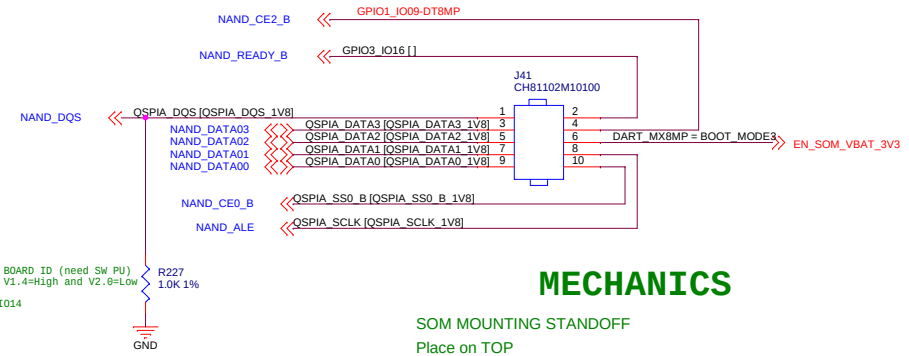
# 10. HEADERS, Mechanics, Pull Ups

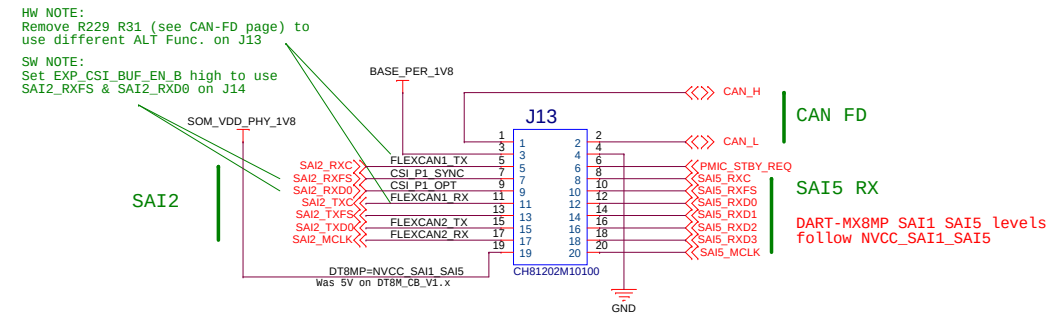


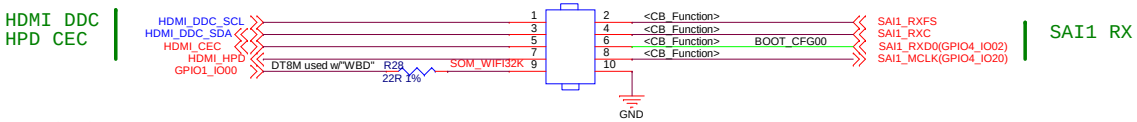



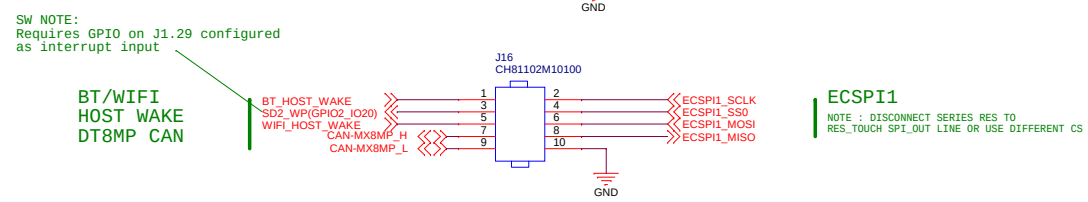

FTDI Adapter can be purchased @ DigiKey :
https://www.digikey.com/product-detail/en/ftdi-future-technology-devices-international-ltd/TTL-232R-3V3/768-1015-ND/1836393
See pinout: http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_TTL-232R_CABLES.pdf

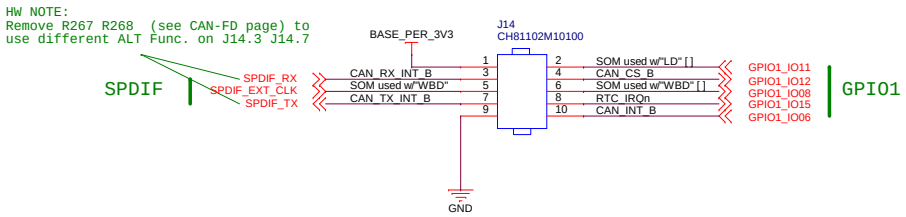
## QSPI HEADER



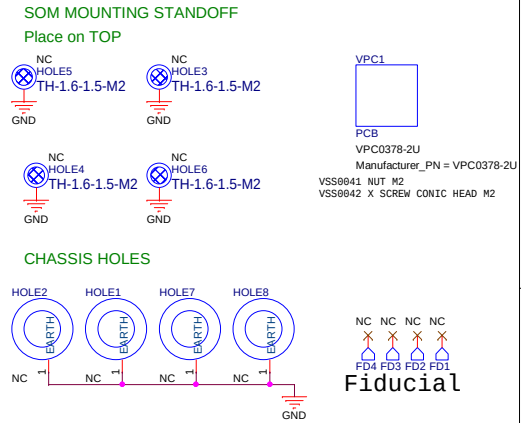




## MECHANICS




Variscite

| | | | |
|---|---|---|---|
| Title: 10. HEADERS, Mechanics, Pull Ups | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 14 of 17 | |

# 11. BOOT CONFIG & MODE

| | | | INT. BOOT | EXT. BOOT | |
|---|---|---|---|---|---|
| SAI1_RXD0(GPIO4_IO02) | <CB_Function> | BOOT_CFG00 | 0 | 0 | Need to Enable PU in DTS; See pp. 5 |
| SAI1_RXD1(GPIO4_IO03) | CSI_P2_TRIG | BOOT_CFG01 | 0 | 0 | |
| SAI1_RXD2(GPIO4_IO04) | ENET1_MDC | BOOT_CFG02 | 0 | 0 | |
| SAI1_RXD3(GPIO4_IO05) | ENET1_MDIO | BOOT_CFG03 | 0 | 0 | |
| SAI1_RXD4(GPIO4_IO06) | ENET1_RGMII_RD0 | BOOT_CFG04 | 0 | 0 | |
| SAI1_RXD5(GPIO4_IO07) | ENET1_RGMII_RD1 | BOOT_CFG05 | 0 | 0 | |
| SAI1_RXD6(GPIO4_IO08) | ENET1_RGMII_RD2 | BOOT_CFG06 | 0 | 0 | |
| SAI1_RXD7(GPIO4_IO09) | ENET1_RGMII_RD3 | BOOT_CFG07 | 0 | 0 | |
| SAI1_TXD0(GPIO4_IO12) | ENET1_RGMII_TD0 | BOOT_CFG08 | 0 | 0 | |
| SAI1_TXD1(GPIO4_IO13) | ENET1_RGMII_TD1 | BOOT_CFG09 | 0 | 0 | |
| SAI1_TXD2(GPIO4_IO14) | ENET1_RGMII_TD2 | BOOT_CFG10 | 0 | 1 | |
| SAI1_TXD3(GPIO4_IO15) | ENET1_RGMII_TD3 | BOOT_CFG11 | 0 | 0 | |
| SAI1_TXD4(GPIO4_IO16) | ENET1_RGMII_TX_CTL | BOOT_CFG12 | 0 | 1 | |
| SAI1_TXD5(GPIO4_IO17) | ENET1_RGMII_TXC | BOOT_CFG13 | 1 | 0 | |
| SAI1_TXD6(GPIO4_IO18) | GP_LED4 | BOOT_CFG14 | 0 | 0 | |
| SAI1_TXD7(GPIO4_IO19) | CSI_P1_TRIG | BOOT_CFG15 | 0 | 0 | |

10K R52 NC BOOT_CFG00 <CB_Function> SAI1_RXD0(GPIO4_IO02)
10K R228 NC BOOT_CFG01 CSI_P2_TRIG SAI1_RXD1(GPIO4_IO03)
10K R53 NC BOOT_CFG02 ENET1_MDC SAI1_RXD2(GPIO4_IO04)
10K R93 NC BOOT_CFG03 ENET1_MDIO SAI1_RXD3(GPIO4_IO05)
10K R58 NC BOOT_CFG04 ENET1_RGMII_RD0 SAI1_RXD4(GPIO4_IO06)
10K R55 NC BOOT_CFG05 ENET1_RGMII_RD1 SAI1_RXD5(GPIO4_IO07)
10K R92 NC BOOT_CFG06 ENET1_RGMII_RD2 SAI1_RXD6(GPIO4_IO08)
10K R54 NC BOOT_CFG07 ENET1_RGMII_RD3 SAI1_RXD7(GPIO4_IO09)

GND

POR_B_PER
R254 10K
C230 4.7uF
GND
POR_B_PER_DELAY

SOM_NVCC_3V3
C103 100nF GND

Vih >1.39V
Vil <0.65V

BOOT_CFG

U19 SN74LV1T125DCKR
U18 SN74LV1T125DCKR
U17 SN74AUP1G240DCK
VCC GND

10K R91 NC BOOT_CFG08 ENET1_RGMII_TD0 SAI1_TXD0(GPIO4_IO12)
10K R64 NC BOOT_CFG09 ENET1_RGMII_TD1 SAI1_TXD1(GPIO4_IO13)
10K R89 BOOT_CFG10 ENET1_RGMII_TD2 SAI1_TXD2(GPIO4_IO14)
10K R112 NC BOOT_CFG11 ENET1_RGMII_TD3 SAI1_TXD3(GPIO4_IO15)
10K R90 BOOT_CFG12 ENET1_RGMII_TX_CTL SAI1_TXD4(GPIO4_IO16)
C104 100nF GND
10K R107 BOOT_CFG13 ENET1_RGMII_TXC SAI1_TXD5(GPIO4_IO17)
10K R113 NC BOOT_CFG14 GP_LED4 SAI1_TXD6(GPIO4_IO18)
10K R111 NC BOOT_CFG15 CSI_P1_TRIG SAI1_TXD7(GPIO4_IO19)

**U17 U18 U19 Note:**
* Tristate buffers required not to pull ENET1 to 3.3V while running @ lower voltage.
* Buffers required for DART-MX8M & DART-MX8M-MINI
* For DART-MX8M-PLUS only U19 required

**Notes:**
a. Sampled on rising edge of POR_B
b. SOC PD during POR_B and after on BOOT CFG[15:0] and BOOTMODE[1:0]
c. BOOT_MODE[1:0] ="10" is Internal Boot - Always used.
d. Active boot cfg for one dip sw sel EXTERNAL/INTERNAL

**DART-MX8M-MINI Notes:**
b. Boot config lines do not follow the Mini datasheet in full DART-MX8M-MINI have added logic to be compatible to DART-MX8M

**DART-MX8M-PLUS Notes:**
a. Boot configuration set only by SAI1_TXD2 connected on DART via buffer to BOOT_MODE0

*i.MX8M Plus Boot Mode*

| BOOT_MODE3 | BOOT_MODE2 | BOOT_MODE1 | BOOT_MODE0 | Boot Modes |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Boot From Internal Fuses |
| 0 | 0 | 0 | 1 | USB Serial Download |
| 0 | 0 | 1 | 0 | USDHC3 (eMMC boot only, SD3 8-bit) Default |
| 0 | 0 | 1 | 1 | USDHC2 (SD boot only, SD2) |

CustomBoard Net: BOOT_MODE0 SAI1_TXD2 EN_SOM_VBAT_3V3 BOOT_MODE1

**DART-MX8MP BOOT MODE**

SOM_NVCC_3V3
R106 10K
BOOT_CFG
SW7 TDA01H0SB1R
D21
GND

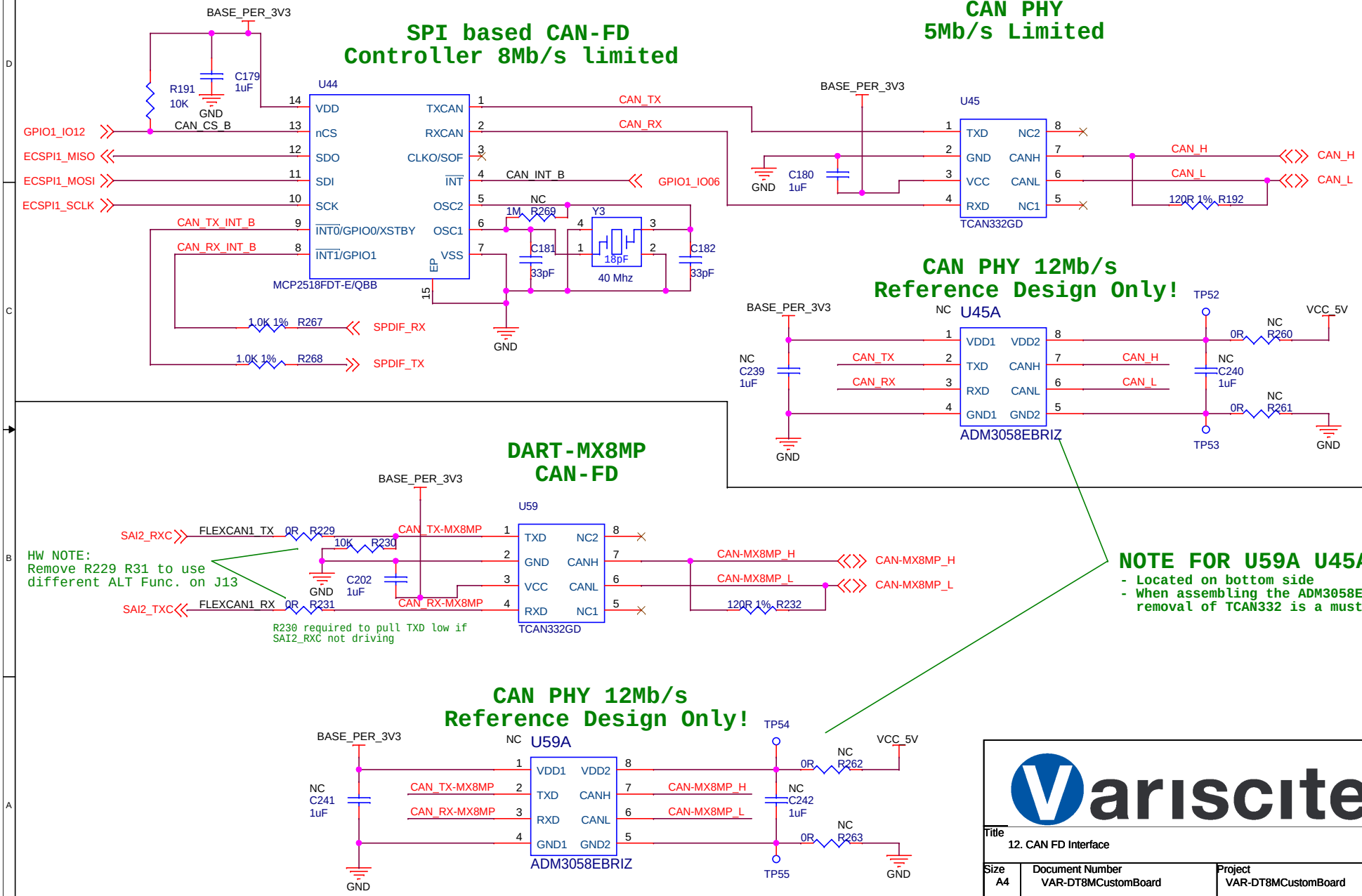
BOOT CFG PRIORITY:
H Ext. SD Card
L Int. eMMC

SOM_NVCC_3V3
R87 4.7K
R100 4.7K NC
R88 10K NC
R99 4.7K
BOOT_MODE0
BOOT_MODE1
GND

Variscite

| | | | |
|---|---|---|---|
| Title: 11. BOOT CONFIG & MODE | | | |
| Size: B | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 15 of 17 | |

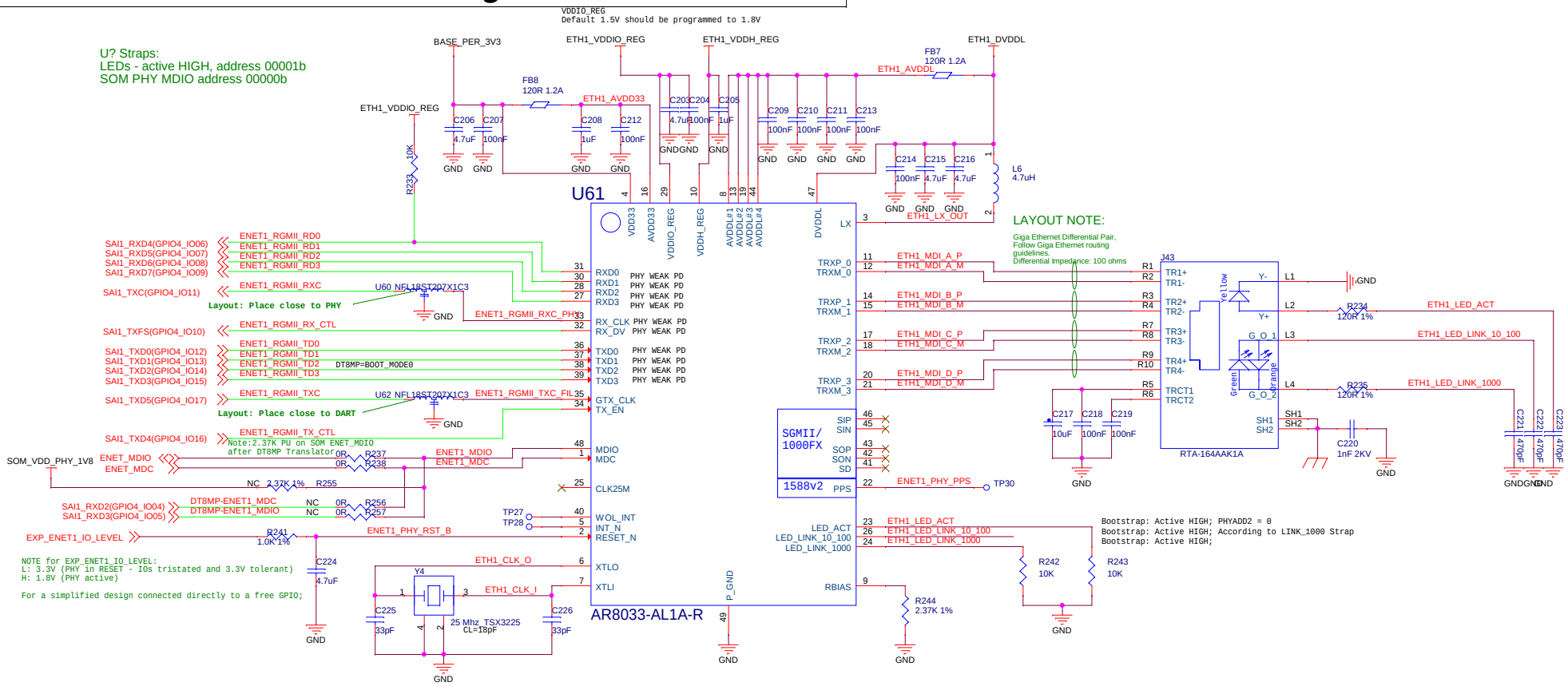
# 13. CAN FD Interface




Variscite

| | | | |
|---|---|---|---|
| Title: 12. CAN FD Interface | | | |
| Size: A4 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 16 of 17 | |

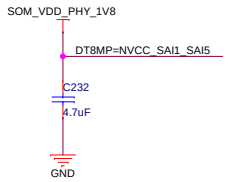
# 13. DART-MX8MP- ENET1 Gigabit Ethernet



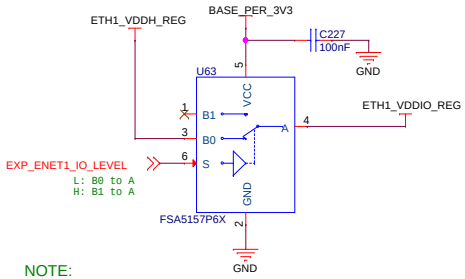

NOTE:
For DT8MP net SOM_VDD_PHY_1V8 connected to NVCC_SAI1_SAI5 which is an output from the DT8MP programmable PMIC LDO.

This output voltage will set SAI1 and SAI5 pads voltage level;
With DT8MCustomBoard-V1.x and earlier it is set to 3.3V.
On DT8MCustomBoard-V2.x it is set to 1.8V for RGMII.

Bypass with 4.7uF min. 6.3V capacitor.




NOTE for U63:
Required for compatibility to DT8M & DT8MM
where SAI1 levels are fixed to 3.3V;




NOTE:
EXP_ENET1_IO_LEVEL = LOW causes PHY RST_B to be asserted;
PHY ENET1 signals become 3.3V tolerant.
This is accomplished by shorting ETH1_VDDIO_REG to ETH1_VDDH_REG
according to AR8033 Datasheet.

NOTE:
Test points below used to access
DT8M & DT8MM SAI1 signals;

Levels are fixed to 3.3V by modules;

SAI1_RXD2(GPIO4_IO04) DT8MP-ENET1_MDC TP50
SAI1_RXD3(GPIO4_IO05) DT8MP-ENET1_MDIO TP51

SAI1_RXD4(GPIO4_IO06) ENET1_RGMII_RD0 TP31
SAI1_RXD5(GPIO4_IO07) ENET1_RGMII_RD1 TP33
SAI1_RXD6(GPIO4_IO08) ENET1_RGMII_RD2 TP37
SAI1_RXD7(GPIO4_IO09) ENET1_RGMII_RD3 TP35

SAI1_TXC(GPIO4_IO11) ENET1_RGMII_RXC TP40
SAI1_TXFS(GPIO4_IO10) ENET1_RGMII_RX_CTL TP41

SAI1_TXD0(GPIO4_IO12) ENET1_RGMII_TD0 TP32
SAI1_TXD1(GPIO4_IO13) ENET1_RGMII_TD1 TP34
SAI1_TXD2(GPIO4_IO14) ENET1_RGMII_TD2 TP38
SAI1_TXD3(GPIO4_IO15) ENET1_RGMII_TD3 TP39

SAI1_TXD5(GPIO4_IO17) ENET1_RGMII_TXC TP36
SAI1_TXD4(GPIO4_IO16) ENET1_RGMII_TX_CTL TP42

Variscite

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|---|---|---|---|
| Title: 13. Ethernet2 | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 2.0_R1.0 |
| Designer: Leonid S. | | Approved By: | |
| Date: Monday, March 01, 2021 | | Sheet 17 of 17 | |