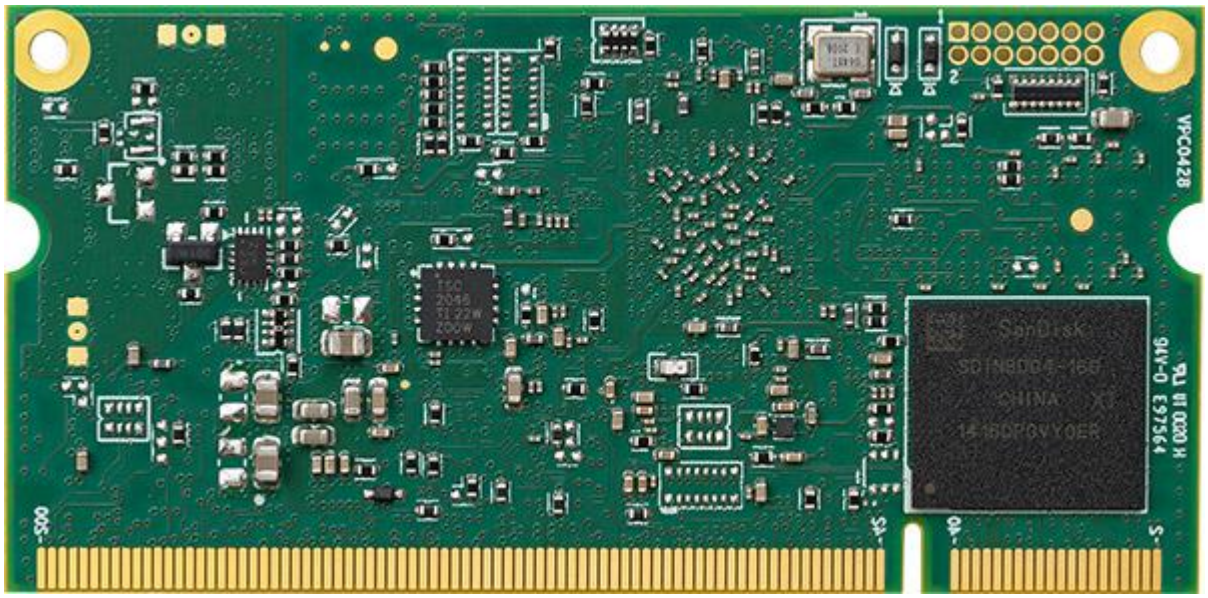
VARISCITE LTD.

VAR-SOM-AM62 V1.x Datasheet

TI Sitara™ AM62x - based System-on-Module



VARISCITE LTD.

VAR-SOM-AM62 Datasheet

© 2022 Variscite Ltd.
All Rights Reserved. No part of this document may be photocopied, reproduced, stored in a retrieval system, or transmitted, in any form or by any means whether, electronic, mechanical, or otherwise without the prior written permission of Variscite Ltd.
No warranty of accuracy is given concerning the contents of the information contained in this publication. To the extent permitted by law no liability (including liability to any person by reason of negligence) will be accepted by Variscite Ltd., its subsidiaries or employees for any direct or indirect loss or damage caused by omissions from or inaccuracies in this document.
Variscite Ltd. reserves the right to change details in this publication without notice. Product and company names herein may be the trademarks of their respective owners.

Variscite Ltd.
4, Hamelacha Street
Lod
P.O.B 1121
Airport City, 70100
ISRAEL

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

1. Document Revision History

Revision	Date	Notes
1.0	November 17, 2022	Initial - Preliminary
1.01	January 26, 2023	Updated specifications in sections: 4.2,4.3,5.17,5.2,5.8 Updated notes for SOM pins 30,74,1,16,96,97
1.02	February 1, 2023	Updated pinout for pins 50,51
1.03	February 19, 2023	Updated section 10.4, added power consumption values.
1.04	February 23, 2023	Updated section 11
1.05	March 2, 2023	Updated notes pins 36,85,174,176
1.06	March 16, 2023	Updated notes section 8.11, pins 174,176 Updated notes pins 30,74
1.07	April 16, 2023	Updated section 8.7 features
1.08	September 26, 2023	Updated notes pins 104,106,130,134,136,140,141,146,148 Updated notes JTAG pins Table 91 Updated features following TI AM62x datasheet update (Rev 4): • CSI data rate (sections 4.2, 5.1.6, 8.3.1) • Security features (section 5.1.9) • MMC/SD features (section 5.1.13)
1.09	June 10, 2024	Updated section 12.2 Heat sink P/N
1.10	Feb 26, 2025	Updated note for pin 36 in Tables 21, 95 Corrected Assy for pin 195 in Table 96 Added notes for pins 128,153 in Table 99 Updated notes table 1 Updated notes section 12.2 Updated Table 98 Added note for pin 80 Updated note for BOOTMODE pins Updated section 4.3

2. Table of Contents

3. List of Tables

4. Overview

4.1 General Information

The VAR-SOM-AM62 offers a high-performance processing for a low-power System-on-Module. The product is based on the AM62x Sitara™ MPU family of application processors.

The AM62x Sitara™ MPU family of application processors are built for Linux® application development. With scalable Arm® Cortex®-A53 performance and embedded features, such as: dual-display support and 3D graphics acceleration, along with an extensive set of peripherals that make the AM62x device well-suited for a broad range of industrial and automotive applications while offering intelligent features and optimized power architecture as well.

The VAR-SOM-AM62 provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

- Symphony-Board – evaluation board
  - ✓ Carrier Board, compatible with VAR-SOM-AM62
  - ✓ Schematics
- VAR-DVK-AM62 full development kit, including:
  - ✓ Symphony-Board
  - ✓ VAR-SOM-AM62
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

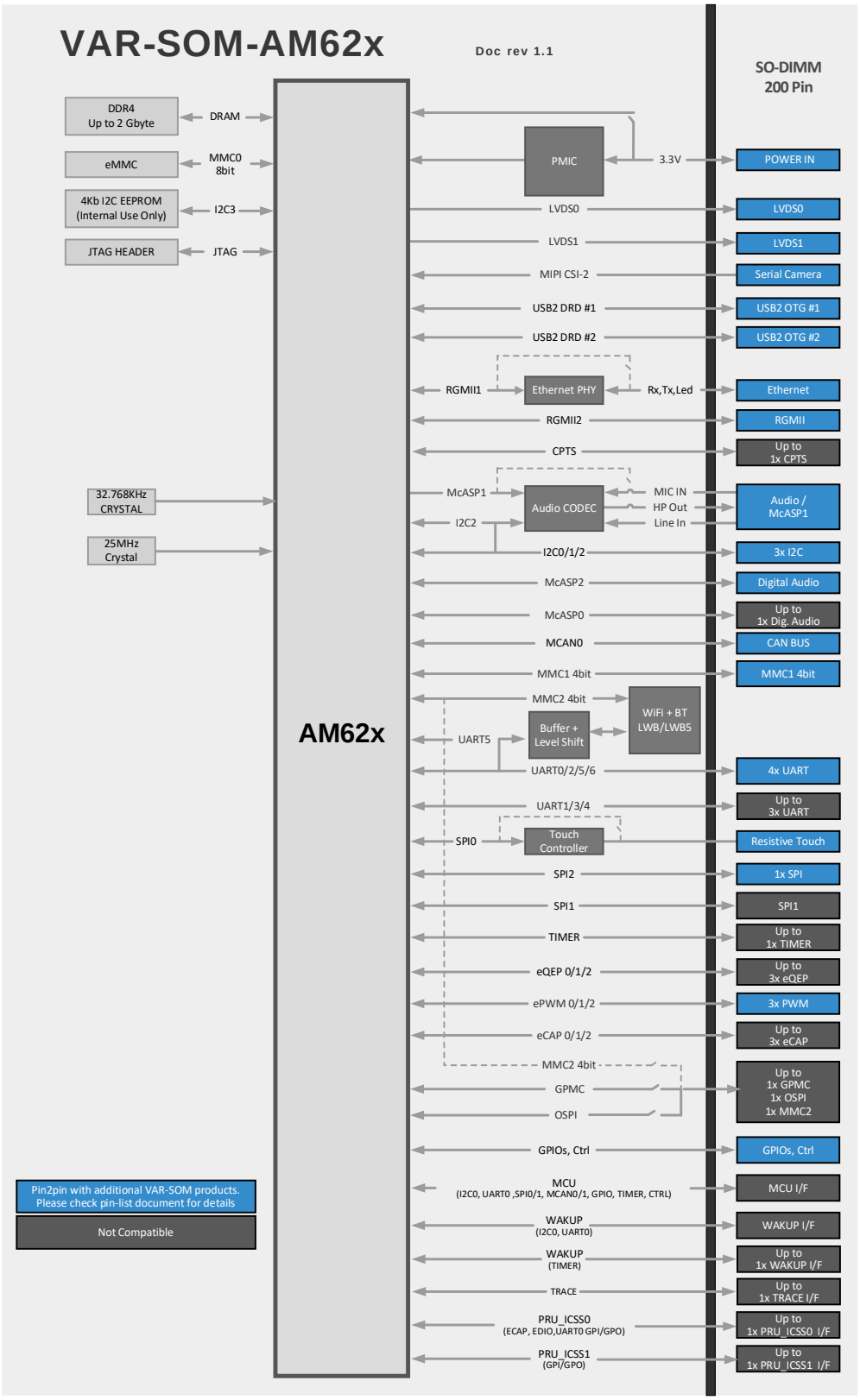
Contact Variscite support services for further information: support@variscite.com.

4.2 Feature Summary

- TI AM62x Sitara series SOC
  - Up to 4x Cortex A53 @ 1.4 GHz
  - 1x Cortex M4F up to @ 400 MHz
  - 1x PRUSS up to @ 333 MHz (only in industrial graded modules)
- Graphics Processing Unit
  - 3D GPU with OpenGL ES 3.1 & Vulkan1.2
  - 2D graphics capable
- Memory
  - Up to 4GB DDR4-3200 RAM @ 800MHz
  - 8-bit up to 128GB eMMC boot and storage
- Display Support
  - 2x OLDI/LVDS interface 4-lane each - supporting up to 1920x1080@60fps
- Networking
  - 2x 10/100/1000 Mbit/s Ethernet Interface
  - Certified Wi-Fi 802.11 ac/a/b/g/n
  - Bluetooth: 5.2/BLE
- Camera
  - 1x MIPI CSI-2 – CMOS Serial camera Interface 4 lanes
  - Support for 1,2,3 or 4 data lane mode up to 1.5Gbps
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - Up to 3x Digital audio (McASP)
- USB
  - 2x USB 2.0 Host/Device
- Media and data storage
  - SDIO/MMC
  - OSPI/QSPI
  - GPMC parallel bus
- Other Interfaces
  - Resistive touch controller
  - Serial interfaces (SPI, I2C, UART, ePWM, eCAP, eQEP, CAN-FD, JTAG)
  - GPIOs
- Single power supply: 3.3V
- Dimensions (W x L x H): 67.6 mm x 33 mm x 3.4 mm
- Industrial temperature range: -40°C to 85°C

4.3 Block Diagram

Figure 1 : VAR-SOM-AM62 Block Diagram



5. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-AM62.

5.1 AM62x Sitara™ MPU

5.1.1 Overview

The low-cost AM62x Sitara™ MPU family of application processors are built for Linux® application development. With scalable Arm® Cortex®-A53 performance and embedded features, such as: dual-display support and 3D graphics acceleration, along with an extensive set of peripherals that make the AM62x device well-suited for a broad range of industrial and automotive applications while offering intelligent features and optimized power architecture as well.

Some of these applications include:

- Industrial HMI
- EV charging stations
- Touchless building access
- Driver monitoring systems

Industrial and Automotive functional safety requirements can be addressed using the integrated Cortex-M4F cores and dedicated peripherals, which can all be isolated from the rest of the AM62x processor.

The 3-port Gigabit Ethernet switch has one internal port and two external ports with Time-Sensitive Networking (TSN) support. An additional PRU module on the device enables real-time I/O capability for customer's own use cases. In addition, the extensive set of peripherals included in AM62x enables system-level connectivity, such as: USB, MMC/SD, Camera interface, OSPI, CAN-FD and GPMC.

The AM62x device also supports secure boot for IP protection with the built-in Hardware Security Module (HSM) and employs advanced power management support for portable and power-sensitive applications.

5.1.2 AM62x Sitara Block Diagram

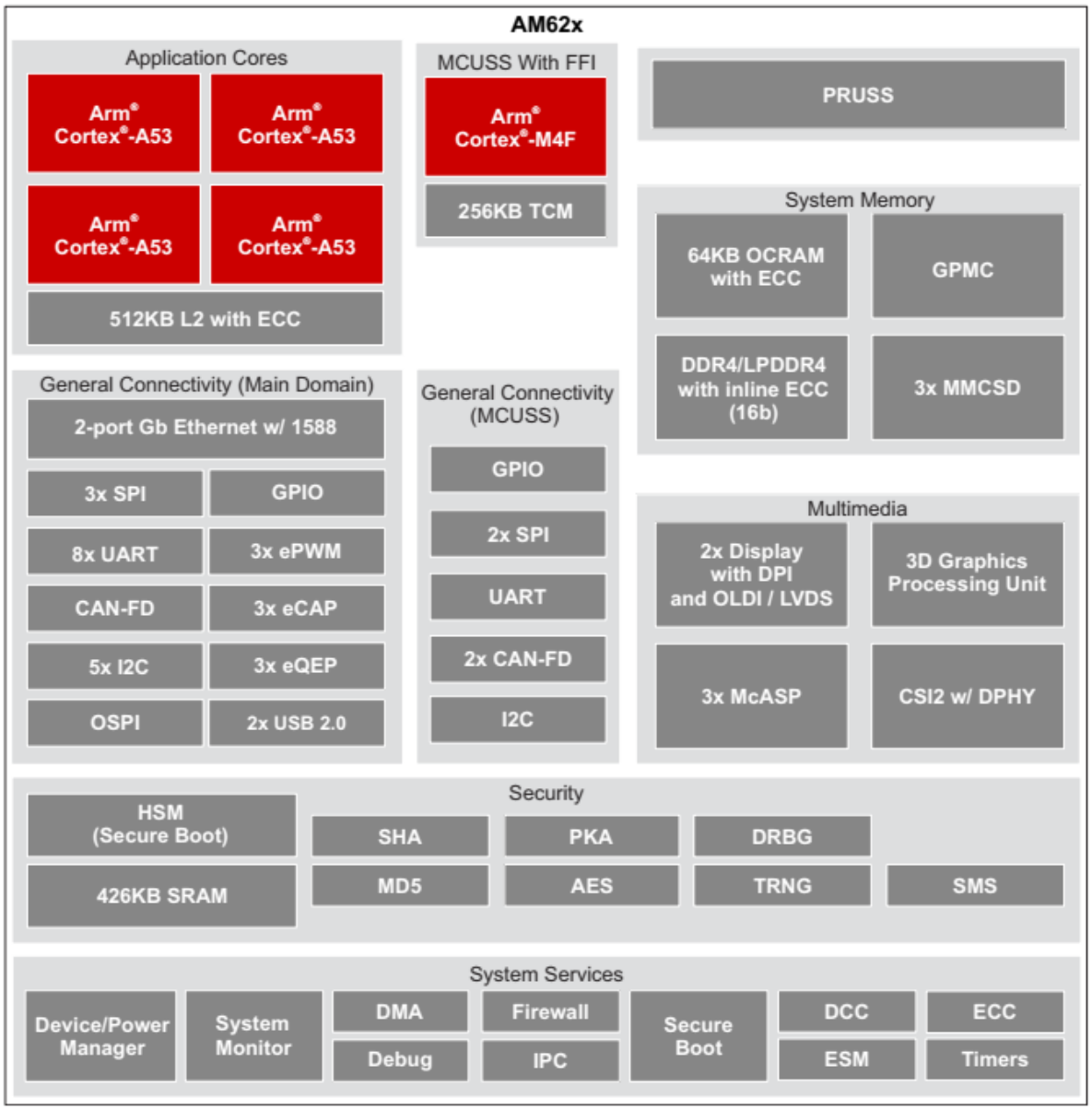


Figure 2 AM62x Sitara Block Diagram

5.1.3 Arm Cortex-A53 Subsystem (A53SS)

- Up to Quad 64-bit Arm® Cortex®-A53 microprocessor subsystem at 1.4 GHz
  - Quad-core Cortex-A53 cluster with 512KB L2 shared cache with SECDED ECC
  - Each A53 Core has 32KB L1 DCache with SECDED ECC and 32KB L1 ICache with Parity

5.1.4 MCU Arm Cortex M4F Subsystem (MCU_M4FSS)

- Single-core Arm® Cortex®-M4F MCU at up to 400MHz
  - 256KB SRAM with SECDED ECC

The Integrated single Arm Cortex-M4F core can be configured as an isolated safety MCU or general purpose MCU.

5.1.5 Arm Cortex-R5F Processor (R5FSS)

- Armv7-R architecture
- R5FSS Memory System
  - 32KB Instruction Cache
    - 4x8KB ways
    - SECDED ECC protected per 64 bits
  - 32KB Data Cache
    - 4x8KB ways
    - SECDED ECC protected per 32 bits
  - 64KB tightly-coupled memory (TCM) per CPU
    - SECDED ECC protected per 32 bits
    - TCM hard error cache Implemented in CPU
    - Readable/writable from system
    - TCMs initialized (to 0's) at reset
    - 32KB TCMA (ATCM)
    - 16KB TCMB0 (B0TCM)
    - 16KB TCMB1 (B1TCM)
- Full-precision Floating Point (VFPv3)
- 16-region Memory Protection Unit (MPU)
- 8 breakpoints, 8 watch points
- CoreSight Debug Access Port (DAP)
- CoreSight ETM-R5 interface (CTI, ETM)
- Performance Monitoring Unit (PMU)
- 32-bit to 36-bit Region-based Address Translation (RAT) on memory access initiators
- Integrated Vectored Interrupt Manager (VIM) per core with 256 Interrupt Inputs each
  - Programmable interrupt priority (4-bit)
  - Programmable interrupt enable mask
  - Software-generated interrupts
  - Synchronous clock domain crossing on all core interfaces

5.1.6 Multimedia

- Display subsystem
  - 1920x1080 @ 60fps
  - Up to 165 MHz pixel clock support with Independent PLL
  - OLDI/LVDS (4 lanes - 2x)
  - Support safety feature such as freeze frame detection and MISR data check
- 3D Graphics Processing Unit
  - 1 pixel per clock or higher
  - Fillrate greater than 500 Mpixels/sec
  - >500 MTexels/s, >8 GFLOPs
  - Supports at least 2 composition layers
  - Supports up to 2048x1080 @60fps
  - Supports ARGB32, RGB565 and YUV formats
  - 2D graphics capable
  - OpenGL ES 3.1, Vulkan 1.2
- One Camera Serial interface (CSI-Rx) - 4 Lane with DPHY
  - MIPI CSI-2 1.3 Compliant + MIPI-DPHY 1.2
  - Support for 1,2,3 or 4 data lane mode up to 1.5Gbps
  - ECC verification/correction with CRC check + ECC on RAM
  - Virtual Channel support (up to 16)
  - Ability to write stream data directly to DDR via DMA

5.1.7 Memory Subsystem:

- Internal processor's on-chip RAM up to 816KB
  - 64KB of On-chip RAM (OCSRAM) with SECDED ECC, Can be divided into smaller banks in increments of 32KB for as many as 2 separate memory banks
  - 256KB of On-chip RAM with SECDED ECC in SMS Subsystem
  - 176KB of On-chip RAM with SECDED ECC in SMS Subsystem for TI security firmware
  - 256KB of On-chip RAM with SECDED ECC in Cortex-M4F MCU subsystem
  - 64KB of On-chip RAM with SECDED ECC in Device/Power Manager Subsystem
- DDR Subsystem (DDRSS)
  - Supports DDR4 memory types up to 4GB
  - 16-Bit data bus with inline ECC
  - Supports speeds up to 1600 MT/s
  - Max addressable range

5.1.8 Functional Safety

- Functional Safety-Compliant targeted [Industrial]
  - Developed for functional safety applications
  - Documentation will be available to aid IEC 61508 functional safety system design
  - Systematic capability up to SIL 3 targeted
  - Hardware Integrity up to SIL 2 targeted
  - Safety-related certification
    - IEC 61508 by TUV SUD planned
- Functional Safety-Compliant targeted [Automotive]
  - Developed for functional safety applications
  - Documentation will be available to aid ISO 26262 functional safety system design
  - Systematic capability up to ASIL D targeted
  - Hardware integrity up to ASIL B targeted
  - Safety-related certification
    - ISO 26262 by TUV SUD planned
- AEC-Q100 qualified

5.1.9 Security

- Secure boot supported
  - Hardware-enforced Root-of-Trust (RoT)
  - Support to switch RoT via backup key
  - Support for takeover protection, IP protection, and anti-roll back protection
- Trusted Execution Environment (TEE) supported
  - Arm TrustZone® based TEE
  - Extensive firewall support for isolation
  - Secure watchdog/timer/IPC
  - Secure storage support
  - Replay Protected Memory Block (RPMB) support
- Dedicated Security Controller with user programmable HSM core and dedicated security DMA & IPC subsystem for isolated processing
- Cryptographic acceleration supported
  - Session-aware cryptographic engine with ability to auto-switch key-material based on incoming data stream
  - Supports cryptographic cores
    - AES – 128-/192-/256-Bit key sizes
    - SHA2 – 224-/256-/384-/512-Bit key sizes
    - DRBG with true random number generator
    - PKA (Public Key Accelerator) to Assist in RSA/ECC processing for secure boot
- Debugging security
  - Secure software controlled debug access
  - Security aware debugging

5.1.10 PRU Subsystem

- Dual-core Programmable Real-Time Unit Subystem (PRUSS) running up to 333 MHz, available only in industrial graded processors
- Intended for driving GPIO for cycle accurate protocols such as additional:
  - General Purpose Input/Output (GPIO)
  - UARTs
  - I2C
  - External ADC
- 16KByte program memory per PRU with SECDED ECC
- 8KB data memory per PRU with SECDED ECC
- 32KB general purpose memory with SECDED ECC
- CRC32/16 HW accelerator
- Scratch PAD memory with 3 banks of 30 x 32-bit registers
- 1 Industrial 64-bit timer with 9 capture and 16 compare events, along with slow and fast compensation
- 1 interrupt controller (INTC), minimum of 64 input events supported

5.1.11 High-Speed Interfaces

- Integrated Ethernet switch supporting (total 2 external ports)
  - RMII (10/100) or RGMII (10/100/1000)
  - IEEE1588 (Annex D, Annex E, Annex F with 802.1AS PTP)
  - Clause 45 MDIO PHY management
  - Packet Classifier based on ALE engine with 512 classifiers
  - Priority based flow control
  - Time sensitive networking (TSN) support
  - Four CPU H/W interrupt Pacing
  - IP/UDP/TCP checksum offload in hardware
- Two USB2.0 Ports
  - Port configurable as USB host, USB peripheral, or USB Dual-Role Device (DRD mode)
  - Integrated USB VBUS detection
  - Trace over USB supported

5.1.12 General Connectivity

- 9x Universal Asynchronous Receiver-Transmitters (UART)
- 5x Serial Peripheral Interface (SPI) controllers
- 5x Inter-Integrated Circuit (I2C) ports
- 3x Multichannel Audio Serial Ports (McASP)
  - Transmit and Receive Clocks up to 50 MHz
  - Up to 16/10/6 Serial Data Pins across 3 McASP with Independent TX and RX Clocks
  - Supports Time Division Multiplexing (TDM) Inter-IC Sound (I2S), and Similar Formats
  - Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 Formats)
  - FIFO Buffers for Transmit and Receive (256 Bytes)
  - Support for audio reference output clock
- 3x enhanced PWM modules (ePWM)
- 3x enhanced Quadrature Encoder Pulse modules (eQEP)
- 3x enhanced Capture modules (eCAP)
- General-Purpose I/O (GPIO), All LVCMOS I/O can be configured as GPIO

- 3x Controller Area Network (CAN) modules with CAN-FD support
    - Conforms w/ CAN Protocol 2.0 A, B and ISO11898-1
    - Full CAN FD support (up to 64 data bytes)
    - Parity/ECC check for Message RAM
    - Speed up to 8Mbps

5.1.13 Media and Data Storage

- 3x Multi-Media Card/Secure Digital® (MMC/SD®) interface
    - 1x 8-bit eMMC interface up to HS200 speed
    - 2x 4-bit SD/SDIO interface up to UHS-I
    - Compliant with eMMC 5.1, SD 3.0 and SDIO Version 3.0
- 1× General-Purpose Memory Controller (GPMC) up to 133 MHz
    - Flexible 8- and 16-Bit Asynchronous Memory Interface With up to four Chip Selects (NAND)
    - Uses BCH Code to Support 4-, 8-, or 16-BitECC
    - Uses Hamming Code to Support 1-Bit ECC
    - Error Locator Module (ELM)
        - Used With the GPMC to Locate Addresses of Data Errors From Syndrome Polynomials Generated Using a BCH Algorithm
        - Supports 4-, 8-, and 16-Bit Per 512-Byte Block Error Location Based on BCH Algorithms
- OSPI/QSPI with DDR / SDR support
    - Support for Serial NAND and Serial NOR flash devices
    - 4GBytes memory address support
    - XIP mode with optional on-the-fly encryption

5.1.14 Power Management

- Low power modes supported by Device/Power Manager
    - DeepSleep
    - MCU Only
    - Standby
    - Dynamic frequency scaling for Cortex-A53

5.2 Memory

5.2.1 RAM

The VAR-SOM-AM62 is available with up to 4 GB of DDR4-3200 memory.

5.2.2 Non-volatile Storage Memory

The VAR-SOM-AM62 is available with a non-volatile MLC eMMC storage memory with optional densities of up to 128GB. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.

5.3 Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4 Wi-Fi + BT

VAR-SOM-AM62 module can be configured either for Dual band or Single Band Wi-Fi® and Bluetooth® add on modules. Both realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

VAR-SOM-AM62 Wi-Fi and BT Key Features:

- IEEE 802.11 ac/a/b/g/n (Dual Band Option)
- IEEE 802.11 b/g/n (Single Band Option)
- Bluetooth 2.1+EDR, and BLE 5.2
- U.F.L connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- Industrial operating Temperature Range: -40 to +85

5.4.1 VAR-SOM-AM62 Dual Band Option

The VAR-SOM-AM62 contains LSR's certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 5.2 wireless connectivity.

5.4.2 VAR-SOM-AM62 Single Band Option

The VAR-SOM-AM62 contains Laird's certified high-performance Sterling-LWB™ 2.4 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW4343W chipset supporting IEEE 802.11 b/g/n,
BT 2.1+EDR, and BLE 5.1 wireless connectivity.

5.5 PMIC

The VAR-SOM-AM62 features TI's TPS65219 chip as a Power Management Integrated circuit (PMIC) designed specifically for use with TI's AM62x Sitara family of application processors. The TPS65219 regulates power rails required on SOM from a single 3.3V power supply.
The PMIC is programmable via the I2C interface and associated register map.

5.6 10/100/1000 Mbps Ethernet Transceiver

The VAR-SOM-AM62 features on board an Integrated Ethernet Transceiver Analog Devices ADIN1300.

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.
- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover
- Auto-negotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

5.7 Resistive Touch Controller (TSC2046)

The VAR-SOM-AM62 features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

5.8 EEPROM

The SOM uses a serial EEPROM to store memory calibration and manufacturing parameters.
This EEPROM is connected to I2C3 bus and intended only for holding the above information.
The SOM may not boot if the contents of EEPROM device are corrupted.

6. VAR-SOM-AM62 Hardware Configuration

The table below lists the Hardware configurations options orderable for the VAR-SOM-AM62.

Table 1 Hardware Configuration Options

Option	Description
EC	Ethernet PHY assembled on SOM, 2nd Ethernet port always available over RGMII2/RMII2
AC	Audio Codec assembled on SOM
WBD	Dual band Wi-Fi and BT/BLE combo assembled on SOM
WB	Single band Wi-Fi and BT/BLE combo assembled on SOM
TP	Resistive Touch controller assembled on SOM (note: capacitive touch is always available via I2C)
GPMC/ OSPI/ MMC2	OSPI – Extra Octal/Quad SPI signals exported via SOM connector pins GPMC – Parallel bus signals exported via SOM connector pins MMC2 – Additional SD/MMC2 signals exported via SOM connector pins, available only when Wi-Fi/BT chip is not assembled
RG2CM	Switching from the default 3.3V to 1.8V over RGMII2/RMII2, RGMII1/RMII1 signals exported via SOM

Note: Other orderable options are available and are not part of this datasheet.
Please refer to Variscite official website for full list of configuration options.

7. External Connectors

7.1 Board to Board Connector

The VAR-SOM-AM62 exposes a 200-pin SO-DIMM connector.

- The recommended mating connectors for baseboard interfacing are:
  1. Concraft - 0701A0BE52E
  2. Tyco Electronics -1565917-4

7.2 Wi-Fi & BT Connector

In Modules with Wi-Fi “WB” or “WBD” Configuration - a combined Wi-Fi + BT antenna connector is assembled.

- Connector type: U.FL JACK connector
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 JTAG Header

In addition to the 200-pin SO-DIMM interface, the SOM exposes JTAG interface via an optional header.

7.4 VAR-SOM-AM62 Connector Pin-out

Table 2: VAR-SOM-AM62 J1 Pinout

Pin	Assembly	Pin name	Notes	GPIO	Ball
1	no EC	RGMII1_TX_CTL	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	GPIO0_73	AD19
1	EC	NC	With "EC" configuration this pin is Not Connected		NC
2		GND	Digital Ground		GND
3	no EC	RGMII1_TD3	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_78	AD18
3	EC	ETH0_MDI_A_P	Signal source is Ethernet PHY		ADIN1300.12
4	no EC	RGMII1_RD0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_81	AB17
4	EC	ETH0_MDI_C_P	Signal source is Ethernet PHY		ADIN1300.16
5	no EC	RGMII1_TD2	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_77	AE18
5	EC	ETH0_MDI_A_M	Signal source is Ethernet PHY		ADIN1300.13
6	no EC	RGMII1_RD1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_82	AC17
6	EC	ETH0_MDI_C_M	Signal source is Ethernet PHY		ADIN1300.17
7		GND	Digital Ground		GND
8		GND	Digital Ground		GND
9	no EC	RGMII1_TD1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_76	AD20
9	EC	ETH0_MDI_B_P	Signal source is Ethernet PHY		ADIN1300.14
10	no EC	RGMII1_RD2	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_83	AB16
10	EC	ETH0_MDI_D_P	Signal source is Ethernet PHY		ADIN1300.18
11	no EC	RGMII1_TD0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_75	AE20
11	EC	ETH0_MDI_B_M	Signal source is Ethernet PHY		ADIN1300.15
12	no EC	RGMII1_RD3	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_84	AA15
12	EC	ETH0_MDI_D_M	Signal source is Ethernet PHY		ADIN1300.19
13		GND	Digital Ground		GND
14		GND	Digital Ground		GND
15	no EC	RGMII1_RX_CTL	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_79	AE17
15	EC	ETH0_LED_ACT	Signal source is Ethernet PHY		ADIN1300.21

Pin	Assembly	Pin name	Notes	GPIO	Ball
16	no EC	RGMII1_RXC	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_80	AD17
16	EC	ETH0_LED_LINK_10_100_1000	Signal source is Ethernet PHY		ADIN1300.26 via inv. FET
17		MCASP0_AXR1		GPIO1_9	B18
18	no AC & no GPMC	GPMC0_WEN	Available in SOM without "AC" and without "GPMC" configuration	GPIO0_34	L25
18	AC	DMIC_CLK	Signal source is Audio Codec		WM8904.1
19		GND	Digital Ground		GND
20	no AC & no GPMC	GPMC0_WPN	Available in SOM without "AC" and without "GPMC" configuration	GPIO0_39	K25
20	AC	DMIC_DATA	Signal source is Audio Codec		WM8904.27
21		GPMC0_AD10	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_25	T25
22		GPMC0_AD15	BOOTMODE15 pin, 100K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_30	U24
23		GPMC0_AD14	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_29	U25
24		GPMC0_AD12	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_27	T22
25		GPMC0_AD13	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_28	T24
26		GPMC0_AD11	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_26	R21
27		GND	Digital Ground		GND
28		GND	Digital Ground		GND
29		EXT_REFCLK1		GPIO1_30	A18
30		MDIO0_MDIO	Pin is referenced to 3.3V, and has an internal 1.47K Pull Up. In "RG2CM" configuration pin is routed via on SOM 1.8<->3.3V voltage translator. Do not alter pinmux with "EC" configuration	GPIO0_85	AB22
31	no GPMC & no OSPI & no MMC2	NC			NC
31	GPMC	GPMC0_AD0	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_15	M25
31	OSPI	OSPI0_CLK	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_0	H24
31	MMC2 & no (WB or WBD)	MMC2_DAT3	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_65	D24
32		VCC_SOM	SOM Power		VCC_SOM
33	no GPMC & no OSPI & no MMC2	NC			NC
33	GPMC	GPMC0_AD1	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_16	N23
33	OSPI	OSPI_LBCLKO	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_1	G25
33	MMC2 & no (WB or WBD)	MMC2_DAT2	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_66	E23

Pin	Assembly	Pin name	Notes	GPIO	Ball
34		VCC_SOM	SOM Power		VCC_SOM
35	no GPMC & no OSPI & no MMC2	NC			NC
35	GPMC	GPMC0_DIR	Available in SOM with "GPMC" configuration;	GPIO0_40	M22
35	OSPI	OSPI0_D1	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_4	G24
35	MMC2 & no (WB or WBD)	MMC2_DAT1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_67	C25
36	no GPMC & no OSPI & no MMC2	VCC_SOM	SOM Power		VCC_SOM
36	GPMC	GPMC0_OEN_REN	Available in SOM with "GPMC" configuration;	GPIO0_33	L24
36	OSPI	OSPI0_DQS	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_2	J24
36	MMC2 & no (WB or WBD)	VDDSHV6	MMC2 pins group power IN		J18
37		GND	Digital Ground		GND
38		NC			NC
39		MCASP0_AFSR		GPIO1_13	E19
40		GPMC0_AD7	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_22	R23
41		MCASP0_AXR2		GPIO1_8	A19
42		BOOT_SEL	Controls internal OR external boot source; Internal signal pulled up to SOM_PGOOD using 1K resistor;		BOOT_SEL
43		MCASP0_ACLKR		GPIO1_14	A20
44		MCAN0_TX		GPIO1_24	C15
45		MCASP0_AXR3		GPIO1_7	B19
46		MCAN0_RX		GPIO1_25	E15
47	no GPMC & no OSPI & no MMC2	GND	Digital Ground		GND
47	GPMC	GPMC0_BE1N	Available in SOM with "GPMC" configuration;	GPIO0_36	N20
47	OSPI	OSPI0_CSN3	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_14	E24
47	MMC2 & no (WB or WBD)	MMC2_SDCD	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_71	A23
48		GPMC0_AD5	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_20	P22
49		SOM_PGOOD	SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw allowed.		SOM_PGOOD
50		VOUT0_DATA12	Used internally with "WBD", Function can be released if BT Function disabled (In initial SOM Rev 1.0 exported on pin 51)	GPIO0_58	AB25
51		VOUT0_DATA13	Used internally with "WBD", Function can be released if BT Function disabled (In initial SOM Rev 1.0 exported on pin 50)	GPIO0_57	AA24

Pin	Assembly	Pin name	Notes	GPIO	Ball
52		VOUT0_DATA7	Used internally with "WBD", Function can be released if BT Function disabled	GPIO0_52	AA25
53		VOUT0_DATA6	Used internally with "WBD", Function can be released if BT Function disabled	GPIO0_51	Y23
54		RGMII2_RD3	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	GPIO1_6	AE22
55		RGMII2_TD3	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	GPIO1_0	AC20
56		RGMII2_TD2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	GPIO0_91	AD21
57		RGMII2_RXC	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	GPIO1_2	AD23
58		MCU_UART0_CTSN		MCU_GPIO0_7	A6
59	no GPMC & no OSPI & no MMC2	GND	Digital Ground		GND
59	GPMC	GPMC0_CLK	Available in SOM with "GPMC” configuration;	GPIO0_31	P25
59	OSPI	OSPI0_D3	Available in SOM with "OSPI” configuration; Pin referenced to 1.8V	GPIO0_6	F24
59	MMC2 & no (WB or WBD)	MMC2_SDWP	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_72	B23
60		MMC1_CLK	Bank voltage set on SOM 1.8V/3.3V	GPIO1_46	B22
61		MMC1_DAT2	Bank voltage set on SOM 1.8V/3.3V	GPIO1_43	C21
62		MMC1_DAT0	Bank voltage set on SOM 1.8V/3.3V	GPIO1_45	A22
63		MMC1_DAT1	Bank voltage set on SOM 1.8V/3.3V	GPIO1_44	B21
64		MMC1_CMD	Bank voltage set on SOM 1.8V/3.3V	GPIO1_47	A21
65		MMC1_DAT3	Bank voltage set on SOM 1.8V/3.3V	GPIO1_42	D22
66		GND	Digital Ground		GND
67		GND	Digital Ground		GND
68		SPI0_CS1		GPIO1_16	C13
69		MCASP0_AXR0		GPIO1_10	E18
70		OSPI0_D6	Pin referenced to 1.8V in SOM with "OSPI” configuration;	GPIO0_9	H25
71		RGMII2_RD2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	GPIO1_5	AC21
72		MCASP0_AFSX		GPIO1_12	D20
73		RGMII2_TD0	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	GPIO0_89	Y18
74		MDIO0_MDC	Pin is referenced to 3.3V. In "RG2CM" configuration pin is routed via on SOM 1.8<->3.3V voltage translator. Do not alter pinmux with "EC" configuration	GPIO0_86	AD24
75		OSPI0_D5	Pin referenced to 1.8V in SOM with "OSPI” configuration;	GPIO0_8	J25
76	no GPMC & no OSPI & no MMC2	GND	Digital Ground		GND
76	GPMC	GPMC0_AD2	Available in SOM with "GPMC” configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_17	N24
76	OSPI	OSPI0_D0	Available in SOM with "OSPI” configuration; Pin referenced to 1.8V	GPIO0_3	E25

Pin	Assembly	Pin name	Notes	GPIO	Ball
76	MMC2 & no (WB or WBD)	MMC2_CLK	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_69	D25
77		OSPI0_D7	Pin referenced to 1.8V in SOM with "OSPI" configuration;	GPIO0_10	J22
78		GND	Digital Ground		GND
79		OSPI0_D4	Pin referenced to 1.8V in SOM with "OSPI" configuration;	GPIO0_7	J23
80		MMC1_SDCD	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	GPIO1_48	D17
81		RGMII2_RD1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO1_4	AB20
82		USB1_DRVVBUS		GPIO1_51	F18
83		UART0_RXD	Used as debug UART on Variscite base board	GPIO1_20	D14
84		GPMC0_AD4	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_19	P24
85		UART0_TXD	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	GPIO1_21	E14
86		GPMC0_AD6	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_21	P21
87		I2C0_SDA		GPIO1_27	A16
88		I2C0_SCL		GPIO1_26	B16
89		GND	Digital Ground		GND
90		I2C1_SDA		GPIO1_29	A17
91		MCU_UART0_RXD		MCU_GPIO0_5	B5
92		I2C1_SCL		GPIO1_28	B17
93		MCU_UART0_RTSN		MCU_GPIO0_8	B6
94		USB0_DRVVBUS		GPIO1_50	C20
95		GND	Digital Ground		GND
96		RGMII2_TXC	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_88	AE21
97	no EC	RGMII1_TXC	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_74	AE19
97	EC	NC	With "EC" configuration this pin is Not Connected		NC
98		SYS_NRSTIN_3V3			D2 (via diode)
99		MCU_UART0_TXD		MCU_GPIO0_6	A5
100	no GPMC & no OSPI & no MMC2	NC			NC
100	GPMC	GPMC0_CSN0	Available in SOM with "GPMC" configuration;	GPIO0_41	M21
100	OSPI	OSPI0_D2	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_5	F25
100	MMC2 & no (WB or WBD)	MMC2_CMD	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_70	C24
101		GND	Digital Ground		GND
102	no GPMC & no OSPI & no MMC2	NC			NC

Pin	Assembly	Pin name	Notes	GPIO	Ball
102	GPMC	GPMC0_CSN1	Available in SOM with "GPMC" configuration;	GPIO0_42	L21
102	OSPI	OSPI0_CSN0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_11	F23
102	MMC2 & no (WB or WBD)	MMC2_DAT0	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_68	B24
103		VCC_SOM	SOM Power		VCC_SOM
104		USB1_VBUS			AB10
105		VCC_SOM	SOM Power		VCC_SOM
106		USB0_VBUS			AC11
107		VCC_SOM	SOM Power		VCC_SOM
108		USB1_DM			AD10
109		VCC_SOM	SOM Power		VCC_SOM
110		USB1_DP			AE9
111		VCC_SOM	SOM Power		VCC_SOM
112		GND	Digital Ground		GND
113		RGMII2_TX_CTL	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_87	AA19
114		USB0_DM			AE11
115		GPMC0_AD8	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_23	R24
116		USB0_DP			AD11
117		MCASP0_ACLKX		GPIO1_11	B20
118		GND	Digital Ground		GND
119		CSI0_RXP0			AC15
120		RGMII2_RX_CTL	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO1_1	AD22
121		CSI0_RXN0			AB14
122		RGMII2_RD0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO1_3	AE23
123		CSI0_RXN1			AD14
124		MMC1_SDWP		GPIO1_49	C17
125		CSI0_RXP1			AE14
126		GND	Digital Ground		GND
127		CSI0_RXP2			AE13
128		MCU_RESETSTATZ		MCU_GPIO0_21	B12
129		CSI0_RXN2			AD13
130		MCU_RESETZ	Internal signal pulled up to SOM_PGOOD using 10K resistor.		E11
131		CSI0_RXN3			AB12
132		GND	Digital Ground		GND
133		CSI0_RXP3			AC13
134		RESET_REQZ	Internal signal pulled up to SOM_PGOOD using 10K resistor.		F20
135		CSI0_RXCLKP			AE15
136		MCU_ERRORN	Pin is referenced to 1.8V. Internal signal pulled down to GND using 10K resistor.		D1

Pin	Assembly	Pin name	Notes	GPIO	Ball
137		CSI0_RXCLKN			AD15
138		GND	Digital Ground		GND
139		GND	Digital Ground		GND
140		WKUP_I2C0_SCL	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	MCU_GPIO0_19	B9
141		WKUP_I2C0_SDA	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	MCU_GPIO0_20	A9
142		WKUP_UART0_CTSN		MCU_GPIO0_11	C6
143		WKUP_UART0_RTSN		MCU_GPIO0_12	A4
144		GND	Digital Ground		GND
145		WKUP_UART0_RXD		MCU_GPIO0_9	B4
146		MCU_I2C0_SCL	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	MCU_GPIO0_17	A8
147		WKUP_UART0_TXD		MCU_GPIO0_10	C5
148		MCU_I2C0_SDA	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	MCU_GPIO0_18	D10
149		GND	Digital Ground		GND
150		MCU_SPI0_CLK		MCU_GPIO0_2	A7
151		MCU_SPI0_D0		MCU_GPIO0_3	D9
152		MCU_SPI0_D1		MCU_GPIO0_4	C9
153		MCU_SPI0_CS1		MCU_GPIO0_1	B8
154		MCU_MCAN1_RX		MCU_GPIO0_16	D4
155		MCU_MCAN0_RX		MCU_GPIO0_14	B3
156		MCU_MCAN1_TX		MCU_GPIO0_15	E5
157		MCU_MCAN0_TX		MCU_GPIO0_13	D6
158		GND	Digital Ground		GND
159		GND	Digital Ground		GND
160		OLDI0_A1N			AD3
161		OLDI0_A0N			AA5
162		OLDI0_A1P			AB4
163		OLDI0_A0P			Y6
164		OLDI0_A2N			Y8
165		OLDI0_A3N			AB6
166		OLDI0_A2P			AA8
167		OLDI0_A3P			AA7
168		OLDI0_CLK0N			AD4
169		GND	Digital Ground		GND
170		OLDI0_CLK0P			AE3
171		GPMC0_AD9	BOOTMODE09 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_24	R25
172		GND	Digital Ground		GND
173		GPMC0_AD3	BOOTMODE03 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_18	N25
174		GPMC0_CSN2	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	GPIO0_43	K22

Pin	Assembly	Pin name	Notes	GPIO	Ball
175		GPMC0_WAIT1		GPIO0_38	V25
176		GPMC0_CSN3	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	GPIO0_44	K24
177		RGMII2_TD1	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	GPIO0_90	AA18
178		GND	Digital Ground		GND
179		GND	Digital Ground		GND
180		OLDI0_CLK1N			AE4
181		OLDI0_A7P			AE7
182		OLDI0_CLK1P			AD5
183		OLDI0_A7N			AD8
184		OLDI0_A4N			AC6
185		GND	Digital Ground		GND
186		OLDI0_A4P			AC5
187	no TP	SPI0_D0	Available in SOM without TP	GPIO1_18	B13
187	TP	TS_X-	Signal source is Resistive Touch controller		TSC2046.8
188		OLDI0_A5N			AE5
189	no TP	SPI0_CLK	Available in SOM without TP	GPIO1_17	A14
189	TP	TS_X+	Signal source is Resistive Touch controller		TSC2046.6
190		OLDI0_A5P			AD6
191	no TP	SPI0_CS0	Available in SOM without TP	GPIO1_15	A13
191	TP	TS_Y+	Signal source is Resistive Touch controller		TSC2046.7
192		OLDI0_A6N			AE6
193	no TP	SPI0_D1	Available in SOM without TP	GPIO1_19	B14
193	TP	TS_Y-	Signal source is Resistive Touch controller		TSC2046.9
194		OLDI0_A6P			AD7
195	AC	AGND	Audio Ground		AGND
196	no AC & no GPMC	NC			NC
196	no AC & GPMC	GPMC0_WEN	Available in SOM without "AC” and with "GPMC" configuration	GPIO0_34	L25
196	AC	HPOUTFB	Signal source is Audio Codec		WM8904.14
197	no AC & no GPMC	NC			NC
197	no AC & GPMC	GPMC0_WPN	Available in SOM without "AC” and with "GPMC" configuration	GPIO0_39	K25
197	AC	LINEIN1_LP	Signal source is Audio Codec		WM8904.26
198	no AC	GPMC0_ADVN_ALE	Available in SOM without "AC” configuration	GPIO0_32	L23
198	AC	HPLOUT	Signal source is Audio Codec		WM8904.13
199	no AC	GPMC0_WAIT0	Available in SOM without "AC” configuration	GPIO0_37	U23
199	AC	LINEIN1_RP	Signal source is Audio Codec		WM8904.24
200	no AC	GPMC0_BE0N_CLE	Available in SOM without "AC” configuration	GPIO0_35	M24
200	AC	HPROUT	Signal source is Audio Codec		WM8904.15

7.5 VAR-SOM-AM62 Connector Pin Mux

Table 3: VAR-SOM-AM62 PINMUX

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
1	no EC	AD19	RGMII1_TX_CTL	RMII1_TX_EN						GPIO0_73			
3	no EC	AD18	RGMII1_TD3		PR0_UART0_TXD					GPIO0_78			
4	no EC	AB17	RGMII1_RD0	RMII1_RXD0						GPIO0_81			
5	no EC	AE18	RGMII1_TD2		PR0_UART0_RXD					GPIO0_77			
6	no EC	AC17	RGMII1_RD1	RMII1_RXD1						GPIO0_82			
9	no EC	AD20	RGMII1_TD1	RMII1_TXD1						GPIO0_76			
10	no EC	AB16	RGMII1_RD2		PR0_UART0_RTSn					GPIO0_83			
11	no EC	AE20	RGMII1_TD0	RMII1_TXD0						GPIO0_75			
12	no EC	AA15	RGMII1_RD3							GPIO0_84			
15	no EC	AE17	RGMII1_RX_CTL	RMII1_RX_ER						GPIO0_79			
16	no EC	AD17	RGMII1_RXC	RMII1_REF_CLK	PR0_UART0_CTSn					GPIO0_80			
17		B18	MCASP0_AXR1	SPI2_CS2	ECAP1_IN_APWM_OUT			PR0_UART0_RXD	EHRPWM1_A	GPIO1_9	EQEP0_S		
18	no AC & no GPMC	L25	GPMC0_WEn		MCASP1_AXR0		PR0_PRU0_GPO11	PR0_PRU0_GPI11	TRC_DATA9	GPIO0_34			
20	no AC & no GPMC	K25	GPMC0_WPn	AUDIO_EXT_REFCLK1	GPMC0_A22	UART6_TXD	PR0_PRU0_GPO15	PR0_PRU0_GPI15	TRC_DATA13	GPIO0_39			
21		T25	GPMC0_AD10	VOUT0_DATA18	UART3_RXD	MCASP2_AXR2	PR0_PRU1_GPO2	PR0_PRU1_GPI2		GPIO0_25	OBSCLK0		BOOTMODE10
22		U24	GPMC0_AD15	VOUT0_DATA23	UART5_TXD	MCASP2_ACLKR	PR0_PRU0_GPO3	PR0_PRU0_GPI3	TRC_DATA19	GPIO0_30	UART2_RTSn		BOOTMODE15
23		U25	GPMC0_AD14	VOUT0_DATA22	UART5_RXD	MCASP2_AFSR	PR0_PRU0_GPO2	PR0_PRU0_GPI2	TRC_DATA20	GPIO0_29	UART2_CTSn		BOOTMODE14
24		T22	GPMC0_AD12	VOUT0_DATA20	UART4_RXD	MCASP2_AFSX	PR0_PRU0_GPO0	PR0_PRU0_GPI0	TRC_DATA22	GPIO0_27			BOOTMODE12
25		T24	GPMC0_AD13	VOUT0_DATA21	UART4_TXD	MCASP2_ACLKX	PR0_PRU0_GPO1	PR0_PRU0_GPI1	TRC_DATA21	GPIO0_28			BOOTMODE13
26		R21	GPMC0_AD11	VOUT0_DATA19	UART3_TXD	MCASP2_AXR3	PR0_PRU1_GPO3	PR0_PRU1_GPI3	TRC_DATA23	GPIO0_26			BOOTMODE11
29		A18	EXT_REFCLK1	SYNC1_OUT	SPI2_CS3	SYSCLKOUT0	TIMER_IO4	CLKOUT0	CP_GEMAC_CPTS0_RFT_CLK	GPIO1_30	ECAP0_IN_APWM_OUT		
30		AB22	MDIO0_MDIO							GPIO0_85			
31	GPMC	M25	GPMC0_AD0	PR0_PRU1_GPO8	PR0_PRU1_GPI8	MCASP2_AXR4	PR0_PRU0_GPO0	PR0_PRU0_GPI0	TRC_CLK	GPIO0_15			BOOTMODE00
31	OSPI	H24	OSPI0_CLK							GPIO0_0			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
31	MMC2 & no (WB or WBD)	D24	MMC2_DAT3	MCASP1_AXR3		UART5_RXD				GPIO0_65			
33	GPMC	N23	GPMC0_AD1	PR0_PRU1_GPO9	PR0_PRU1_GPI9	MCASP2_AXR5	PR0_PRU0_GPO1	PR0_PRU0_GPI1	TRC_CTL	GPIO0_16			BOOTMODE01
33	OSPI	G25	OSPI0_LBCLKO					UART5_RTSn		GPIO0_1			
33	MMC2 & no (WB or WBD)	E23	MMC2_DAT2	MCASP1_AXR2		UART5_TXD				GPIO0_66			
35	GPMC	M22	GPMC0_DIR	PR0_ECAP0_IN_APWM_OUT		MCASP2_AXR13	PR0_PRU0_GPO16	PR0_PRU0_GPI16	TRC_DATA14	GPIO0_40	EQEP2_S		
35	OSPI	G24	OSPI0_D1							GPIO0_4			
35	MMC2 & no (WB or WBD)	C25	MMC2_DAT1	MCASP1_AXR1						GPIO0_67			
36	GPMC	L24	GPMC0_OEn_REn		MCASP1_AXR1		PR0_PRU0_GPO10	PR0_PRU0_GPI10	TRC_DATA8	GPIO0_33			
36	OSPI	J24	OSPI0_DQS					UART5_CTSn		GPIO0_2			
39		E19	MCASP0_AFSR	SPI2_CS0	UART1_RXD				EHRPWM0_A	GPIO1_13	EQEP1_S		
40		R23	GPMC0_AD7	PR0_PRU1_GPO15	PR0_PRU1_GPI15	MCASP2_AXR11	PR0_PRU0_GPO7	PR0_PRU0_GPI7	TRC_DATA5	GPIO0_22			BOOTMODE07
41		A19	MCASP0_AXR2	SPI2_D1	UART1_RTSn	UART6_TXD	PR0_IEP0_EDIO_DATA_IN_OUT29	ECAP2_IN_APWM_OUT	PR0_UART0_TXD	GPIO1_8	EQEP0_B		
43		A20	MCASP0_ACLKR	SPI2_CLK	UART1_TXD				EHRPWM0_B	GPIO1_14	EQEP1_I		
44		C15	MCAN0_TX	UART5_RXD	TIMER_IO2	SYNC2_OUT	UART1_DTRn	EQEP2_I	PR0_UART0_RXD	GPIO1_24	MCASP2_AXR0	EHRPWM_TZn_IN3	
45		B19	MCASP0_AXR3	SPI2_D0	UART1_CTSn	UART6_RXD	PR0_IEP0_EDIO_DATA_IN_OUT28	ECAP1_IN_APWM_OUT	PR0_UART0_RXD	GPIO1_7	EQEP0_A		
46		E15	MCAN0_RX	UART5_TXD	TIMER_IO3	SYNC3_OUT	UART1_RIn	EQEP2_S	PR0_UART0_TXD	GPIO1_25	MCASP2_AXR1	EHRPWM_TZn_IN4	
47	GPMC	N20	GPMC0_BE1n			MCASP2_AXR12	PR0_PRU0_GPO13	PR0_PRU0_GPI13	TRC_DATA11	GPIO0_36			
47	OSPI	E24	OSPI0_CSn3	OSPI0_RESET_OUT0	OSPI0_ECC_FAIL	MCASP1_ACLKR	MCASP1_AXR3	UART5_TXD		GPIO0_14			
47	MMC2 & no (WB or WBD)	A23	MMC2_SDCD	MCASP1_ACLKX		UART4_RXD				GPIO0_71			
48		P22	GPMC0_AD5	PR0_PRU1_GPO13	PR0_PRU1_GPI13	MCASP2_AXR9	PR0_PRU0_GPO5	PR0_PRU0_GPI5	TRC_DATA3	GPIO0_20			BOOTMODE05
50		AB25	VOUT0_DATA12	GPMC0_A12	PR0_PRU1_GPO11	PR0_PRU1_GPI11	UART5_RTSn	PR0_PRU0_GPO2	PR0_PRU0_GPI2	GPIO0_57			
51		AA24	VOUT0_DATA13	GPMC0_A13	PR0_PRU1_GPO12	PR0_PRU1_GPI12	UART5_CTSn	PR0_PRU0_GPO3	PR0_PRU0_GPI3	GPIO0_58			
52		AA25	VOUT0_DATA7	GPMC0_A7	PR0_PRU1_GPO7	PR0_PRU1_GPI7	UART5_TXD	PR0_PRU0_GPO15	PR0_PRU0_GPI15	GPIO0_52			
53		Y23	VOUT0_DATA6	GPMC0_A6	PR0_PRU1_GPO6	PR0_PRU1_GPI6	UART5_RXD	PR0_PRU0_GPO14	PR0_PRU0_GPI14	GPIO0_51			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
54		AE22	RGMII2_RD3		AUDIO_EXT_REFCLK0	PR0_PRU0_GPO16	PR0_PRU0_GPI16	PR0_UART0_TXD		GPIO1_6	EQEP2_B		
55		AC20	RGMII2_TD3		MCASP2_ACLKX	PR0_PRU1_GPO16	PR0_PRU1_GPI16	PR0_ECAP0_SYNC_OUT	PR0_UART0_CTSn	GPIO1_0	EQEP2_S		
56		AD21	RGMII2_TD2		MCASP2_AFSX	PR0_PRU1_GPO4	PR0_PRU1_GPI4	PR0_ECAP0_IN_APWM_OUT		GPIO0_91	EQEP2_I		
57		AD23	RGMII2_RXC	RMII2_REF_CLK	MCASP2_AXR1	PR0_PRU0_GPO1	PR0_PRU0_GPI1	PR0_ECAP0_SYNC_IN		GPIO1_2			
58		A6	MCU_UART0_CTSn	MCU_TIMER_IO0		MCU_SPI1_D0				MCU_GPIO0_7			
59	GPMC	P25	GPMC0_CLK		MCASP1_AXR3	GPMC0_FCLK_MUX	PR0_PRU0_GPO8	PR0_PRU0_GPI8	TRC_DATA6	GPIO0_31			
59	OSPI	F24	OSPI0_D3							GPIO0_6			
59	MMC2 & no (WB or WBD)	B23	MMC2_SDWP	MCASP1_AFSX		UART4_TXD				GPIO0_72			
60		B22	MMC1_CLK		TIMER_IO4	UART3_RXD				GPIO1_46			
61		C21	MMC1_DAT2	CP_GEMAC_CPTS0_TS_SYNC	TIMER_IO1	UART2_TXD				GPIO1_43			
62		A22	MMC1_DAT0	CP_GEMAC_CPTS0_HW2TSPUSH	TIMER_IO3	UART2_CTSn	ECAP2_IN_APWM_OUT			GPIO1_45			
63		B21	MMC1_DAT1	CP_GEMAC_CPTS0_HW1TSPUSH	TIMER_IO2	UART2_RTSn	ECAP1_IN_APWM_OUT			GPIO1_44			
64		A21	MMC1_CMD		TIMER_IO5	UART3_TXD				GPIO1_47			
65		D22	MMC1_DAT3	CP_GEMAC_CPTS0_TS_COMP	TIMER_IO0	UART2_RXD				GPIO1_42			
68		C13	SPI0_CS1	CP_GEMAC_CPTS0_TS_COMP	EHRPWM0_B	ECAP0_IN_APWM_OUT				GPIO1_16		EHRPWM_TZn_IN5	
69		E18	MCASP0_AXR0	PR0_ECAP0_IN_APWM_OUT	AUDIO_EXT_REFCLK0			PR0_UART0_TXD	EHRPWM1_B	GPIO1_10	EQEP0_I		
70		H25	OSPI0_D6	SPI1_D0	MCASP1_ACLKX	UART6_RTSn				GPIO0_9			
71		AC21	RGMII2_RD2		MCASP2_AXR0	PR0_PRU0_GPO4	PR0_PRU0_GPI4	PR0_UART0_RXD		GPIO1_5	EQEP2_A		
72		D20	MCASP0_AFSX	SPI2_CS3	AUDIO_EXT_REFCLK1					GPIO1_12	EQEP1_B		
73		Y18	RGMII2_TD0	RMII2_TXD0	MCASP2_AXR6	PR0_PRU1_GPO2	PR0_PRU1_GPI2			GPIO0_89			
74		AD24	MDIO0_MDC							GPIO0_86			
75		J25	OSPI0_D5	SPI1_CLK	MCASP1_AXR0	UART6_TXD				GPIO0_8			
76	GPMC	N24	GPMC0_AD2	PR0_PRU1_GPO10	PR0_PRU1_GPI10	MCASP2_AXR6	PR0_PRU0_GPO2	PR0_PRU0_GPI2	TRC_DATA0	GPIO0_17			BOOTMODE02
76	OSPI	E25	OSPI0_D0							GPIO0_3			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
76	MMC2 & no (WB or WBD)	D25	MMC2_CLK	MCASP1_ACLKR	MCASP1_AXR5	UART6_RXD				GPIO0_69			
77		J22	OSPI0_D7	SPI1_D1	MCASP1_AFSX	UART6_CTSn				GPIO0_10			
79		J23	OSPI0_D4	SPI1_CS0	MCASP1_AXR1	UART6_RXD				GPIO0_7			
80		D17	MMC1_SDCD	UART6_RXD	TIMER_IO6	UART3_RTSn				GPIO1_48			
81		AB20	RGMII2_RD1	RMII2_RXD1	MCASP2_AFSR	PR0_PRU0_GPO3	PR0_PRU0_GPI3	MCASP2_AXR7		GPIO1_4			
82		F18	USB1_DRVVBUS							GPIO1_51			
83		D14	UART0_RXD	ECAP1_IN_APWM_OUT	SPI2_D0	EHRPWM2_A				GPIO1_20			
84		P24	GPMC0_AD4	PR0_PRU1_GPO12	PR0_PRU1_GPI12	MCASP2_AXR8	PR0_PRU0_GPO4	PR0_PRU0_GPI4	TRC_DATA2	GPIO0_19			BOOTMODE04
85		E14	UART0_TXD	ECAP2_IN_APWM_OUT	SPI2_D1	EHRPWM2_B				GPIO1_21			
86		P21	GPMC0_AD6	PR0_PRU1_GPO14	PR0_PRU1_GPI14	MCASP2_AXR10	PR0_PRU0_GPO6	PR0_PRU0_GPI6	TRC_DATA4	GPIO0_21			BOOTMODE06
87		A16	I2C0_SDA	PR0_IEP0_EDIO_DATA_IN_OUT31	SPI2_CS2	TIMER_IO5	UART1_DSRn	EQEP2_B	EHRPWM_SOCB	GPIO1_27	ECAP2_IN_APWM_OUT		
88		B16	I2C0_SCL	PR0_IEP0_EDIO_DATA_IN_OUT30	SYNC0_OUT	OBSCLK0	UART1_DCDn	EQEP2_A	EHRPWM_SOCA	GPIO1_26	ECAP1_IN_APWM_OUT	SPI2_CS0	
90		A17	I2C1_SDA	UART1_TXD	TIMER_IO1	SPI2_CLK	EHRPWM0_SYNCO			GPIO1_29	EHRPWM2_B	MMC2_SDWP	
91		B5	MCU_UART0_RXD							MCU_GPIO0_5			
92		B17	I2C1_SCL	UART1_RXD	TIMER_IO0	SPI2_CS1	EHRPWM0_SYNCI			GPIO1_28	EHRPWM2_A	MMC2_SDCD	
93		B6	MCU_UART0_RTSn	MCU_TIMER_IO1		MCU_SPI1_D1				MCU_GPIO0_8			
94		C20	USB0_DRVVBUS							GPIO1_50			
96		AE21	RGMII2_TXC	RMII2_CRS_DV	MCASP2_AXR5	PR0_PRU1_GPO1	PR0_PRU1_GPI1			GPIO0_88			
97	no EC	AE19	RGMII1_TXC	RMII1_CRS_DV						GPIO0_74			
98		D2 (via diode)	MCU_PORz										
99		A5	MCU_UART0_TXD							MCU_GPIO0_6			
100	GPMC	M21	GPMC0_CSn0			MCASP2_AXR14	PR0_PRU0_GPO17	PR0_PRU0_GPI17	TRC_DATA15	GPIO0_41			
100	OSPI	F25	OSPI0_D2							GPIO0_5			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
100	MMC2 & no (WB or WBD)	C24	MMC2_CMD	MCASP1_AFSR	MCASP1_AXR4	UART6_TXD				GPIO0_70			
102	GPMC	L21	GPMC0_CSn1	PR0_PRU1_GPO16	PR0_PRU1_GPI16	MCASP2_AXR15	PR0_PRU0_GPO18	PR0_PRU0_GPI18	TRC_DATA16	GPIO0_42			
102	OSPI	F23	OSPI0_CSn0							GPIO0_11			
102	MMC2 & no (WB or WBD)	B24	MMC2_DAT0	MCASP1_AXR0						GPIO0_68			
113		AA19	RGMII2_TX_CTL	RMII2_TX_EN	MCASP2_AXR4	PR0_PRU1_GPO0	PR0_PRU1_GPI0			GPIO0_87			
115		R24	GPMC0_AD8	VOUT0_DATA16	UART2_RXD	MCASP2_AXR0	PR0_PRU1_GPO0	PR0_PRU1_GPI0		GPIO0_23			BOOTMODE08
117		B20	MCASP0_ACLKX	SPI2_CS1	ECAP2_IN_APWM_OUT					GPIO1_11	EQEP1_A		
120		AD22	RGMII2_RX_CTL	RMII2_RX_ER	MCASP2_AXR3	PR0_PRU0_GPO0	PR0_PRU0_GPI0			GPIO1_1			
122		AE23	RGMII2_RD0	RMII2_RXD0	MCASP2_AXR2	PR0_PRU0_GPO2	PR0_PRU0_GPI2		PR0_UART0_RTSn	GPIO1_3			
124		C17	MMC1_SDWP	UART6_TXD	TIMER_IO7	UART3_CTSn				GPIO1_49			
128		B12	MCU_RESETSTATz							MCU_GPIO0_21			
130		E11	MCU_RESETz										
134		F20	RESET_REQz										
136		D1	MCU_ERRORn										
140		B9	WKUP_I2C0_SCL							MCU_GPIO0_19			
141		A9	WKUP_I2C0_SDA							MCU_GPIO0_20			
142		C6	WKUP_UART0_CTSn	WKUP_TIMER_IO0		MCU_SPI1_CS0				MCU_GPIO0_11			
143		A4	WKUP_UART0_RTSn	WKUP_TIMER_IO1		MCU_SPI1_CLK				MCU_GPIO0_12			
145		B4	WKUP_UART0_RXD		MCU_SPI0_CS2					MCU_GPIO0_9			
146		A8	MCU_I2C0_SCL							MCU_GPIO0_17			
147		C5	WKUP_UART0_TXD		MCU_SPI1_CS2					MCU_GPIO0_10			
148		D10	MCU_I2C0_SDA							MCU_GPIO0_18			
150		A7	MCU_SPI0_CLK							MCU_GPIO0_2			
151		D9	MCU_SPI0_D0							MCU_GPIO0_3			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
152		C9	MCU_SPI0_D1							MCU_GPIO0_4			
153		B8	MCU_SPI0_CS1	MCU_OBSCLK0	MCU_SYSCLKOUT0	MCU_EXT_REFCLK0	MCU_TIMER_IO1			MCU_GPIO0_1			
154		D4	MCU_MCAN1_RX	MCU_TIMER_IO3	MCU_SPI0_CS2	MCU_SPI1_CS2	MCU_SPI1_CLK			MCU_GPIO0_16			
155		B3	MCU_MCAN0_RX	MCU_TIMER_IO0	MCU_SPI1_CS3					MCU_GPIO0_14			
156		E5	MCU_MCAN1_TX	MCU_TIMER_IO2		MCU_SPI1_CS1	MCU_EXT_REFCLK0			MCU_GPIO0_15			
157		D6	MCU_MCAN0_TX	WKUP_TIMER_IO0	MCU_SPI0_CS3					MCU_GPIO0_13			
171		R25	GPMC0_AD9	VOUT0_DATA17	UART2_TXD	MCASP2_AXR1	PR0_PRU1_GPO1	PR0_PRU1_GPI1		GPIO0_24			BOOTMODE09
173		N25	GPMC0_AD3	PR0_PRU1_GPO11	PR0_PRU1_GPI11	MCASP2_AXR7	PR0_PRU0_GPO3	PR0_PRU0_GPI3	TRC_DATA1	GPIO0_18			BOOTMODE03
174		K22	GPMC0_CSn2	I2C2_SCL	MCASP1_AXR4	UART4_RXD	PR0_PRU0_GPO19	PR0_PRU0_GPI19	TRC_DATA17	GPIO0_43	MCASP1_AFSR		
175		V25	GPMC0_WAIT1	VOUT0_EXTPCLKIN	GPMC0_A21	UART6_RXD				GPIO0_38	EQEP2_I		
176		K24	GPMC0_CSn3	I2C2_SDA	GPMC0_A20	UART4_TXD	MCASP1_AXR5		TRC_DATA18	GPIO0_44	MCASP1_ACLKR		
177		AA18	RGMII2_TD1	RMII2_TXD1	MCASP2_ACLKR	PR0_PRU1_GPO3	PR0_PRU1_GPI3	MCASP2_AXR8		GPIO0_90			
187	no TP	B13	SPI0_D0	CP_GEMAC_CPTS0_HW1TSPUSH	EHRPWM1_B					GPIO1_18			
189	no TP	A14	SPI0_CLK	CP_GEMAC_CPTS0_TS_SYNC	EHRPWM1_A					GPIO1_17			
191	no TP	A13	SPI0_CS0		EHRPWM0_A				PR0_ECAP0_SYNC_IN	GPIO1_15			
193	no TP	B14	SPI0_D1	CP_GEMAC_CPTS0_HW2TSPUSH	EHRPWM_TZn_IN0					GPIO1_19			
196	no AC & GPMC	L25	GPMC0_WEn		MCASP1_AXR0		PR0_PRU0_GPO11	PR0_PRU0_GPI11	TRC_DATA9	GPIO0_34			
197	no AC & GPMC	K25	GPMC0_WPn	AUDIO_EXT_REFCLK1	GPMC0_A22	UART6_TXD	PR0_PRU0_GPO15	PR0_PRU0_GPI15	TRC_DATA13	GPIO0_39			
198	no AC	L23	GPMC0_ADVn_ALE		MCASP1_AXR2		PR0_PRU0_GPO9	PR0_PRU0_GPI9	TRC_DATA7	GPIO0_32			
199	no AC	U23	GPMC0_WAIT0		MCASP1_AFSX		PR0_PRU0_GPO14	PR0_PRU0_GPI14	TRC_DATA12	GPIO0_37			
200	no AC	M24	GPMC0_BE0n_CLE		MCASP1_ACLKX		PR0_PRU0_GPO12	PR0_PRU0_GPI12	TRC_DATA10	GPIO0_35			

8. SOM's Interfaces

8.1 Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 4: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, MIPI CSI, LVDS	100 Ω Differential

8.2 Display Interfaces

8.2.1 OLDI/LVDS

The VAR-SOM-AM62 exports the AM62x Sitara's two single-link Open LVDS Display Interface transmitters (OLDITX) provided by the Display Subsystem (DSS) with the following main features:

- Up to 170MHz input pixel data for each interface support: RGB[23:0], VS, HS, DE. Limited by the maximum data rate provided by the DISPC video port output connected to OLDITX.
- One single-link OLDI output link mode.
- Two single-link (duplicate) OLDI output link mode.
- One dual-link OLDI output link mode.
- 18-bit or 24-bit output with OLDI mapping modes (three or four LVDS data channels, one clock channel) per instance.
- LVDS signaling: Compliant with ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits).
- LVDS transmit throughput performance: 1920x1080@60fps.
- Up to 165 MHz pixel clock support with Independent PLL.
- Test support features: Built-in pattern generator; loopback mode.

8.2.1.1 LVDS0 Signals

Table 5: LVDS0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
161		OLDI0_A0N	0	LVDS0 Data0 Differential Pair Negative side	AA5
163		OLDI0_A0P	0	LVDS0 Data0 Differential Pair Positive side	Y6
160		OLDI0_A1N	0	LVDS0 Data1 Differential Pair Negative side	AD3
162		OLDI0_A1P	0	LVDS0 Data1 Differential Pair Positive side	AB4
164		OLDI0_A2N	0	LVDS0 Data2 Differential Pair Negative side	Y8
166		OLDI0_A2P	0	LVDS0 Data2 Differential Pair Positive side	AA8
165		OLDI0_A3N	0	LVDS0 Data3 Differential Pair Negative side	AB6
167		OLDI0_A3P	0	LVDS0 Data3 Differential Pair Positive side	AA7
168		OLDI0_CLK0N	0	LVDS0 clock Differential Pair Negative side	AD4
170		OLDI0_CLK0P	0	LVDS0 clock Differential Pair Positive side	AE3

8.2.1.2 LVDS1 Signals

Table 6: LVDS1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
184		OLDI0_A4N	0	LVDS1 Data0 Differential Pair Negative side	AC6
186		OLDI0_A4P	0	LVDS1 Data0 Differential Pair Positive side	AC5
188		OLDI0_A5N	0	LVDS1 Data1 Differential Pair Negative side	AE5
190		OLDI0_A5P	0	LVDS1 Data1 Differential Pair Positive side	AD6
192		OLDI0_A6N	0	LVDS1 Data2 Differential Pair Negative side	AE6
194		OLDI0_A6P	0	LVDS1 Data2 Differential Pair Positive side	AD7
183		OLDI0_A7N	0	LVDS1 Data3 Differential Pair Negative side	AD8
181		OLDI0_A7P	0	LVDS1 Data3 Differential Pair Positive side	AE7
180		OLDI0_CLK1N	0	LVDS1 clock Differential Pair Negative side	AE4
182		OLDI0_CLK1P	0	LVDS1 clock Differential Pair Positive side	AD5

8.3 Camera Interface

8.3.1 MIPI CSI-2

The VAR-SOM-AM62 exports one Camera Serial interface 4 Lane with DPHY provided by the AM62x CSI_RX_IF module.

The CSI_RX_IF deals with the processing of the pixel data coming from an external image sensor and supports the following features:

- Compliant to MIPI CSI-2 v1.3
- Supports up to 16 virtual channels per input (partial MIPI CSI v2.0 feature)
- Data rate up to 1.5 Gbps per lane (wire rate)
- Supports 1, 2, 3, or 4 Data Lane connection to DPHY_RX
- Programmable formats including YUV420, YUV422, RGB, Raw, and User Defined (over 25 different formats supported)
- One independent (simultaneous) output stream:
    - One (up to 32 Channels) DMA interface through a 128-bit PSI_L connection to DMSS for transfers to memory:
        - Byte packed (32x4) format, elastic buffer mode
        - Max rate 1 data cycle every 4 main clocks
        - ByteValid per byte in Last Data Phase (LDP)
        - 32 thread ID's supported (virtual channel & data type combinations); Flexible number of threads (32 Max)
        - Virtual channels and data types mapped via mmr to PSI_L thread ID's
        - Internal FF based FIFO; RAM based buffer (2kx128)
- Functional and data path error interrupts
- ECC support

8.3.1.1 MIPI-CSI2 Signals

Table 7: MIPI-CSI2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
137		CSI0_RXCLKN		Differential Pair Negative side	AD15
135		CSI0_RXCLKP		Differential Pair Positive side	AE15
121		CSI0_RXN0		Differential Pair Negative side	AB14
119		CSI0_RXP0		Differential Pair Positive side	AC15
123		CSI0_RXN1		Differential Pair Negative side	AD14
125		CSI0_RXP1		Differential Pair Positive side	AE14
129		CSI0_RXN2		Differential Pair Negative side	AD13
127		CSI0_RXP2		Differential Pair Positive side	AE13
131		CSI0_RXN3		Differential Pair Negative side	AB12
133		CSI0_RXP3		Differential Pair Positive side	AC13

8.4 Ethernet Interface

The AM62x device has an integrated one 3-port Gigabit Ethernet Switch subsystem into device MAIN domain named CPSW0. The CPSW0 subsystem provides Ethernet packet communication for the device and can be configured as an Ethernet switch.
The CPSW3G subsystem supports two external Ethernet ports both capable of simultaneous operation.

The 3-port CPSW0 subsystem provides the following features:

- Two Ethernet ports (port 1 and 2) with selectable RGMII and RMII interfaces and an internal Communications
- Port Programming Interface (CPPI) port (port 0)
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Cut through switch support
- Eight priority level Quality Of Service (QOS) support (802.1p)
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
    - Timestamp module capable of time stamping external timesync events like Pulse-Per-Second and also generating Pulse-Per-Second outputs
    - CPTS module that supports time stamping for IEEE1588 with support for 4 hardware push events and generation of compare output pulses
- DSCP Priority Mapping (IPv4 and IPv6)
- Energy Efficient Ethernet (EEE) support (802.3az)
- Flow Control Support (802.3x)
- Wire rate switching (802.1d)
- Non-Blocking switch fabric
- Time Sensitive Network Support
    - IEEE P802.3br Interspersing Express Traffic
    - IEEE 802.1Qbv Enhancements for Scheduled Traffic
- Address Lookup Engine (ALE)
    - 512 ALE table entries
    - Configurable number of addresses plus VLANs
    - Wire rate lookup
    - Host controlled time-based aging and/or auto-aging
    - Spanning tree support
    - L2 address lock and L2 filtering support
    - MAC authentication (802.1x)
    - Receive-based or destination-based Multicast and Broadcast rate limits
    - MAC address blocking
    - Source port locking
    - OUI (Vendor ID) host accept/deny feature
    - Configurable number of classifier/policers (32)
    - VLAN support
        - 802.1Q compliant:
          Auto add port VLAN for untagged frames on ingress
          Auto VLAN removal on egress and auto pad to minimum frame size
- EtherStats and 802.3Stats Remote Network Monitoring (RMON) statistics gathering (per port statistics)

- Ethernet Mac transmit to Ethernet Mac receive Loopback mode (digital loopback) supported
- CPSGMII Loopback Modes (transmit to receive)
- Maximum frame size of 2024 bytes
- Management Data Input/Output (MDIO) module for PHY Management with Clause 45 support
- Programmable interrupt control with selected interrupt pacing
- Host port CPPI Streaming Packet Interface (CPPI_GCLK)
- Digital loopback and FIFO loopback modes supported
- Emulation support
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps modes only.
- RAM Error Detection and Correction (SECDED)

8.4.1 RGMII1/RMII1

The SOM can be ordered in one of the following configurations:

- **"EC" configuration** – The VAR-SOM-AM62 includes an on SOM a Gigabit PHY Analog Devices ADIN1300 connected to RGMII1 interface signals.
  External connector and magnetics should be implemented on carrier board to complete the interface to the media.
- **"no EC" configuration** - The VAR-SOM-AM62 exposes the RGMII1/RMII1 interface signals to the SO-DIMM connector, pins will be referenced to voltage level depending on "RG2CM" configuration:
  - In **"no RG2CM" configuration** – RGMII1/RMII1 pins will be referenced to 3.3V
  - In **"RG2CM" configuration** – RGMII1/RMII1 pins will be referenced to 1.8V

8.4.1.1 Ethernet PHY

The on-SOM Analog Devices ADIN1300 Gigabit PHY in conjunction with the external magnetics on carrier board complete the interface to the media.
PHY LINK LEDs 10/100 and 1000 combined on SOM to one signal 10/100/1000.

The Following External Gigabit magnetics are required to complete the Ethernet PHY interface to the media.

Table 8: Gigabit Ethernet Magnetics

Vendor	P/N	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

Table 9: Ethernet PHY Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
15	EC	ETH0_LED_ACT		Signal source is Ethernet PHY Ethernet PHY Activity LED, active low	ADIN1300.21
16	EC	ETH0_LED_LINK_10_100_1000		Signal source is Ethernet PHY Ethernet PHY Link LED, active low	ADIN1300.26 via inv. FET
5	EC	ETH0_MDI_A_M		Signal source is Ethernet PHY	ADIN1300.13
3	EC	ETH0_MDI_A_P		Differential Pair Positive side Signal source is Ethernet PHY	ADIN1300.12
11	EC	ETH0_MDI_B_M		Signal source is Ethernet PHY	ADIN1300.15
9		ETH0_MDI_B_P		Differential Pair Positive side	ADIN1300.14
6	EC	ETH0_MDI_C_M		Signal source is Ethernet PHY	ADIN1300.17
4	EC	ETH0_MDI_C_P		Differential Pair Positive side Signal source is Ethernet PHY	ADIN1300.16
12	EC	ETH0_MDI_D_M		Signal source is Ethernet PHY	ADIN1300.19
10	EC	ETH0_MDI_D_P		Differential Pair Positive side Signal source is Ethernet PHY	ADIN1300.18
1	EC	NC		With "EC" configuration this pin is Not Connected	NC
97	EC	NC		With "EC" configuration this pin is Not Connected	NC

Table 10: ADIN1300 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100_1000	ON	ON	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

8.4.1.2 RGMII1/RMII1 Signals

Table 11: RGMII1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
4	no EC	RGMII1_RD0	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	AB17
6	no EC	RGMII1_RD1	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	AC17
10	no EC	RGMII1_RD2	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	AB16
12	no EC	RGMII1_RD3	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	AA15
15	no EC	RGMII1_RX_CTL	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Receive Control signal	AE17
16	no EC	RGMII1_RXC	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL;	AD17
11	no EC	RGMII1_TD0	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	AE20
9	no EC	RGMII1_TD1	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	AD20
5	no EC	RGMII1_TD2	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	AE18
3	no EC	RGMII1_TD3	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	AD18
1	no EC	RGMII1_TX_CTL	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input! RGMII - Transmit Control signal	AD19
97	no EC	RGMII1_TXC	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	AE19

Table 12: RMII1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		CLKOUT0	5	RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	A18
97	no EC	RMII1_CRS_DV	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII - Carrier sense/receive data valid	AE19
16	no EC	RMII1_REF_CLK	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII - 50MHz reference clock.	AD17
15	no EC	RMII1_RX_ER	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII - Receive error	AE17
4	no EC	RMII1_RXD0	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII Data in	AB17
6	no EC	RMII1_RXD1	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII Data in	AC17
1	no EC	RMII1_TX_EN	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input! RMII - transmit enable	AD19
11	no EC	RMII1_TXD0	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII Data out	AE20
9	no EC	RMII1_TXD1	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII Data out	AD20

8.4.2 RGMII2/RMII2

RGMII2/RMII2 interface signals are always exported through SO-DIMM connector.
Signals, in conjunction to MDIO signals exported from SO-DIMM connector, they can be used to interface an external Ethernet PHY.

Voltage level depends on "RG2CM" configuration:

- In **"no RG2CM" configuration** – RGMII2/RMII2 pins will be referenced to 3.3V
- In **"RG2CM" configuration** – RGMII2/RMII2 pins will be referenced to 1.8V

8.4.2.1 RGMIII2/RMII2 Signals

Table 13: RGMII2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
122		RGMII2_RD0	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	AE23
81		RGMII2_RD1	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	AB20
71		RGMII2_RD2	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	AC21
54		RGMII2_RD3	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	AE22
120		RGMII2_RX_CTL	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Receive Control signal	AD22
57		RGMII2_RXC	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL;	AD23
73		RGMII2_TD0	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	Y18
177		RGMII2_TD1	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	AA18
56		RGMII2_TD2	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	AD21
55		RGMII2_TD3	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	AC20
113		RGMII2_TX_CTL	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Transmit Control signal	AA19
96		RGMII2_TXC	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	AE21

Table 14: RMII2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		CLKOUT0	5	RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	A18
96		RMII2_CRS_DV	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII - Carrier sense/receive data valid	AE21
57		RMII2_REF_CLK	1	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V; RMII - 50MHz reference clock.	AD23
120		RMII2_RX_ER	1	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V; RMII - Receive error	AD22
122		RMII2_RXD0	1	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V; RMII Data in	AE23
81		RMII2_RXD1	1	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V; RMII Data in	AB20
113		RMII2_TX_EN	1	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V; RMII - transmit enable	AA19
73		RMII2_TXD0	1	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V; RMII Data out	Y18
177		RMII2_TXD1	1	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V; RMII Data out	AA18

8.4.3 RGMII1/RMII1 & RGMIII2/RMII2 Control Signals

Table 15: RGMII1/RMII1 & RGMIII2/RMII2 control Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
30		MDIO0_MDIO	0	Pin is referenced to 3.3V, and has an internal 1.47K Pull Up. In "RG2CM" configuration pin is routed via on SOM 1.8<->3.3V voltage translator.; Do not alter pinmux with "EC" configuration	AB22
74		MDIO0_MDC	0	Pin is referenced to 3.3V. In "RG2CM" configuration pin is routed via on SOM 1.8<->3.3V voltage translator.; Do not alter pinmux with "EC" configuration	AD24

8.4.4 Common Platform Time Sync (CPTS)

The Common Platform Time Sync (CPTS) module is used to facilitate host control of time sync operations. It enables compliance with the IEEE 1588-2008 standard for a precision clock synchronization protocol.

Main features of CPTS module are:

- Supports the selection of multiple external clock sources
- Software control of time sync events via interrupt or polling
- Supports up to 8 hardware timestamp push inputs
- Supports timestamp counter compare output (CPTS_COMP)
- Supports timestamp counter bit output (CPTS_SYNC)
- Supports a configurable number of timestamp Generator bit outputs (CPTS_GENFn).
- Supports Ethernet Enhanced Scheduled Traffic Operations (CPTS_ESTFn).
- 32-bit and 64-bit timestamp modes with PPM and nudge adjustment.

NOTE

CPTS has one or more signals which can be exported from more than one pin.
However, only specific pin combinations known as IOSETs are valid.
These are defined in TI's SysConfig-PinMux Tool.
The below tables present the valid IOSETs

Table 16: CPTS Signal Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		CP_GEMAC_CPTS0_RFT_CLK	6	CPTS Reference Clock Input	A18
88		SYNC0_OUT	2	CPTS Time Stamp Generator Bit 0 Output from Time Sync Router	B16
29		SYNC1_OUT	1	CPTS Time Stamp Generator Bit 1 Output from Time Sync Router	A18
44		SYNC2_OUT	3	CPTS Time Stamp Generator Bit 2 Output from Time Sync Router	C15
46		SYNC3_OUT	3	CPTS Time Stamp Generator Bit 3 Output from Time Sync Router	E15

Table 17: CPTS Signal IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
187	no TP	CP_GEMAC_CPTS0_HW1TSPUSH	1	CPTS Hardware Time Stamp Push Input to Time Sync Router Available in SOM without TP	B13
193	no TP	CP_GEMAC_CPTS0_HW2TSPUSH	1	CPTS Hardware Time Stamp Push Input to Time Sync Router Available in SOM without TP	B14
68		CP_GEMAC_CPTS0_TS_COMP	1	CPTS Time Stamp Counter Compare Output from CPSW3G0 CPTS	C13
189	no TP	CP_GEMAC_CPTS0_TS_SYNC	1	CPTS Time Stamp Counter Bit Output from CPSW3G0 CPTS Available in SOM without TP	A14

Table 18: CPTS Signal IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
63		CP_GEMAC_CPTS0_HW1TSPUSH	1	CPTS Hardware Time Stamp Push Input to Time Sync Router Bank voltage set on SOM 1.8V/3.3V	B21
62		CP_GEMAC_CPTS0_HW2TSPUSH	1	CPTS Hardware Time Stamp Push Input to Time Sync Router Bank voltage set on SOM 1.8V/3.3V	A22
65		CP_GEMAC_CPTS0_TS_COMP	1	CPTS Time Stamp Counter Compare Output from CPSW3G0 CPTS Bank voltage set on SOM 1.8V/3.3V	D22
61		CP_GEMAC_CPTS0_TS_SYNC	1	CPTS Time Stamp Counter Bit Output from CPSW3G0 CPTS Bank voltage set on SOM 1.8V/3.3V	C21

8.5 Wi-Fi & BT

The VAR-SOM-AM62 contains a certified high-performance Wi-Fi (Single or Dual Band option) and Bluetooth (BT) module:

- IEEE 802.11 ac/a/b/g/n (Dual Band Option)
- IEEE 802.11 b/g/n (Single Band Option)
- Bluetooth 2.1+EDR
- BLE 5.2 capabilities
- Modules have an antenna connection through a U. FL JACK connector
- Antenna cable connected to module must have 50-Ω impedance

Figure 3 illustrates the VAR-SOM-AM62 internal Wi-Fi and BT connectivity.

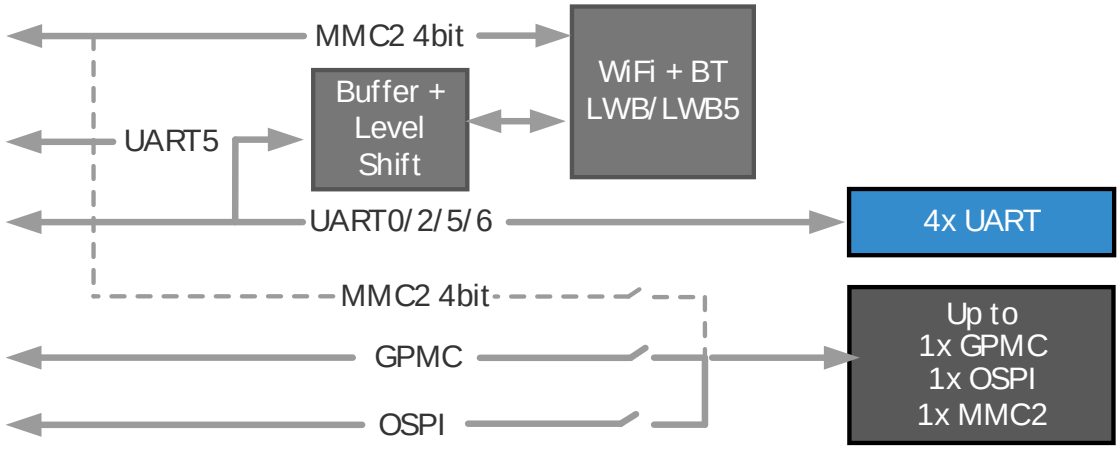


Figure 3: VAR-SOM-AM62 Wi-Fi & BT Internal Connection

To allow the most flexible solution the following elements are added to the VAR-SOM-AM62:

- Buffer with tristate on the BT link based on UART interface.
  Will allow isolation from the BT module and the use by external circuity via the VAR-SOM-AM62 connector.
- Dedicated MMCSD channel for the Wi-Fi module interface which can be exported to SOM pins in case WIFI module is not assembled.

NOTE

BT UART tristate buffer controlled using GPIO0_53.

- Logic “High” enables the buffer
- Logic “Low” disable it and releases the signals to be used via SOM connector.

8.5.1 Interface Implementation Options

8.5.1.1 Module Configuration with “WBD” or “WB” Option

- System use: Wi-Fi and Bluetooth.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT buffer (using GPIO0_53) and BT function.
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi.**
  - Disable Wi-Fi function.
  - Enable the BT buffer (using GPIO0_53) and BT function.

8.5.1.2 Module Configuration without “WBD” or “WB” Option

- System use: **no Wi-Fi and no BT**.
  - BT UART interface accessible externally with any of its alternative functions.
  - MMC2 interface accessible externally in case of SOM configuration with “MMC2”

8.5.2 Bluetooth Interface Signals

Table 19: BT UART Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
50		UART5_RTSn	4	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	AB25
51		UART5_CTSn	4	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	AA24
52		UART5_TXD	4	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	AA25
53		UART5_RXD	4	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	Y23

8.6 Multi-Media Card Secure Digital (MMCSD)

The VAR-SOM-AM62 exposes the MMCSD1/MMCSD2 controller 4-bit interface.

Key features of MMCSD:
SD Host Controller Standard Specification 4.10 and SD Physical
Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications

- SD Host Controller Standard Specification 4.10
- SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00
- 1.8 V and 3.3 V operation
- 1-bit/4-bit SD and SDIO modes
- Up to SDR104 rate

MMCSD1 interface is used for supporting interface between the host system and the SD/SDIO/MMC cards.

MMCSD2 is used internally for the Wi-Fi SDIO interface on the SOM.
In case of SOM Module Configuration without “WBD” or “WB” and with “MMC2” interface MMCSD2 interface is accessible externally via SOM pins

8.6.1 MMCSD1 Signals

For ***Card Detect function*** any GPIO can be used; For pinout compatibility with other SOMs of VAR-SOM pin2pin family, pin 80 GPIO1_48 is used.

Table 20: MMCSD1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
60		MMC1_CLK	0	Bank voltage set on SOM 1.8V/3.3V	B22
64		MMC1_CMD	0	Bank voltage set on SOM 1.8V/3.3V	A21
62		MMC1_DAT0	0	Bank voltage set on SOM 1.8V/3.3V	A22
63		MMC1_DAT1	0	Bank voltage set on SOM 1.8V/3.3V	B21
61		MMC1_DAT2	0	Bank voltage set on SOM 1.8V/3.3V	C21
65		MMC1_DAT3	0	Bank voltage set on SOM 1.8V/3.3V	D22
80		MMC1_SDCD	0	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D17

8.6.2 MMCSD2 Interface Signals

Table 21: MMC2 Supply voltage input Signal

Pin#	Assy	Pin Function	Alt#	Notes	Ball
36	MMC2 & no (WB or WBD)	VDDSHV6		MMC2 pins group power IN “no MMC2" configuration: * Not Connected "MMC2" configuration: VDDSHV6 1.8V/3.3V voltage input. Must supply one option: 1.8 or 3.3V, Use SOM pin 49 to sequence 1.8 or 3.3V supply. The following SOM pins are referenced to this voltage: 31,33,35,47,59,76,100,102	J18

Table 22: MMC2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
76	MMC2 & no (WB or WBD)	MMC2_CLK	0	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	D25
100	MMC2 & no (WB or WBD)	MMC2_CMD	0	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	C24
102	MMC2 & no (WB or WBD)	MMC2_DAT0	0	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	B24
35	MMC2 & no (WB or WBD)	MMC2_DAT1	0	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	C25
33	MMC2 & no (WB or WBD)	MMC2_DAT2	0	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	E23
31	MMC2 & no (WB or WBD)	MMC2_DAT3	0	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	D24
47	MMC2 & no (WB or WBD)	MMC2_SDCD	0	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	A23
92		MMC2_SDCD	9		B17
59	MMC2 & no (WB or WBD)	MMC2_SDWP	0	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	B23
90		MMC2_SDWP	9		A17

8.6.3 MMCSD3 Signals

MMCSD controller, MMCSD3, is used internally for the eMMC interface on the SOM.

8.7 USB 2.0

The VAR-SOM-AM62 consists Two USB controllers and PHYs that support USB 2.0

The USB 2.0 subsystem supports the following USB Features:

- Operational modes:
  - Supports USB 2.0 Host mode at High-Speed (HS, 480 Mbps), Full-Speed (FS, 12 Mbps), and Low-Speed (LS, 1.5 Mbps)
  - Supports USB 2.0 Device mode at High-Speed (HS, 480 Mbps), and Full-Speed (FS, 12 Mbps). LowSpeed is not supported in Device mode.
  - Supports all modes of transfers - Control, Bulk, Interrupt, and Isochronous.
- A DRD (Dual-Role-Device - Host or Device) USB controller with the following features:
  - Compatible to the xHCI 1.0 specification in Host mode
  - Compatible with the USB 2.0 specification in Device mode
  - Supports 15 IN (Receive), 15 OUT (Transmit) endpoints (EPs), and one EP0 endpoint which is bidirectional
  - Internal DMA controller
  - Descriptor caching and data pre-fetching ensures high performance
  - Dynamic FIFO memory allocation for all endpoints
- Operation flexibility
  - Same programming model for HS, FS, and LS operation
  - Each controller instance can provide either USB Host or USB Device functionality

8.7.1 USB Port0/Port1 Interface Signals

Table 23: USB 2.0 Port0/Port1 Interface signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
114		USB0_DM		Differential Pair Negative side, USB DRD capable	AE11
116		USB0_DP		Differential Pair Positive side, USB DRD capable	AD11
94		USB0_DRVVBUS		USB PWR signal, active high control signal used to enable power to the downstream port switch.	C20
106		USB0_VBUS		USB PHY power pin (5V) input	AC11
108		USB1_DM		Differential Pair Negative side, USB DRD capable	AD10
110		USB1_DP		Differential Pair Positive side, USB DRD capable	AE9
82		USB1_DRVVBUS		USB PWR signal, active high control signal used to enable power to the downstream port switch.	F18
104		USB1_VBUS		USB PHY power pin (5V) input	AB10

USBx_ID

The USB PHY ID pin functionality can be implemented via any GPIO:

- "Low" means the SoC is Host role
- "High" or “Float” means the SoC is Device role.

8.8 Audio

The VAR-SOM-AM62 features the following audio interfaces:

- WM8904CGEFL Audio codec interfaces:
  - Analog outputs & inputs: stereo line-in & Stereo HP out.
  - Digital microphone input
- 3x Multichannel Audio Serial Ports (McASP)
  - Transmit and Receive Clocks up to 50 MHz
  - Up to 16/10/6 Serial Data Pins across 3 McASP with Independent TX and RX Clocks
  - Supports Time Division Multiplexing (TDM) Inter-IC Sound (I2S), and Similar Formats
  - Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 Formats)
  - FIFO Buffers for Transmit and Receive (256 Bytes)
  - Support for audio reference output clock

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only. The codec interfaces the SoC via McASP1 lines, when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

The following figure illustrates the connectivity for no large AC coupling capacitors implemented on SOM.

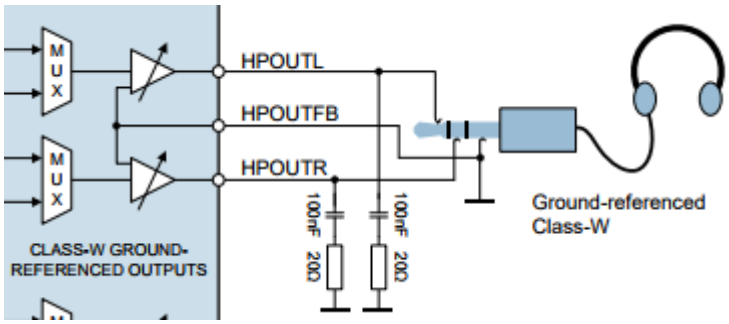


Figure 4: WM8904 Headphone connectivity

8.8.1 WM8904CGEFL Audio Codec

8.8.1.1 Audio Codec Signals

Table 24: Analog audio Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
195		AGND		Audio Ground	AGND
18	AC	DMIC_CLK		Signal source is Audio Codec Digital microphone clock output	WM8904.1
20	AC	DMIC_DATA		Signal source is Audio Codec Digital microphone data input; Divided internally by 475 Ohm resistors to match Codec input levels	WM8904.27
198	AC	HPLOUT		Signal source is Audio Codec Left headphone output (line or headphone output)	WM8904.13
196	AC	HPOUTFB		Signal source is Audio Codec Headphone output ground loop noise rejection feedback	WM8904.14
200	AC	HPROUT		Signal source is Audio Codec Right headphone output (line or headphone output)	WM8904.15
197	AC	LINEIN1_LP		Signal source is Audio Codec Left channel input	WM8904.26
199	AC	LINEIN1_RP		Signal source is Audio Codec Right channel input	WM8904.24

8.8.2 Multichannel Audio Serial Ports (McASP)

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although inter-component digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

NOTE

McASP has one or more signals which can be exported from more than one pin.
However, only specific pin combinations known as IOSETs are valid.
These are defined in TI's SysConfig-PinMux Tool.
The below tables present the valid IOSETs

The following table details the MCASP and AUDIO_EXT_REFCLK interface signals definition.

Table 25: SAI interface signals definition

Name	Function	DIR
MCASPx_AXRxx	Audio transmit/receive data – channel xx	I/O
MCASPx_ACLKX	Transmit bit clock	I/O
MCASPx_AFSX	Transmit frame synchronization	I/O
MCASPx_ACLKR	Receive bit clock	I/O
MCASPx_AFSR	Receive frame synchronization	I/O
AUDIO_EXT_REFCLKx	Transmit/ Receive high-frequency controller clock	I/O

8.8.2.1 McASP0 Signals

Table 26: McASP0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
43		MCASP0_ACLKR	0		A20
117		MCASP0_ACLKX	0		B20
39		MCASP0_AFSR	0		E19
72		MCASP0_AFSX	0		D20
69		MCASP0_AXR0	0		E18
17		MCASP0_AXR1	0		B18
41		MCASP0_AXR2	0		A19
45		MCASP0_AXR3	0		B19

8.8.2.2 McASP1 Signals

Note: McASP1 interface is used by internal Audio Codec.
McASP1interface can be used externally only in SOMs without "AC" assembly option.

Table 27: McASP1 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
47	OSPI	MCASP1_AXR3	4	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	E24
79		MCASP1_AXR1	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J23
75		MCASP1_AXR0	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J25
70		MCASP1_ACLKX	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	H25
77		MCASP1_AFSX	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J22

Table 28: McASP1 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
79		MCASP1_AXR1	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J23
75		MCASP1_AXR0	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J25
70		MCASP1_ACLKX	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	H25
77		MCASP1_AFSX	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J22
47	OSPI	MCASP1_ACLKR	3	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	E24

Table 29: McASP1 IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
59	GPMC	MCASP1_AXR3	2	Available in SOM with "GPMC" configuration;	P25
198	no AC	MCASP1_AXR2	2	Available in SOM without "AC" configuration	L23
36	GPMC	MCASP1_AXR1	2	Available in SOM with "GPMC" configuration;	L24
18	no AC & no GPMC	MCASP1_AXR0	2	Available in SOM without "AC" and without "GPMC" configuration	L25
200	no AC	MCASP1_ACLKX	2	Available in SOM without "AC" configuration	M24
199	no AC	MCASP1_AFSX	2	Available in SOM without "AC" configuration	U23
174		MCASP1_AFSR	8	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K22
176		MCASP1_ACLKR	8	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K24

Table 30: McASP1 IOSet_4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
176		MCASP1_AXR5	4	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K24
174		MCASP1_AXR4	2	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K22
59	GPMC	MCASP1_AXR3	2	Available in SOM with "GPMC" configuration;	P25
198	no AC	MCASP1_AXR2	2	Available in SOM without "AC" configuration	L23
36	GPMC	MCASP1_AXR1	2	Available in SOM with "GPMC" configuration;	L24
18	no AC & no GPMC	MCASP1_AXR0	2	Available in SOM without "AC" and without "GPMC" configuration	L25
200	no AC	MCASP1_ACLKX	2	Available in SOM without "AC" configuration	M24
199	no AC	MCASP1_AFSX	2	Available in SOM without "AC" configuration	U23

Table 31: McASP1 IOSet_5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	MMC2 & no (WB or WBD)	MCASP1_AXR3	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	D24
33	MMC2 & no (WB or WBD)	MCASP1_AXR2	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	E23
35	MMC2 & no (WB or WBD)	MCASP1_AXR1	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	C25
102	MMC2 & no (WB or WBD)	MCASP1_AXR0	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	B24
47	MMC2 & no (WB or WBD)	MCASP1_ACLKX	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	A23
59	MMC2 & no (WB or WBD)	MCASP1_AFSX	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	B23
100	MMC2 & no (WB or WBD)	MCASP1_AFSR	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	C24
76	MMC2 & no (WB or WBD)	MCASP1_ACLKR	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	D25

Table 32: McASP1 IOSet_6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
76	MMC2 & no (WB or WBD)	MCASP1_AXR5	2	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	D25
100	MMC2 & no (WB or WBD)	MCASP1_AXR4	2	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	C24
31	MMC2 &	MCASP1_AXR3	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	D24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
	no (WB or WBD)				
33	MMC2 & no (WB or WBD)	MCASP1_AXR2	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	E23
35	MMC2 & no (WB or WBD)	MCASP1_AXR1	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	C25
102	MMC2 & no (WB or WBD)	MCASP1_AXR0	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	B24
47	MMC2 & no (WB or WBD)	MCASP1_ACLKX	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	A23
59	MMC2 & no (WB or WBD)	MCASP1_AFSX	1	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	B23

8.8.2.3 McASP2 Signals

Table 33: McASP2 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
102	GPMC	MCASP2_AXR15	3	Available in SOM with "GPMC" configuration;	L21
100	GPMC	MCASP2_AXR14	3	Available in SOM with "GPMC" configuration;	M21
35	GPMC	MCASP2_AXR13	3	Available in SOM with "GPMC" configuration;	M22
47	GPMC	MCASP2_AXR12	3	Available in SOM with "GPMC" configuration;	N20
40		MCASP2_AXR11	3	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R23
86		MCASP2_AXR10	3	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P21
48		MCASP2_AXR9	3	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P22
84		MCASP2_AXR8	3	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P24
173		MCASP2_AXR7	3	BOOTMODE03 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N25
76	GPMC	MCASP2_AXR6	3	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N24
33	GPMC	MCASP2_AXR5	3	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N23
31	GPMC	MCASP2_AXR4	3	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	M25

Pin#	Assy	Pin Function	Alt#	Notes	Ball
26		MCASP2_AXR3	3	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R21
21		MCASP2_AXR2	3	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T25
171		MCASP2_AXR1	3	BOOTMODE09 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R25
115		MCASP2_AXR0	3	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R24
25		MCASP2_ACLKX	3	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T24
24		MCASP2_AFSX	3	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T22
23		MCASP2_AFSR	3	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U25
22		MCASP2_ACLKR	3	BOOTMODE15 pin, 100K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U24

Table 34: McASP2 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
73		MCASP2_AXR6	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	Y18
96		MCASP2_AXR5	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE21
113		MCASP2_AXR4	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AA19
120		MCASP2_AXR3	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AD22
122		MCASP2_AXR2	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AE23
57		MCASP2_AXR1	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AD23
71		MCASP2_AXR0	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AC21
55		MCASP2_ACLKX	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AC20
56		MCASP2_AFSX	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AD21
81		MCASP2_AFSR	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AB20
177		MCASP2_ACLKR	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AA18

Table 35: McASP2 IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
177		MCASP2_AXR8	5	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AA18
81		MCASP2_AXR7	5	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AB20
73		MCASP2_AXR6	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	Y18
96		MCASP2_AXR5	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE21
113		MCASP2_AXR4	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AA19
120		MCASP2_AXR3	2	By default, referenced to 3.3V,	AD22

Pin#	Assy	Pin Function	Alt#	Notes	Ball
				In “RG2CM” configuration referenced to 1.8V;	
122		MCASP2_AXR2	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AE23
57		MCASP2_AXR1	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AD23
71		MCASP2_AXR0	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AC21
55		MCASP2_ACLKX	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AC20
56		MCASP2_AFSX	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AD21

8.8.2.4 Audio External reference clock Signals

The VAR-SOM-AM62 exports also the AUDIO_EXT_REFCLK[0-1] signals which can be used as External clock input to McASP or output from McASP

Table 36: AUDIO_EXT_REFCLK Signals

54		AUDIO_EXT_REFCLK0	2	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AE22
69		AUDIO_EXT_REFCLK0	2		E18
20	no AC & no GPMC	AUDIO_EXT_REFCLK1	1	Available in SOM without "AC” and without "GPMC" configuration	K25
72		AUDIO_EXT_REFCLK1	2		D20
197	no AC & GPMC	AUDIO_EXT_REFCLK1	1	Available in SOM without "AC” and with "GPMC" configuration	K25

8.9 Resistive Touch

The VAR-SOM-AM62 features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

The Resistive Touch is available only in SOMs with the “TP” assembly option
when not assembled, SPI0 SoC balls are exported to SOM connector instead of Resistive Touch interface pins.

8.9.1.1 Resistive Touch Signals

Table 37: Serial Resistive Touch Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
187	TP	TS_X-		Signal source is Resistive Touch controller	TSC2046.8
189	TP	TS_X+		Signal source is Resistive Touch controller	TSC2046.6
191	TP	TS_Y+		Signal source is Resistive Touch controller	TSC2046.7
193	TP	TS_Y-		Signal source is Resistive Touch controller	TSC2046.9

8.10 UART

The VAR-SOM-AM62 exposes up to nine UART interfaces. UART5 is used on SOM for Bluetooth interface and can be accessible only if the on SOM buffer is disabled or on SOM without ***"WBD" and "WB" Configuration***.

The UART includes the following features:

- Edge-selectable RTS_B and edge-detect interrupts
- 16C750-compatible
- RS-485 external transceiver auto flow control support
- 64-byte FIFO buffer for receiver and 64-byte FIFO buffer for transmitter
- Programmable interrupt trigger levels for FIFOs
- Programmable sleep mode
- The 48 MHz functional clock is default option and allows baud rates up to 3.6 Mbps
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Optional multi-drop transmission
- Configurable time-guard feature
- Configurable data format:
    - Parity bit: Even, odd, none
    - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- False start bit detection
- Line break generation and detection
- Fully prioritized interrupt system controls

Table 38: UART I/O Configuration vs. mode

Module Pin Name	Device Level Signal Name	I/O	Description	Module Pin Reset Value
WKUP_UARTi				
RX	WKUP_UARTi_RXD	I	Serial data input	HiZ
TX	WKUP_UARTi_TXD	O	Serial data output	1
CTS	WKUP_UARTi_CTS	I	Clear to send	HiZ
RTS	WKUP_UARTi_RTS	O	Request to send	1
MCU_UARTi				
RX	MCU_UARTi_RXD	I	Serial data input	HiZ
TX	MCU_UARTi_TXD	O	Serial data output	1
CTS	MCU_UARTi_CTS	I	Clear to send	HiZ
RTS	MCU_UARTi_RTS	O	Request to send	1
UARTi Modem Signals				
DCD	UARTi_DCDn	I		HiZ
DSR	UARTi_DSRn	I		HiZ
DTR	UARTi_DTRn	O		1
RIN	UARTi_RIN	I		HiZ

Note: i represents a UART instance.

8.10.1 UART0 Signals

Table 39: UART0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
83		UART0_RXD	0	Used as debug UART on Variscite base board	D14
85		UART0_TXD	0	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	E14

8.10.2 UART1 Signals

Table 40: UART1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
45		UART1_CTSn	2		B19
88		UART1_DCDn	4		B16
87		UART1_DSRn	4		A16
44		UART1_DTRn	4		C15
46		UART1_RIn	4		E15
41		UART1_RTSn	2		A19
39		UART1_RXD	2		E19
92		UART1_RXD	1		B17
43		UART1_TXD	2		A20
90		UART1_TXD	1		A17

8.10.3 UART2 Signals

Table 41: UART2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
23		UART2_CTSn	8	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U25
62		UART2_CTSn	3	Bank voltage set on SOM 1.8V/3.3V	A22
22		UART2_RTSn	8	BOOTMODE15 pin, 100K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U24
63		UART2_RTSn	3	Bank voltage set on SOM 1.8V/3.3V	B21
65		UART2_RXD	3	Bank voltage set on SOM 1.8V/3.3V	D22
115		UART2_RXD	2	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R24
61		UART2_TXD	3	Bank voltage set on SOM 1.8V/3.3V	C21
171		UART2_TXD	2	BOOTMODE09 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R25

8.10.4 UART3 Signals

Table 42: UART3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
124		UART3_CTSn	3		C17
80		UART3_RTSn	3	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D17
21		UART3_RXD	2	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T25
60		UART3_RXD	3	Bank voltage set on SOM 1.8V/3.3V	B22
26		UART3_TXD	2	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R21
64		UART3_TXD	3	Bank voltage set on SOM 1.8V/3.3V	A21

8.10.5 UART4 Signals

Table 43: UART4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
24		UART4_RXD	2	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T22
47	MMC2 & no (WB or WBD)	UART4_RXD	3	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	A23
174		UART4_RXD	3	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	K22
25		UART4_TXD	2	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T24
59	MMC2 & no (WB or WBD)	UART4_TXD	3	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	B23
176		UART4_TXD	3	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	K24

8.10.6 UART5 Signals

Table 44: UART5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
36	OSPI	UART5_CTSn	5	Available in SOM with "OSPI” configuration; Pin referenced to 1.8V	J24
51		UART5_CTSn	4	Used internally with "WBD", Function can be released if BT Function disabled	AA24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
33	OSPI	UART5_RTSn	5	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	G25
50		UART5_RTSn	4	Used internally with "WBD", Function can be released if BT Function disabled	AB25
23		UART5_RXD	2	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U25
31	MMC2 & no (WB or WBD)	UART5_RXD	3	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	D24
44		UART5_RXD	1		C15
53		UART5_RXD	4	Used internally with "WBD", Function can be released if BT Function disabled	Y23
22		UART5_TXD	2	BOOTMODE15 pin, 100K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U24
33	MMC2 & no (WB or WBD)	UART5_TXD	3	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	E23
46		UART5_TXD	1		E15
47	OSPI	UART5_TXD	5	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	E24
52		UART5_TXD	4	Used internally with "WBD", Function can be released if BT Function disabled	AA25

8.10.7 UART6 Signals

Table 45: UART6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
77		UART6_CTSn	3	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J22
70		UART6_RTSn	3	Pin referenced to 1.8V in SOM with "OSPI" configuration;	H25
45		UART6_RXD	3		B19
76	MMC2 & no (WB or WBD)	UART6_RXD	3	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	D25
79		UART6_RXD	3	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J23
80		UART6_RXD	1	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D17
175		UART6_RXD	3		V25
20	no AC & no GPMC	UART6_TXD	3	Available in SOM without "AC" and without "GPMC" configuration	K25
41		UART6_TXD	3		A19
75		UART6_TXD	3	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J25

Pin#	Assy	Pin Function	Alt#	Notes	Ball
100	MMC2 & no (WB or WBD)	UART6_TXD	3	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	C24
124		UART6_TXD	1		C17
197	no AC & GPMC	UART6_TXD	3	Available in SOM without "AC" and with "GPMC" configuration	K25

8.10.8 MCU UART0 Signals

Table 46: MCU_UART Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
58		MCU_UART0_CTSn	0		A6
93		MCU_UART0_RTSn	0		B6
91		MCU_UART0_RXD	0		B5
99		MCU_UART0_TXD	0		A5

8.10.9 WKUP UART0 Signals

Table 47: WKUP UART Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
142		WKUP_UART0_CTSn	0		C6
143		WKUP_UART0_RTSn	0		A4
145		WKUP_UART0_RXD	0		B4
147		WKUP_UART0_TXD	0		C5

8.11 I2C

The VAR-SOM-AM62 exposes up to 5x I2C Interface connectivity peripherals which provides serial interface for external devices. Data rates of up to 400 kbps are supported.

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices.
This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The I2C has the following key features:

- Compliant with Philips I2C-bus specification version 2.1
- Supports a standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- 7-bit and 10-bit device addressing modes
- General call
- Start/Restart/Stop
- Multicontroller transmitter/target receiver mode
- Multicontroller receiver/target transmitter mode
- Combined controller transmit/receive and receive/transmit mode
- Built-in FIFO for buffered read
- Module enable/disable capability
- Programmable multitarget channel (responds to four separate addresses)
- Programmable clock generation
- 8-bit-wide data access
- Low power consumption
- Support Auto Idle mechanism
- Support Idle Request/Idle Acknowledge handshake mechanism
- Support for asynchronous wakeup mechanism
- Wide interrupt capability

8.11.1 I2C0 Signals

Table 48: I2C0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
88		I2C0_SCL	0		B16
87		I2C0_SDA	0		A16

8.11.2 I2C1 Signals

Table 49: I2C1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
92		I2C1_SCL	0		B17
90		I2C1_SDA	0		A17

8.11.3 I2C2 Signals

Table 50: I2C2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
174		I2C2_SCL	1	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K22
176		I2C2_SDA	1	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K24

8.11.4 I2C3 Signals

I2C3 is used internally by on-SOM EEPROM.

8.11.5 MCU I2C0 Signals

Table 51: MCU I2C0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
146		MCU_I2C0_SCL	0	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	A8
148		MCU_I2C0_SDA	0	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	D10

8.11.6 WKUP I2C0 Signals

Table 52: WKUP I2C0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
140		WKUP_I2C0_SCL	0	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	B9

Pin#	Assy	Pin Function	Alt#	Notes	Ball
141		WKUP_I2C0_SDA	0	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	A9

8.12 Modular Controller Area Network (MCAN)

The Modular Controller Area Network (MCAN) module is a communication controller supporting CAN and CAN FD (CAN Flexible Data Rate) conforming with CAN Protocol 2.0 A, B and ISO 11898-1:2015

Signal Description:

- CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
- CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

8.12.1 MCAN0 Signals

Table 53: MCAN0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
46		MCAN0_RX	0		E15
44		MCAN0_TX	0		C15

8.12.2 MCU_MCAN0 Signals

Table 54: MCU_MCAN0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
155		MCU_MCAN0_RX	0		B3
157		MCU_MCAN0_TX	0		D6

8.12.3 MCU_MCAN1 Signals

Table 55: MCU_MCAN1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
154		MCU_MCAN1_RX	0		D4
156		MCU_MCAN1_TX	0		E5

8.13 Multichannel Serial Peripheral Interface (MCSPI)

The VAR-SOM-AM62 exposes up 5 MCSPI interfaces.

The Multichannel Serial Peripheral Interface (MCSPI) is a multichannel transmit/receive, controller/peripheral synchronous serial bus.

Key features of the MCSPI include:

- Full-duplex synchronous serial interface
- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of MCSPI word lengths, ranging from 4 to 32 bits
- Up to four controller channels, or single channel in peripheral mode
- Controller multichannel mode:
    - Full duplex/half duplex
    - Transmit-only/receive-only/transmit-and-receive modes
    - Flexible input/output (I/O) port controls per channel
    - Programmable clock granularity
    - MCSPI configuration per channel. This means, clock definition, polarity enabling and word width
- Single interrupt line for multiple interrupt source events
- Enable the addition of a programmable start-bit for MCSPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable shift operations (1-32 bits)
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel.

NOTE

MCSPI has one or more signals which can be exported from more than one pin.
However, only specific pin combinations known as IOSETs are valid.
These are defined in TI's SysConfig-PinMux Tool.
The below tables present the valid IOSETs

Note: For interacting multiple peripherals on same SPI bus, one can define any GPIO to be used as chip select.

8.13.1 MCSPI0 Signals

Note: MCSPI0 interface is used by internal Resistive Touch Controller.
MCSPI0 interface can be used externally only in SOMs without "TP" assembly option.

Table 56: MCSPI0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
189	no TP	SPI0_CLK	0	Available in SOM without TP	A14
191	no TP	SPI0_CS0	0	Available in SOM without TP	A13
68		SPI0_CS1	0		C13
187	no TP	SPI0_D0	0	Available in SOM without TP	B13
193	no TP	SPI0_D1	0	Available in SOM without TP	B14

8.13.2 MCSPI1 Signals

Table 57: MCSPI1 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
75		SPI1_CLK	1	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J25
79		SPI1_CS0	1	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J23
70		SPI1_D0	1	Pin referenced to 1.8V in SOM with "OSPI" configuration;	H25
77		SPI1_D1	1	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J22

8.13.3 MCSPI2 Signals

Table 58: MCSPI2 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
72		SPI2_CS3	1		D20
17		SPI2_CS2	1		B18
117		SPI2_CS1	1		B20
39		SPI2_CS0	1		E19
43		SPI2_CLK	1		A20
45		SPI2_D0	1		B19
41		SPI2_D1	1		A19

Table 59: MCSPI2 IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		SPI2_CS3	2		A18
87		SPI2_CS2	2		A16
92		SPI2_CS1	3		B17
88		SPI2_CS0	9		B16
90		SPI2_CLK	3		A17
83		SPI2_D0	2	Used as debug UART on Variscite base board	D14
85		SPI2_D1	2	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	E14

8.13.4 MCU SPI0 Signals

Table 60: MCU SPI0 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
157		MCU_SPI0_CS3	2		D6
145		MCU_SPI0_CS2	2		B4
153		MCU_SPI0_CS1	0		B8
150		MCU_SPI0_CLK	0		A7
151		MCU_SPI0_D0	0		D9
152		MCU_SPI0_D1	0		C9

Table 61: MCU SPI0 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
157		MCU_SPI0_CS3	2		D6
154		MCU_SPI0_CS2	2		D4
153		MCU_SPI0_CS1	0		B8
150		MCU_SPI0_CLK	0		A7
151		MCU_SPI0_D0	0		D9

Pin#	Assy	Pin Function	Alt#	Notes	Ball
152		MCU_SPI0_D1	0		C9

8.13.5 MCU SPI1 Signals

Table 62: MCU SPI1 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
155		MCU_SPI1_CS3	2		B3
154		MCU_SPI1_CS2	3		D4
156		MCU_SPI1_CS1	3		E5
142		MCU_SPI1_CS0	3		C6
143		MCU_SPI1_CLK	3		A4
58		MCU_SPI1_D0	3		A6
93		MCU_SPI1_D1	3		B6

Table 63: MCU SPI1 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
155		MCU_SPI1_CS3	2		B3
147		MCU_SPI1_CS2	2		C5
156		MCU_SPI1_CS1	3		E5
142		MCU_SPI1_CS0	3		C6
143		MCU_SPI1_CLK	3		A4
58		MCU_SPI1_D0	3		A6
93		MCU_SPI1_D1	3		B6

Table 64: MCU SPI1 IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
155		MCU_SPI1_CS3	2		B3
147		MCU_SPI1_CS2	2		C5
142		MCU_SPI1_CS0	3		C6
154		MCU_SPI1_CLK	4		D4
58		MCU_SPI1_D0	3		A6
93		MCU_SPI1_D1	3		B6

8.14 OSPI - Octal Serial Peripheral Interface

The VAR-SOM-AM62 exposes the OSPI module which allows single, dual, quad or octal read and write access to external flash devices.

The module contains the following features:

- Support for single, dual, quad (QSPI mode) or octal I/O instructions
- Supports dual Quad-SPI mode for fast boot applications.
- Memory mapped 'direct' mode of operation for performing flash data transfers and executing code from flash memory.
- Software triggered 'indirect' mode of operation for performing low latency and non-processor intensive flash data transfers.
- Local SRAM of configurable size to reduce advanced high-performance bus overhead and buffer flash data during indirect transfers.
- Set of software advanced peripheral bus accessible flash control registers to perform any flash command, including data transfers up to 8-bytes at a time.
- Additional addressable memory bank to accommodate more than 8-bytes at a time.
- Support for XIP, sometimes referred to as continuous mode.
- Support for DDR Mode and DTR protocol (including Octal DDR protocol with DQS for Octal-SPI devices)
- Programmable device sizes.
- Programmable write protected regions to block system writes from taking effect.
- Programmable delays between transactions.
- Legacy mode allowing software direct access to low level transmit and receive FIFOs, bypassing the higher layer processes.
- An independent reference clock to decouple bus clock from SPI clock – allows slow system clocks.
- Programmable baud rate generator to generate OSPI clocks.
- Features included to improve high speed read data capture mechanism.
- Option to use adapted clocks or DQS to further improve read data capturing.
- Programmable interrupt generation.
- Up to four external device selects - OSPI and QSPI devices can be mixed
- Programmable data decoder, enables continuous addressing mode for each of the connected devices and auto-detection of boundaries between devices.
- Supports BOOT mode.
- Bidirectional CRC on Multiple-SPI interface.
- Handling ECC errors for flash devices with embedded correction engine.
- Full integration with PHY module dedicated to more flexible and power efficient transfers.
- Supports RESET_OUT[1-0] and ECC_FAIL pins for external flash devices where ECC is checked on the flash.

Note: OSPI signals are available on SOM with "OSPI" assembly option.
OSPI signals are referenced to 1.8v.

8.14.1 OSPI Signals

Table 65: OSPI Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	OSPI	OSPI0_CLK	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	H24
102	OSPI	OSPI0_CSn0	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	F23
47	OSPI	OSPI0_CSn3	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	E24
76	OSPI	OSPI0_D0	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	E25
35	OSPI	OSPI0_D1	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	G24
100	OSPI	OSPI0_D2	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	F25
59	OSPI	OSPI0_D3	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	F24
79		OSPI0_D4	0	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J23
75		OSPI0_D5	0	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J25
70		OSPI0_D6	0	Pin referenced to 1.8V in SOM with "OSPI" configuration;	H25
77		OSPI0_D7	0	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J22
36	OSPI	OSPI0_DQS	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	J24
47	OSPI	OSPI0_ECC_FAIL	2	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	E24
33	OSPI	OSPI0_LBCLKO	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	G25
47	OSPI	OSPI0_RESET_OUT0	1	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	E24

8.15 General-Purpose Memory Controller (GPMC)

The VAR-SOM-AM62 exposes the General-Purpose Memory Controller (GPMC) interface which can be used for interfacing with 8-bit/16-bit NAND flash devices.

Note: GPMC signals are available on SOM with “GPMC” assembly option.

8.15.1 GPMC Signals

Table 66: GPMC Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	GPMC	GPMC0_AD0	0	Available in SOM with "GPMC” configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	M25
33	GPMC	GPMC0_AD1	0	Available in SOM with "GPMC” configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N23
21		GPMC0_AD10	0	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T25
26		GPMC0_AD11	0	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R21
24		GPMC0_AD12	0	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T22
25		GPMC0_AD13	0	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T24
23		GPMC0_AD14	0	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U25
22		GPMC0_AD15	0	BOOTMODE15 pin, 100K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U24
76	GPMC	GPMC0_AD2	0	Available in SOM with "GPMC” configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N24
173		GPMC0_AD3	0	BOOTMODE03 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N25
84		GPMC0_AD4	0	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P24
48		GPMC0_AD5	0	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P22
86		GPMC0_AD6	0	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P21
40		GPMC0_AD7	0	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R23
115		GPMC0_AD8	0	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R24
171		GPMC0_AD9	0	BOOTMODE09 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R25
198	no AC	GPMC0_ADVn_ALE	0	Available in SOM without "AC” configuration	L23
200	no AC	GPMC0_BE0n_CLE	0	Available in SOM without "AC” configuration	M24
47	GPMC	GPMC0_BE1n	0	Available in SOM with "GPMC” configuration;	N20
59	GPMC	GPMC0_CLK	0	Available in SOM with "GPMC” configuration;	P25
100	GPMC	GPMC0_CSn0	0	Available in SOM with "GPMC” configuration;	M21
102	GPMC	GPMC0_CSn1	0	Available in SOM with "GPMC” configuration;	L21
174		GPMC0_CSn2	0	Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	K22

Pin#	Assy	Pin Function	Alt#	Notes	Ball
				In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	
176		GPMC0_CSn3	0	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	K24
35	GPMC	GPMC0_DIR	0	Available in SOM with "GPMC” configuration;	M22
59	GPMC	GPMC0_FCLK_MUX	3	Available in SOM with "GPMC” configuration;	P25
36	GPMC	GPMC0_OEn_REn	0	Available in SOM with "GPMC” configuration;	L24
199	no AC	GPMC0_WAIT0	0	Available in SOM without "AC” configuration	U23
175		GPMC0_WAIT1	0		V25
196	no AC & GPMC	GPMC0_WEn	0	Available in SOM without "AC” and with "GPMC" configuration	L25
197	no AC & GPMC	GPMC0_WPn	0	Available in SOM without "AC” and with "GPMC" configuration	K25

8.16 eCAP

The AM62x provides up to 3 Enhanced Pulse Width Modulation (EPWM) Modules.

The Enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The ECAP module includes the following features:

- 32-bit time base counter
- 4 × 32 bits event time-stamp capture registers (through)
- 4-stage sequencer (Mod4 counter), synchronized to external events (ECAPx pin edges)
- Independent edge polarity (rising / falling edge) selection for all 4 sequenced time-stamp capture events
- Input capture signal pre-scaling (from 1 to 16)
- One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Interrupt capabilities on any of the 4 capture events
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output

8.16.1 eCAP0 Signals

Table 67: eCAP0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		ECAP0_IN_APWM_OUT	8		A18
68		ECAP0_IN_APWM_OUT	3		C13

8.16.2 eCAP1 Signals

Table 68: eCAP1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
17		ECAP1_IN_APWM_OUT	2		B18
45		ECAP1_IN_APWM_OUT	5		B19
63		ECAP1_IN_APWM_OUT	4	Bank voltage set on SOM 1.8V/3.3V	B21
83		ECAP1_IN_APWM_OUT	1	Used as debug UART on Variscite base board	D14
88		ECAP1_IN_APWM_OUT	8		B16

8.16.3 eCAP2 Signals

Table 69: eCAP2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
41		ECAP2_IN_APWM_OUT	5		A19
62		ECAP2_IN_APWM_OUT	4	Bank voltage set on SOM 1.8V/3.3V	A22
85		ECAP2_IN_APWM_OUT	1	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	E14
87		ECAP2_IN_APWM_OUT	8		A16
117		ECAP2_IN_APWM_OUT	2		B20

8.17 ePWM

The AM62xx provides up to 3 Enhanced Pulse Width Modulation (EPWM) Modules.

Each EPWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Allows events to trigger both CPU interrupts and ADC start of conversions
- Programmable event prescaling minimizes CPU overhead on interrupts
- PWM chopping by a high-frequency carrier signal, useful for pulse transformer gate drives

The main signals used by the EPWM module are:

- **PWM output signals (EPWMxA and EPWMxB)**
  The PWM output signals are available external to the device through the GPIO peripheral.
- **Trip-zone signals (TZ0 to TZ5)**
  These input signals alert the EPWM module of an external fault condition. Each module on a device can be configured to either use or ignore any of the trip-zone signals. The trip-zone signal can be configured as an asynchronous input through the GPIO peripheral.
- **Time-base synchronization input (EPWMxSYNCI) and output (EPWMxSYNCO) signals**
  The synchronization signals daisy chain the EPWM modules together. Each module can be configured to either use or ignore its synchronization input. *For more information see, Daisy-Chain Connectivity between EPWM Modules (*TRM*).*
- **ADC start-of-conversion signals (EPWMxSOCA and EPWMxSOCB)**
  Each EPWM module has two ADC start of conversion signals (one for each sequencer). Any EPWM module can trigger a start of conversion for either sequencer. Which event triggers the start of conversion configured in the Event-Trigger submodule of the EPWM module.

8.17.1 ePWM Signals

Table 70: ePWM Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
88		EHRPWM_SOCA	6		B16
87		EHRPWM_SOCB	6		A16
193	no TP	EHRPWM_TZn_IN0	2	Available in SOM without TP	B14
44		EHRPWM_TZn_IN3	9		C15
46		EHRPWM_TZn_IN4	9		E15
68		EHRPWM_TZn_IN5	9		C13

8.17.2 ePWM0 Signals

Table 71: ePWM0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
39		EHRPWM0_A	6		E19
191	no TP	EHRPWM0_A	2	Available in SOM without TP	A13
43		EHRPWM0_B	6		A20
68		EHRPWM0_B	2		C13
92		EHRPWM0_SYNCI	4		B17
90		EHRPWM0_SYNCO	4		A17

8.17.3 ePWM1 Signals

Table 72: ePWM1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
17		EHRPWM1_A	6		B18
189	no TP	EHRPWM1_A	2	Available in SOM without TP	A14
69		EHRPWM1_B	6		E18
187	no TP	EHRPWM1_B	2	Available in SOM without TP	B13

8.17.4 ePWM2 Signals

Table 73: ePWM2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
83		EHRPWM2_A	3	Used as debug UART on Variscite base board	D14
92		EHRPWM2_A	8		B17
85		EHRPWM2_B	3	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	E14
90		EHRPWM2_B	8		A17

8.18 eQEP

The VAR-SOM-AM62 exposes the Enhanced Quadrature Encoder Pulse (EQEP) module.
The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns, as shown in Figure 12-1800. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution).
As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

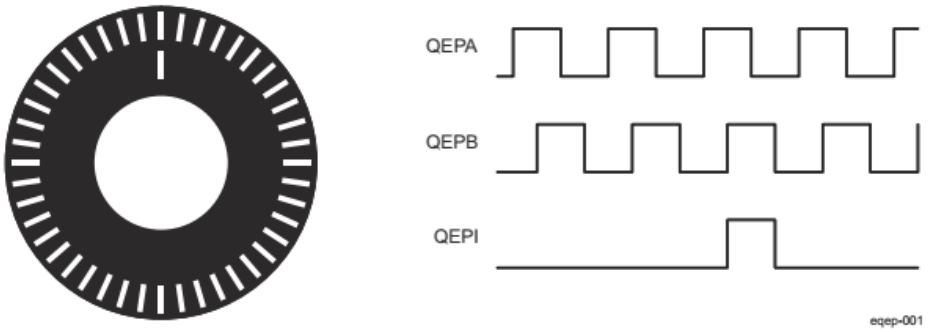


Figure 12-1800. Optical Encoder Disk

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other.
These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vise versa.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 kHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

The EQEP module includes the following features:

- Input synchronization
- Three stage/six stage digital noise filter
- Quadrature decoder unit
- Position counter and control unit for position measurement
- Quadrature edge capture unit for low-speed measurement
- Unit time base for speed and frequency measurement
- Watchdog timer for detecting stalls

- EQEP inputs (A/B/INDEX and STROBE) are available at chip level
- EQEP phase error output is also available. The status of the phase error can be observed by software through the register in the CTRL_MMR0 module.
- Counting modes:
  - Quadrature
  - Clockwise / Counter Clockwise
  - Count / Direction
- Start of Convert input for on-chip Strobe
- EQEP internal strobe (EQEP Strobe input is logically ORed with EQEP A and B inputs) may be used to:
  - Initialize the Position Counter with a non-zero value (for example, due to a limit switch input becoming active)
  - Snapshot the Position Counter into the register
  - Gate the EQEP Index input preventing it from resetting the Position Counter

8.18.1 eQEP0 Signals

Table 74: eQEP0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
45		EQEP0_A	8		B19
41		EQEP0_B	8		A19
69		EQEP0_I	8		E18
17		EQEP0_S	8		B18

8.18.2 eQEP1 Signals

Table 75: eQEP1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
117		EQEP1_A	8		B20
72		EQEP1_B	8		D20
43		EQEP1_I	8		A20
39		EQEP1_S	8		E19

8.18.3 eQEP2 Signals

Table 76: eQEP2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
71		EQEP2_A	8	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AC21
88		EQEP2_A	5		B16
54		EQEP2_B	8	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AE22
87		EQEP2_B	5		A16
44		EQEP2_I	5		C15
56		EQEP2_I	8	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AD21
175		EQEP2_I	8		V25

Pin#	Assy	Pin Function	Alt#	Notes	Ball
35	GPMC	EQEP2_S	8	Available in SOM with "GPMC" configuration;	M22
46		EQEP2_S	5		E15
55		EQEP2_S	8	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AC20

8.19 Timer

The VAR-SOM-AM62 exposes the Timer interface to its connector.

All timers include specific functions to generate accurate tick interrupts to the operating system. Each timer can be clocked from several different independent clocks. The selection of clock source is made from registers in the MCU_CTRL_MMR0/CTRL_MMR0.

Key features of the Timer controllers:

- Target interface supports:
  - 32-bit data bus width
  - 32-bit access supported
  - 10-bit address bus width
  - Write nonposted transaction mode supported
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Compare and capture modes
- Autoreload mode
- Start/stop mode
- Programmable divider clock source (2n, where n = [0-8])
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- On-the-fly read/write register (while counting)
- Generates a 1-ms tick clock with a 32.768 kHz functional clock sourced from the LFOSC

8.19.1.1 MAIN Timer Signals

Table 77: MAIN Timer Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
65		TIMER_IO0	2	Bank voltage set on SOM 1.8V/3.3V	D22
92		TIMER_IO0	2		B17
61		TIMER_IO1	2	Bank voltage set on SOM 1.8V/3.3V	C21
90		TIMER_IO1	2		A17
44		TIMER_IO2	2		C15
63		TIMER_IO2	2	Bank voltage set on SOM 1.8V/3.3V	B21
46		TIMER_IO3	2		E15
62		TIMER_IO3	2	Bank voltage set on SOM 1.8V/3.3V	A22
29		TIMER_IO4	4		A18
60		TIMER_IO4	2	Bank voltage set on SOM 1.8V/3.3V	B22
64		TIMER_IO5	2	Bank voltage set on SOM 1.8V/3.3V	A21
87		TIMER_IO5	3		A16
80		TIMER_IO6	2	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D17
124		TIMER_IO7	2		C17

8.19.1.2 MCU Timer Signals

Table 78: MCU Timer Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
58		MCU_TIMER_IO0	1		A6
155		MCU_TIMER_IO0	1		B3
93		MCU_TIMER_IO1	1		B6
153		MCU_TIMER_IO1	4		B8
156		MCU_TIMER_IO2	1		E5
154		MCU_TIMER_IO3	1		D4

8.19.1.3 WKUP Timer Signals

Table 79: WKUP Timer Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
142		WKUP_TIMER_IO0	1		C6
157		WKUP_TIMER_IO0	1		D6
143		WKUP_TIMER_IO1	1		A4

8.20 PRUSS

The Programmable Real-Time Unit Subsystem (PRUSS) consists of:

- Two 32-bit load/store RISC CPU cores — Programmable Real-Time Units (PRU0 and PRU1)
- Data RAMs per PRU core (DRAM)
- Instruction RAMs per PRU core (IRAM)
- Shared RAM (SRAM)
- Peripheral modules: UART0, ECAP0, IEP0, MDIO
- Interrupt Controller (INTC) per core

The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

The PRU cores are programmed with a small, deterministic instruction set. Each PRU can operate independently or in coordination with each other and can also work in coordination with the device-level host CPU. This interaction between processors is determined by the nature of the firmware loaded into the PRU's instruction memory.

The PRUSS subsystem includes the following main features:

- Two 32-bit load/store RISC CPU cores — Programmable Real-Time Units (PRU0 and PRU1), each with:
    - 20 Enhanced General-Purpose Inputs (EGPI) and 20 Enhanced General-Purpose Outputs (EGPO)
    - Asynchronous capture [Serial Capture Unit (SCU)] with EnDat 2.2 protocol and Sigma-Delta demodulation support
    - 12KB program memory per PRU (PRU0_IRAM and PRU1_IRAM) with ECC
    - MAC (Multiplier with optional Accumulation)
    - CRC16/CRC32 hardware accelerator
    - RX XFR2VBUS
- Scratchpad Memory (SPAD) with 3 banks of 30 × 32-bit registers:
    - 3 banks for the PRU0 and PRU1 cores
- 32 KB Shared general purpose memory RAM with ECC (Data RAM2), shared between PRU0 and PRU1
- Two 8 KB (shared) Data Memories with ECC (Data RAM0 and Data RAM1)
- 36-bit VBUSM Controller Port:
    - Optional address translation for all transactions to External Host
- 16 Software Events generated by 2 PRUs
- One Enhanced Capture Module (ECAP0)
- Interrupt Controller (INTC)
    - Up to 32 internal events, generated by modules, internal to the PRUSS
    - Up to 32 external events, generated by the system
    - Supports up to 10 interrupt channels
    - Generation of 8 Host interrupts:
- 8 Host interrupts, exported from the PRUSS for signaling the Arm interrupt controllers (pulse and level provided)
    - Each system event can be enabled and disabled

  - Each host event can be enabled and disabled
  - Hardware prioritization of events
- One 32-bit VBUSP target port for memory mapped register and internal memories access
- Flexible power management support
- Integrated 32-bit Interconnect

NOTE

PRUSS GPI/GPO have one or more signals which can be exported from more than one pin.
However, only specific pin combinations known as IOSETs are valid.
These are defined in TI's SysConfig-PinMux Tool.
The below tables present the valid IOSETs

8.20.1 PRUSS0 Signals

Table 80: PRUSS0 ECAP Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
35	GPMC	PR0_ECAP0_IN_APWM_OUT	1	Available in SOM with "GPMC" configuration;	M22
56		PR0_ECAP0_IN_APWM_OUT	5	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD21
69		PR0_ECAP0_IN_APWM_OUT	1		E18
57		PR0_ECAP0_SYNC_IN	5	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD23
191	no TP	PR0_ECAP0_SYNC_IN	6	Available in SOM without TP	A13
55		PR0_ECAP0_SYNC_OUT	5	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AC20

Table 81: PRUSS0 EDIO Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
45		PR0_IEP0_EDIO_DATA_IN_OUT28	4		B19
41		PR0_IEP0_EDIO_DATA_IN_OUT29	4		A19
88		PR0_IEP0_EDIO_DATA_IN_OUT30	1		B16
87		PR0_IEP0_EDIO_DATA_IN_OUT31	1		A16

Table 82: PRUSS0 UART Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
16	no EC	PR0_UART0_CTSn	2	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD17
55		PR0_UART0_CTSn	6	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AC20
10	no EC	PR0_UART0_RTSn	2	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AB16
122		PR0_UART0_RTSn	6	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE23
5	no EC	PR0_UART0_RXD	2	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE18
17		PR0_UART0_RXD	5		B18
44		PR0_UART0_RXD	6		C15
45		PR0_UART0_RXD	6		B19
71		PR0_UART0_RXD	5	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AC21
3	no EC	PR0_UART0_TXD	2	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD18
41		PR0_UART0_TXD	6		A19
46		PR0_UART0_TXD	6		E15
54		PR0_UART0_TXD	5	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE22
69		PR0_UART0_TXD	5		E18

Table 83: PRUSS0 GPI/GPO IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	GPMC	PR0_PRU0_GPO0	4	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	M25
33	GPMC	PR0_PRU0_GPO1	4	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N23
76	GPMC	PR0_PRU0_GPO2	4	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N24
173		PR0_PRU0_GPO3	4	BOOTMODE03 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N25
84		PR0_PRU0_GPO4	4	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P24
48		PR0_PRU0_GPO5	4	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P22
86		PR0_PRU0_GPO6	4	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P21
40		PR0_PRU0_GPO7	4	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R23
59	GPMC	PR0_PRU0_GPO8	4	Available in SOM with "GPMC" configuration;	P25
198	no AC	PR0_PRU0_GPO9	4	Available in SOM without "AC" configuration	L23
36	GPMC	PR0_PRU0_GPO10	4	Available in SOM with "GPMC" configuration;	L24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
18	no AC & no GPMC	PR0_PRU0_GPO11	4	Available in SOM without "AC" and without "GPMC" configuration	L25
200	no AC	PR0_PRU0_GPO12	4	Available in SOM without "AC" configuration	M24
47	GPMC	PR0_PRU0_GPO13	4	Available in SOM with "GPMC" configuration;	N20
199	no AC	PR0_PRU0_GPO14	4	Available in SOM without "AC" configuration	U23
20	no AC & no GPMC	PR0_PRU0_GPO15	4	Available in SOM without "AC" and without "GPMC" configuration	K25
35	GPMC	PR0_PRU0_GPO16	4	Available in SOM with "GPMC" configuration;	M22
100	GPMC	PR0_PRU0_GPO17	4	Available in SOM with "GPMC" configuration;	M21
102	GPMC	PR0_PRU0_GPO18	4	Available in SOM with "GPMC" configuration;	L21
174		PR0_PRU0_GPO19	4	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K22
31	GPMC	PR0_PRU0_GPI0	5	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	M25
33	GPMC	PR0_PRU0_GPI1	5	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N23
76	GPMC	PR0_PRU0_GPI2	5	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N24
173		PR0_PRU0_GPI3	5	BOOTMODE03 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N25
84		PR0_PRU0_GPI4	5	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P24
48		PR0_PRU0_GPI5	5	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P22
86		PR0_PRU0_GPI6	5	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P21
40		PR0_PRU0_GPI7	5	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R23
59	GPMC	PR0_PRU0_GPI8	5	Available in SOM with "GPMC" configuration;	P25
198	no AC	PR0_PRU0_GPI9	5	Available in SOM without "AC" configuration	L23
36	GPMC	PR0_PRU0_GPI10	5	Available in SOM with "GPMC" configuration;	L24
18	no AC & no GPMC	PR0_PRU0_GPI11	5	Available in SOM without "AC" and without "GPMC" configuration	L25
200	no AC	PR0_PRU0_GPI12	5	Available in SOM without "AC" configuration	M24
47	GPMC	PR0_PRU0_GPI13	5	Available in SOM with "GPMC" configuration;	N20
199	no AC	PR0_PRU0_GPI14	5	Available in SOM without "AC" configuration	U23
20	no AC & no GPMC	PR0_PRU0_GPI15	5	Available in SOM without "AC" and without "GPMC" configuration	K25
35	GPMC	PR0_PRU0_GPI16	5	Available in SOM with "GPMC" configuration;	M22
100	GPMC	PR0_PRU0_GPI17	5	Available in SOM with "GPMC" configuration;	M21
102	GPMC	PR0_PRU0_GPI18	5	Available in SOM with "GPMC" configuration;	L21

Pin#	Assy	Pin Function	Alt#	Notes	Ball
174		PR0_PRU0_GPI19	5	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	K22

Table 84: PRUSS0 GPI/GPO IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
120		PR0_PRU0_GPO0	3	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AD22
57		PR0_PRU0_GPO1	3	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AD23
122		PR0_PRU0_GPO2	3	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AE23
81		PR0_PRU0_GPO3	3	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AB20
71		PR0_PRU0_GPO4	3	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AC21
54		PR0_PRU0_GPO16	3	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AE22
120		PR0_PRU0_GPI0	4	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AD22
57		PR0_PRU0_GPI1	4	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AD23
122		PR0_PRU0_GPI2	4	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AE23
81		PR0_PRU0_GPI3	4	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AB20
71		PR0_PRU0_GPI4	4	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AC21
54		PR0_PRU0_GPI16	4	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AE22

Table 85: PRUSS0 GPI/GPO IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
50		PR0_PRU0_GPO2	5	Used internally with "WBD", Function can be released if BT Function disabled	AB25
51		PR0_PRU0_GPO3	5	Used internally with "WBD", Function can be released if BT Function disabled	AA24
53		PR0_PRU0_GPO14	5	Used internally with "WBD", Function can be released if BT Function disabled	Y23
52		PR0_PRU0_GPO15	5	Used internally with "WBD", Function can be released if BT Function disabled	AA25
50		PR0_PRU0_GPI2	6	Used internally with "WBD", Function can be released if BT Function disabled	AB25
51		PR0_PRU0_GPI3	6	Used internally with "WBD", Function can be released if BT Function disabled	AA24
53		PR0_PRU0_GPI14	6	Used internally with "WBD", Function can be released if BT Function disabled	Y23
52		PR0_PRU0_GPI15	6	Used internally with "WBD", Function can be released if BT Function disabled	AA25

Table 86: PRUSS0 GPI/GPO IOSet_4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
24		PR0_PRU0_GPO0	4	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T22
25		PR0_PRU0_GPO1	4	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T24
23		PR0_PRU0_GPO2	4	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U25
22		PR0_PRU0_GPO3	4	BOOTMODE15 pin, 100K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U24
24		PR0_PRU0_GPI0	5	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T22
25		PR0_PRU0_GPI1	5	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T24
23		PR0_PRU0_GPI2	5	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U25
22		PR0_PRU0_GPI3	5	BOOTMODE15 pin, 100K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U24

8.20.2 PRUSS1 Signals

Table 87: PRUSS1 GPI/GPO IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	GPMC	PR0_PRU1_GPO8	1	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	M25
33	GPMC	PR0_PRU1_GPO9	1	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N23
76	GPMC	PR0_PRU1_GPO10	1	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N24
173		PR0_PRU1_GPO11	1	BOOTMODE03 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N25
84		PR0_PRU1_GPO12	1	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P24
48		PR0_PRU1_GPO13	1	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P22
86		PR0_PRU1_GPO14	1	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P21
40		PR0_PRU1_GPO15	1	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R23
102	GPMC	PR0_PRU1_GPO16	1	Available in SOM with "GPMC" configuration;	L21
31	GPMC	PR0_PRU1_GPI8	2	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	M25
33	GPMC	PR0_PRU1_GPI9	2	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N23
76	GPMC	PR0_PRU1_GPI10	2	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N24
173		PR0_PRU1_GPI11	2	BOOTMODE03 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N25
84		PR0_PRU1_GPI12	2	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P24
48		PR0_PRU1_GPI13	2	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P22

Pin#	Assy	Pin Function	Alt#	Notes	Ball
86		PR0_PRU1_GPI14	2	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P21
40		PR0_PRU1_GPI15	2	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R23
102	GPMC	PR0_PRU1_GPI16	2	Available in SOM with "GPMC" configuration;	L21

Table 88: PRUSS1 GPI/GPO IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
113		PR0_PRU1_GPO0	3	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AA19
96		PR0_PRU1_GPO1	3	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE21
73		PR0_PRU1_GPO2	3	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	Y18
177		PR0_PRU1_GPO3	3	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AA18
56		PR0_PRU1_GPO4	3	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD21
55		PR0_PRU1_GPO16	3	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AC20
113		PR0_PRU1_GPI0	4	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AA19
96		PR0_PRU1_GPI1	4	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE21
73		PR0_PRU1_GPI2	4	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	Y18
177		PR0_PRU1_GPI3	4	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AA18
56		PR0_PRU1_GPI4	4	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD21
55		PR0_PRU1_GPI16	4	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AC20

Table 89: PRUSS1 GPI/GPO IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
53		PR0_PRU1_GPO6	2	Used internally with "WBD", Function can be released if BT Function disabled	Y23
52		PR0_PRU1_GPO7	2	Used internally with "WBD", Function can be released if BT Function disabled	AA25
50		PR0_PRU1_GPO11	2	Used internally with "WBD", Function can be released if BT Function disabled	AB25
51		PR0_PRU1_GPO12	2	Used internally with "WBD", Function can be released if BT Function disabled	AA24
53		PR0_PRU1_GPI6	3	Used internally with "WBD", Function can be released if BT Function disabled	Y23
52		PR0_PRU1_GPI7	3	Used internally with "WBD", Function can be released if BT Function disabled	AA25
50		PR0_PRU1_GPI11	3	Used internally with "WBD", Function can be released if BT Function disabled	AB25
51		PR0_PRU1_GPI12	3	Used internally with "WBD", Function can be released if BT Function disabled	AA24

Table 90: PRUSS1 GPI/GPO IOSet_4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
115		PR0_PRU1_GPO0	4	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R24
171		PR0_PRU1_GPO1	4	BOOTMODE09 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R25
21		PR0_PRU1_GPO2	4	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T25
26		PR0_PRU1_GPO3	4	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R21
115		PR0_PRU1_GPI0	5	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R24
171		PR0_PRU1_GPI1	5	BOOTMODE09 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R25
21		PR0_PRU1_GPI2	5	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T25
26		PR0_PRU1_GPI3	5	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R21

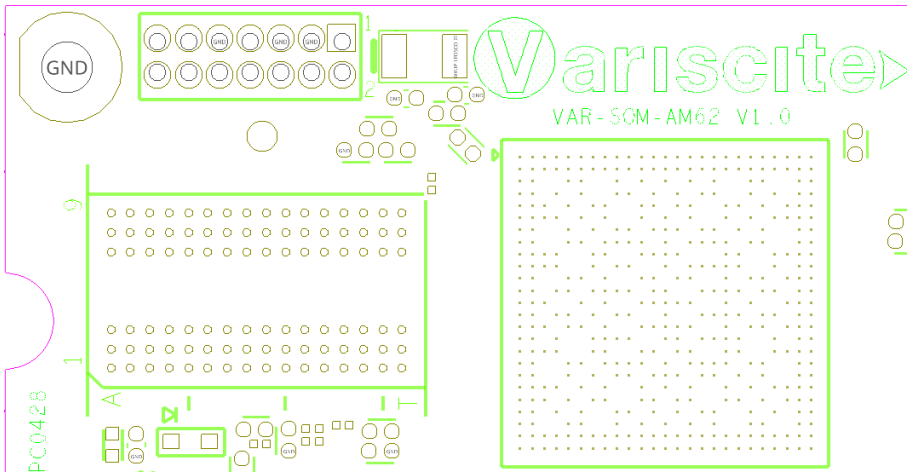
8.21 On chip Debug JTAG

AM62x On-Chip Debug features are supported through three device interfaces:

- JTAG: IEEE 1149.1 compliant interface that provides access to Boundary Scan and acts as the primary interface for off-chip access to On-Chip debug resources.
- Trigger and Debug Boot Mode: Multi-functional interface that supports product level cross-triggering and debug-related boot modes
- Trace Port: Arm TPIU compliant Trace Port interface is used to facilitate export of trace

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support.
The following document is a good reference for guidelines: Emulation and Trace Headers.
More information can also be found here: XDS Target Connection Guide.

VAR-SOM-AM62 exposes JTAG signals on a 14-pin header (not assembled by default) on the SOM top left side.



8.21.1 JTAG Signals

Table 91: JTAG signals on 14-pin Header Connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
1		VDD_3V3		JTAG reference voltage (3.3v)	
2		TMS		Test Mode Select. Controls the transitions of the test interface state machine. Internal signal pulled up to SOM_PGOOD using 10K resistor.	B11
3		GND		Digital Ground	
4		TCK		Test Clock. Controls the timing of the test interface independently from any system clocks. TCK is pulsed by the equipment controlling the test and not by the tested device. Internal signal pulled up to SOM_PGOOD using 10K resistor.	A10
5		GND		Digital Ground	
6		TDO		Test Data Output. Used to serially output the data from the JTAG registers to the equipment controlling the test.	D12
7					
8		TDI		Test Data Input. Supplies the data to the JTAG registers. Internal signal pulled up to SOM_PGOOD using 10K resistor.	A11
9		GND		Digital Ground	
10		JTAG_EMU_RSTn		JTAG System reset	
11		TRST#		Test Reset. Initializes and disables the test interface. Internal signal pulled down to GND using 4.7K resistor.	B10
12		EMU0		Channel 0 trigger or boot mode select. Internal signal pulled up to SOM_PGOOD using 10K resistor.	E12
13					
14		EMU1		Channel 1 trigger or boot mode select. Internal signal pulled up to SOM_PGOOD using 10K resistor.	C11

8.21.2 TRACE Signals

Table 92: TRACE signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	GPMC	TRC_CLK	6	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	M25
33	GPMC	TRC_CTL	6	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N23
76	GPMC	TRC_DATA0	6	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N24
173		TRC_DATA1	6	BOOTMODE03 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N25

Pin#	Assy	Pin Function	Alt#	Notes	Ball
200	no AC	TRC_DATA10	6	Available in SOM without "AC" configuration	M24
47	GPMC	TRC_DATA11	6	Available in SOM with "GPMC" configuration;	N20
199	no AC	TRC_DATA12	6	Available in SOM without "AC" configuration	U23
20	no AC & no GPMC	TRC_DATA13	6	Available in SOM without "AC" and without "GPMC" configuration	K25
197	no AC & GPMC	TRC_DATA13	6	Available in SOM without "AC" and with "GPMC" configuration	K25
35	GPMC	TRC_DATA14	6	Available in SOM with "GPMC" configuration;	M22
100	GPMC	TRC_DATA15	6	Available in SOM with "GPMC" configuration;	M21
102	GPMC	TRC_DATA16	6	Available in SOM with "GPMC" configuration;	L21
174		TRC_DATA17	6	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K22
176		TRC_DATA18	6	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K24
22		TRC_DATA19	6	BOOTMODE15 pin, 100K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U24
84		TRC_DATA2	6	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P24
23		TRC_DATA20	6	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U25
25		TRC_DATA21	6	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T24
24		TRC_DATA22	6	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T22
26		TRC_DATA23	6	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R21
48		TRC_DATA3	6	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P22
86		TRC_DATA4	6	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P21
40		TRC_DATA5	6	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R23
59	GPMC	TRC_DATA6	6	Available in SOM with "GPMC" configuration;	P25
198	no AC	TRC_DATA7	6	Available in SOM without "AC" configuration	L23
36	GPMC	TRC_DATA8	6	Available in SOM with "GPMC" configuration;	L24
18	no AC & no GPMC	TRC_DATA9	6	Available in SOM without "AC" and without "GPMC" configuration	L25
196	no AC & GPMC	TRC_DATA9	6	Available in SOM without "AC" and with "GPMC" configuration	L25

8.22 General Purpose IO

The VAR-SOM-AM62 provides IO pins which can be used as GPIOs.

8.22.1 GPIO Signals

Table 93: GPIO Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	OSPI	GPIO0_0	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	H24
33	OSPI	GPIO0_1	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	G25
77		GPIO0_10	7	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J22
102	OSPI	GPIO0_11	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	F23
47	OSPI	GPIO0_14	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	E24
31	GPMC	GPIO0_15	7	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	M25
33	GPMC	GPIO0_16	7	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N23
76	GPMC	GPIO0_17	7	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N24
173		GPIO0_18	7	BOOTMODE03 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N25
84		GPIO0_19	7	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P24
36	OSPI	GPIO0_2	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	J24
48		GPIO0_20	7	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P22
86		GPIO0_21	7	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P21
40		GPIO0_22	7	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R23
115		GPIO0_23	7	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R24
171		GPIO0_24	7	BOOTMODE09 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R25
21		GPIO0_25	7	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T25
26		GPIO0_26	7	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R21
24		GPIO0_27	7	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T22
25		GPIO0_28	7	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T24
23		GPIO0_29	7	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U25
76	OSPI	GPIO0_3	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	E25
22		GPIO0_30	7	BOOTMODE15 pin, 100K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
59	GPMC	GPIO0_31	7	Available in SOM with "GPMC" configuration;	P25
198	no AC	GPIO0_32	7	Available in SOM without "AC" configuration	L23
36	GPMC	GPIO0_33	7	Available in SOM with "GPMC" configuration;	L24
18	no AC & no GPMC	GPIO0_34	7	Available in SOM without "AC" and without "GPMC" configuration	L25
196	no AC & GPMC	GPIO0_34	7	Available in SOM without "AC" and with "GPMC" configuration	L25
200	no AC	GPIO0_35	7	Available in SOM without "AC" configuration	M24
47	GPMC	GPIO0_36	7	Available in SOM with "GPMC" configuration;	N20
199	no AC	GPIO0_37	7	Available in SOM without "AC" configuration	U23
175		GPIO0_38	7		V25
20	no AC & no GPMC	GPIO0_39	7	Available in SOM without "AC" and without "GPMC" configuration	K25
197	no AC & GPMC	GPIO0_39	7	Available in SOM without "AC" and with "GPMC" configuration	K25
35	OSPI	GPIO0_4	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	G24
35	GPMC	GPIO0_40	7	Available in SOM with "GPMC" configuration;	M22
100	GPMC	GPIO0_41	7	Available in SOM with "GPMC" configuration;	M21
102	GPMC	GPIO0_42	7	Available in SOM with "GPMC" configuration;	L21
174		GPIO0_43	7	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K22
176		GPIO0_44	7	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	K24
100	OSPI	GPIO0_5	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	F25
53		GPIO0_51	7	Used internally with "WBD", Function can be released if BT Function disabled	Y23
52		GPIO0_52	7	Used internally with "WBD", Function can be released if BT Function disabled	AA25
50		GPIO0_57	7	Used internally with "WBD", Function can be released if BT Function disabled	AB25
51		GPIO0_58	7	Used internally with "WBD", Function can be released if BT Function disabled	AA24
59	OSPI	GPIO0_6	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	F24
31	MMC2 & no (WB or WBD)	GPIO0_65	7	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	D24
33	MMC2 & no (WB or WBD)	GPIO0_66	7	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	E23

Pin#	Assy	Pin Function	Alt#	Notes	Ball
35	MMC2 & no (WB or WBD)	GPIO0_67	7	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	C25
102	MMC2 & no (WB or WBD)	GPIO0_68	7	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	B24
76	MMC2 & no (WB or WBD)	GPIO0_69	7	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	D25
79		GPIO0_7	7	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J23
100	MMC2 & no (WB or WBD)	GPIO0_70	7	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	C24
47	MMC2 & no (WB or WBD)	GPIO0_71	7	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	A23
59	MMC2 & no (WB or WBD)	GPIO0_72	7	Available in SOM without WB and without WBD; Referenced to pin 36 supply (1.8V/3.3V)	B23
1	no EC	GPIO0_73	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	AD19
97	no EC	GPIO0_74	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE19
11	no EC	GPIO0_75	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE20
9	no EC	GPIO0_76	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD20
5	no EC	GPIO0_77	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE18
3	no EC	GPIO0_78	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD18
15	no EC	GPIO0_79	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE17
75		GPIO0_8	7	Pin referenced to 1.8V in SOM with "OSPI" configuration;	J25
16	no EC	GPIO0_80	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V,	AD17

Pin#	Assy	Pin Function	Alt#	Notes	Ball
				In "RG2CM" configuration referenced to 1.8V;	
4	no EC	GPIO0_81	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AB17
6	no EC	GPIO0_82	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AC17
10	no EC	GPIO0_83	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AB16
12	no EC	GPIO0_84	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AA15
30		GPIO0_85	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Pin has an internal 1.47K Pull Up Do not alter pinmux with "EC" configuration	AB22
74		GPIO0_86	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Do not alter pinmux with "EC" configuration	AD24
113		GPIO0_87	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AA19
96		GPIO0_88	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AE21
73		GPIO0_89	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	Y18
70		GPIO0_9	7	Pin referenced to 1.8V in SOM with "OSPI" configuration;	H25
177		GPIO0_90	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AA18
56		GPIO0_91	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD21
55		GPIO1_0	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AC20
120		GPIO1_1	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD22
69		GPIO1_10	7		E18
117		GPIO1_11	7		B20
72		GPIO1_12	7		D20
39		GPIO1_13	7		E19
43		GPIO1_14	7		A20
191	no TP	GPIO1_15	7	Available in SOM without TP	A13
68		GPIO1_16	7		C13
189	no TP	GPIO1_17	7	Available in SOM without TP	A14
187	no TP	GPIO1_18	7	Available in SOM without TP	B13
193	no TP	GPIO1_19	7	Available in SOM without TP	B14
57		GPIO1_2	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	AD23
83		GPIO1_20	7	Used as debug UART on Variscite base board	D14
85		GPIO1_21	7	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	E14
44		GPIO1_24	7		C15
46		GPIO1_25	7		E15

Pin#	Assy	Pin Function	Alt#	Notes	Ball
88		GPIO1_26	7		B16
87		GPIO1_27	7		A16
92		GPIO1_28	7		B17
90		GPIO1_29	7		A17
122		GPIO1_3	7	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AE23
29		GPIO1_30	7		A18
81		GPIO1_4	7	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AB20
65		GPIO1_42	7	Bank voltage set on SOM 1.8V/3.3V	D22
61		GPIO1_43	7	Bank voltage set on SOM 1.8V/3.3V	C21
63		GPIO1_44	7	Bank voltage set on SOM 1.8V/3.3V	B21
62		GPIO1_45	7	Bank voltage set on SOM 1.8V/3.3V	A22
60		GPIO1_46	7	Bank voltage set on SOM 1.8V/3.3V	B22
64		GPIO1_47	7	Bank voltage set on SOM 1.8V/3.3V	A21
80		GPIO1_48	7	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D17
124		GPIO1_49	7		C17
71		GPIO1_5	7	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AC21
94		GPIO1_50	7		C20
82		GPIO1_51	7		F18
54		GPIO1_6	7	By default, referenced to 3.3V, In “RG2CM” configuration referenced to 1.8V;	AE22
45		GPIO1_7	7		B19
41		GPIO1_8	7		A19
17		GPIO1_9	7		B18

Table 94: MCU GPIO Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
153		MCU_GPIO0_1	7		B8
147		MCU_GPIO0_10	7		C5
142		MCU_GPIO0_11	7		C6
143		MCU_GPIO0_12	7		A4
157		MCU_GPIO0_13	7		D6
155		MCU_GPIO0_14	7		B3
156		MCU_GPIO0_15	7		E5
154		MCU_GPIO0_16	7		D4
146		MCU_GPIO0_17	7	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	A8
148		MCU_GPIO0_18	7	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	D10
140		MCU_GPIO0_19	7	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	B9
150		MCU_GPIO0_2	7		A7
141		MCU_GPIO0_20	7	Internal signal pulled up to SOM_PGOOD using 10K resistor (In SOM v1.1 and higher).	A9
128		MCU_GPIO0_21	7		B12
151		MCU_GPIO0_3	7		D9
152		MCU_GPIO0_4	7		C9
91		MCU_GPIO0_5	7		B5
99		MCU_GPIO0_6	7		A5
58		MCU_GPIO0_7	7		A6
93		MCU_GPIO0_8	7		B6
145		MCU_GPIO0_9	7		B4

8.23 Power

8.23.1 Power

Table 95: Power

Pin#	Assy	Pin Function	Alt#	Notes	Ball
32, 34, 103, 105, 107, 109, 111		VCC_SOM		SOM Power	VCC_SOM
36	no GPMC & no OSPI & no MMC2	VCC_SOM		SOM Power	VCC_SOM
36	MMC2 & no (WB or WBD)	VDDSHV6		MMC2 pins group power IN “no MMC2" configuration: * Not Connected "MMC2" configuration: VDDSHV6 1.8V/3.3V voltage input. Must supply one option: 1.8 or 3.3V, Use SOM pin 49 to sequence 1.8 or 3.3V supply. The following SOM pins are referenced to this voltage: 31,33,35,47,59,76,100,102	J18
106		USB0_VBUS		USB PHY power pin (5V) input	AC11
104		USB1_VBUS		USB PHY power pin (5V) input	AB10
49		SOM_PGOOD		SOM Peripherals’ 3.3v rail Output. Should be used to sequence carrier board peripherals’ 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw allowed.	SOM_PGOOD

8.23.2 Ground

Table 96: Digital Ground Pins

Pin#	Assy	Pin Function	Alt#	Notes	Ball
2, 7, 8, 13, 14, 19, 27, 28, 37, 47, 59, 66, 67, 76, 78, 89, 95, 101, 112, 118, 126, 132, 138, 139, 144, 149, 158, 159, 169, 172, 178, 179, 185		GND		Digital ground	GND
47, 59, 76	no GPMC & no OSPI & no MMC2	GND		Digital ground	GND
195	AC	AGND		Audio ground	AGND

8.24 System Control

8.24.1 General SOM control Signals

Table 97: General SOM Control Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
49		SOM_PGOOD		SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw is allowed.	SOM_PGOOD
98		SYS_NRSTIN_3V3		SOM reset input pin. Internally pulled up. Connected via diode to internal (not exposed) 1.8V MCU_PORz ball. Once it is asserted low, CPU MCU and MAIN domains perform cold reset.	D2 (via diode)

8.24.2 Main domain System Signals

Table 98: Main System Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		EXT_REFCLK1	0	External clock input to Main Domain	A18
21		OBSCLK0	8	Main Domain Observation clock output for test and debug purposes only BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T25
88		OBSCLK0	3	Main Domain Observation clock output for test and debug purposes only	B16
134		RESET_REQz	0	Main Domain external warm reset request input. Internal signal pulled up to SOM_PGOOD using 10K resistor.	F20
29		SYSCLKOUT0	3	Main Domain system clock output (divided by 4) for test and debug purposes only	A18

8.24.3 MCU domain System Signals

Table 99: MCU System Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
136		MCU_ERRORn	0	Pin is referenced to 1.8V Error signal output from MCU Domain ESM Internal signal pulled down to GND using 10K resistor.	D1
153		MCU_EXT_REFCLK0	3	External input to MCU Domain	B8
156		MCU_EXT_REFCLK0	4	External input to MCU Domain	E5
153		MCU_OBSCLK0	1	MCU Domain Observation clock output for test and debug purposes only	B8
98		SYS_NRSTIN_3V3	0	SOM reset input pin. Connected via diode to internal (not exposed) 1.8V MCU_PORz signal. Internally pulled up. Once it is asserted low, CPU MCU and MAIN domains perform cold reset.	D2 (via diode)
128		MCU_RESETSTATz	0	MCU Domain warm reset status output	B12
130		MCU_RESETz	0	Internal signal pulled up to SOM_PGOOD using 10K resistor.	E11
153		MCU_SYSCLKOUT0	2	MCU Domain system clock output (divided by 4) for test and debug purposes only	B8

8.24.4 Boot configuration

The VAR-SOM-AM62 can be boot from the following sources:

- Internal source - eMMC Flash memory
- External source - SD Card

The AM62x BOOTMODE [15:0] pins determine the boot source.
On SOM, logic circuitry drives the BOOTMODE3, BOOTMODE9 lines on time of boot.
The rest of BOOTMODE pins are strapped internally by PU/PD resistors.

Boot source selection is done via **pin 42** of the SOM-DIMM 200 pin connector.

Table 100: BOOT_SEL signal SOM-DIMM 200 pin connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
42		BOOT_SEL		Controls internal OR external boot source; Internal signal pulled up to SOM_PGOOD using 1K resistor; 0=EXT. BOOT 1/Float=INT. BOOT	INT. LOGIC

BOOT_MODE[15:0] are also exposed on the SOM SO-DIMM 200 in order to allow support of other boot sources.

ATTENTION

External drivers connected to BOOTMODE lines exposed to the connector should be disabled on during reset (SYS_NRSTIN_3V3 rise +1ms), otherwise they may change the boot option and the SOM will not boot.

Table 101: BOOTMODE signals on SO-DIMM 200 pin Connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	GPMC	BOOTMODE00	10	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	M25
33	GPMC	BOOTMODE01	10	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N23
76	GPMC	BOOTMODE02	10	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N24
173		BOOTMODE03	10	BOOTMODE03 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	N25
84		BOOTMODE04	10	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P24
48		BOOTMODE05	10	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P22
86		BOOTMODE06	10	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	P21
40		BOOTMODE07	10	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R23
115		BOOTMODE08	10	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R24
171		BOOTMODE09	10	BOOTMODE09 pin, Driven on SOM during boot Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R25
21		BOOTMODE10	10	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T25
26		BOOTMODE11	10	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	R21
24		BOOTMODE12	10	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T22
25		BOOTMODE13	10	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T24
23		BOOTMODE14	10	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U25
22		BOOTMODE15	10	BOOTMODE15 pin, 100K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U24

9. Assembly Options

To make the solution as Flexible as possible the following assembly options were added. The assembly options help customers to order the SOM variant that includes only the needed interfaces with a lower cost.

9.1 GPMC/OSPI/MMC2

The SOM can be ordered with the GPMC/OSPI/MMC2 related pins exposed.

Table 102: GPMC/OSPI/MMC2 assembly option

	Default SOM option (no GPMC & no OSPI & no MMC2)		Special SOM option (GPMC)		Special SOM option (OSPI)		Special SOM option (MMC2)	
Pin #	Pin Function	Ball	Pin Function	Ball	Pin Function	Ball	Pin Function	Ball
31	NC	NC	GPMC0_AD0	M25	OSPI0_CLK	H24	MMC2_DAT3	D24
33	NC	NC	GPMC0_AD1	N23	OSPI0_LBCLKO	G25	MMC2_DAT2	E23
35	NC	NC	GPMC0_DIR	M22	OSPI0_D1	G24	MMC2_DAT1	C25
36	VCC_SOM	VCC_SOM	GPMC0_OEN_REN	L24	OSPI0_DQS	J24	VDDSHV6	J18
47	GND	GND	GPMC0_BE1N	N20	OSPI0_CSN3	E24	MMC2_SDCD	A23
59	GND	GND	GPMC0_CLK	P25	OSPI0_D3	F24	MMC2_SDWP	B23
76	GND	GND	GPMC0_AD2	N24	OSPI0_D0	E25	MMC2_CLK	D25
100	NC	NC	GPMC0_CSN0	M21	OSPI0_D2	F25	MMC2_CMD	C24
102	NC	NC	GPMC0_CSN1	L21	OSPI0_CSN0	F23	MMC2_DAT0	B24

9.2 Analog Audio Codec

The SOM can be ordered without Audio Codec chip assembled. This allows reducing the overall cost of the product in case the Analog Audio Codec is not used.
when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

Note: For layout reasons, in case of SOM without Audio Codec assembled, the export of CPU balls K25,L25 depends on GPMC assembly option as follows:

Table 103: (no AC & no GPMC/ no AC & GPMC) assembly option

	SOM option (no AC & no GPMC)		SOM option (no AC & GPMC)	
Pin #	Pin Function	Ball	Pin Function	Ball
18	GPMC0_WEN	L25	NC	NC
20	GPMC0_WPN	K25	NC	NC
196	NC	NC	GPMC0_WEN	L25
197	NC	NC	GPMC0_WPN	K25

9.3 Single/Dual band Wi-Fi and BT/BLE combo

The SOM can be ordered without the Single or Dual band Wi-Fi and BT/BLE combo chip assembled, it allows reducing the overall cost of the product in case the Wi-Fi and BT/BLE is not used.

9.4 Resistive Touch

The SOM can be ordered without Resistive Touch controller assembled. This allows reducing the overall cost of the product in case the Resistive Touch is not used.
when not assembled, SoC balls are exported to SOM connector instead of Resistive Touch interface pins.

9.5 Ethernet PHY

The SOM can be ordered without Ethernet PHY chip assembled; it allows reducing the overall cost of the product in case the Ethernet Interfaces are not used.
when not assembled, SoC balls are exported to SOM connector instead of Ethernet interface pins.

9.6 DDR4

The SOM can be ordered with different RAM size capacities, it allows reducing the overall cost of the product in case lower RAM size is sufficient.

9.7 eMMC

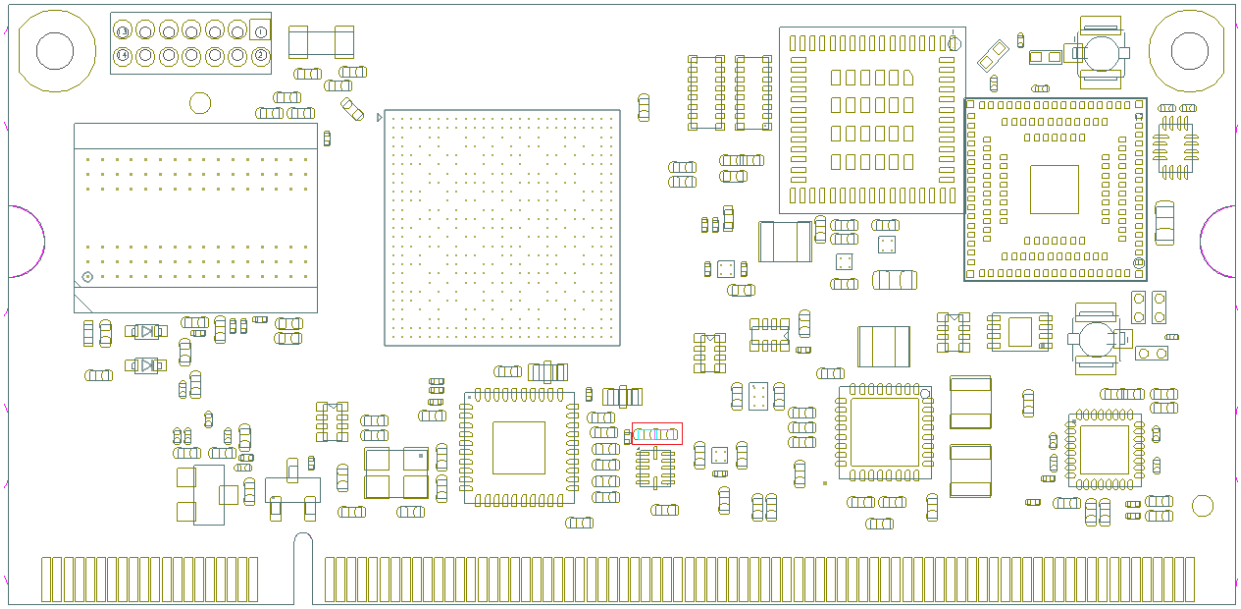
The SOM can be ordered with different eMMC size capacities, it allows reducing the overall cost of the product in case lower eMMC size is sufficient.

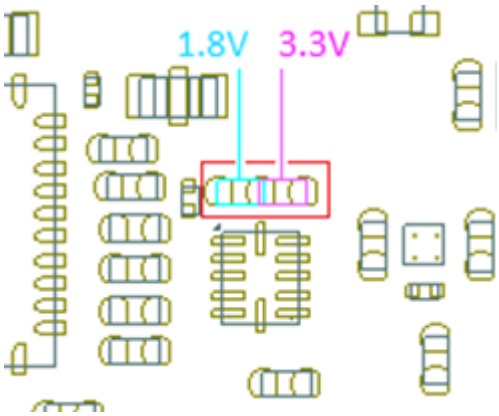
9.8 RG2CM

The SOM can be ordered with RGMII2/RMII2 signals referenced to 1.8V, for compatibility with other VAR-SOM family modules in which RGMII2 operates at 1.8V.
Note that with RG2CM configuration, in case of “no EC”, RGMII1/RMII1 signals exported via SOM connectors will also run at 1.8V.

The voltage is set according to resistor assembly which provides power to VDDSHV2 domain of CPU.
In “no RG2CM” configuration, the right resistor will be assembled and voltage will be set to 3.3V.
In “RGCM” configuration, left resistor will be assembled and voltage will be set to 1.8V.

(Resistors are 0R OHM, 1/16W, 5%, 0402 P/N: RC0402JR-070RL or equivalent)





10. Electrical Specifications

10.1 Absolute Maximum Ratings

Table 104: Absolute Maximum Ratings

Pin #	Min	Max	Units	Comments
VCC_SOM	-0.3	3.6	V	
USB0_VBUS, USB1_VBUS	-0.3	5.25	V	
VDDSHV6	-0.3	3.63	V	
ESD damage immunity Human Body Model (HBM)	--	+/-1000	V	Per ANSI/ESDA/JEDEC JS-001
ESD damage immunity Charge Device Model (CDM)	--	+/-250	V	Per ANSI/ESDA/JEDEC JS-002

10.2 Operating Conditions

Table 105: Operating Ranges

Parameter		Min.	Typ.	Max.	Unit
VCC_SOM		3.25	3.3	3.45	V
USB0_VBUS, USB1_VBUS		4.75	5	5.25	V
VDDSHV6	1.8	1.71	1.8	1.89	V
	3.3	3.135	3.3	3.465	

10.3 Peripheral Voltage Levels

Most of the peripheral interface lines used as inputs or output to the VAR-SOM-AM62 uses 3.3V levels, with the below exceptions for the following interfaces: USB, MIPI-CSI,LVDS,MMC1, MMC2, RGMII1/RGMII2, OSPI, MCU_ERRORN.

***USB/MIPI-CSI/LVDS*:** Interfaces follow a different standard since they are high-speed signals.

MMC1: (SDIO lines) interface IOs will change voltage between 3.3V and 1.8V depending on the SD card capabilities. With other alternative function user can determine the voltage MMC1 IOs bank will be 1.8V or 3.3V;

MMC2: interface available in case SOM is ordered with "MMC2." interface IOs will run at voltage 1.8V or 3.3V levels depending on the power fed to VDDSHV6 (pin 36) (1.8V/3.3V)

RGMII1/RMI1, RGMII2/RMII2:
In “no RG2CM” configuration – pins will be referenced to 3.3V
In “RG2CM” configuration – pins will be referenced to 1.8V

OSPI: interface available in case SOM is ordered with "OSPI." interface IOs will run at 1.8V levels.

MCU_ERRORN: Signal is refenced to 1.8V levels

10.4 Power Consumption

Table 106: VAR-SOM-AM62 Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.35V	710mA	2.37W	Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz (Dual Band Module)
Run	3.35V	620mA	2.07W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz (Dual Band Module)
Run	3.35V	TBD		Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz (Single Band Module)
Run	3.35V	550mA	1.84W	Linux up. Ethernet0 & Ethernet1 running benchmark
Run	3.35V	387mA	1.29W	Linux up. Ethernet0, Ethernet1, Wi-Fi module up
Standby	3.35V	TBD		Memory retention mode
Off	3.35V	TBD		All power rails are Off

NOTE

HW Setup:
VAR-SOM-AM62_1400C_2048R_16G_AC_EC_TP_WBD_IT V1.0

Note: *The Wi-Fi module needs a power source that can provide a peak current of 750 mA for around 20 milliseconds during transmitter calibration, even though its max continuous supply current is less than 320 mA.*
Module calibration occurs:

- *When the Module is initially powered up.*
- *The module is reset.*
- *When the radio is initialized.*
- *Every two minutes after the radio is initialized.*

DISCLAIMER:

The power consumption measurements apply only to limited operation scenarios. Actual power consumption may vary depending on the interfacing peripherals and user application modes; Users must conduct testing per their specific operation scenarios.

Depending on the specific use cases and end product system design, an appropriate thermal solution should be applied.

11. Environmental Specifications

Table 107: Environmental Specifications

Parameter	Min	Max
Extended Operating Temperature Range	0°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Prediction Method Model: Telcordia Technologies Special Report SR-332, Issue 4 50°C, GB	> TBD Khrs	

Note: Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

12. Mechanical

12.1 Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-3.0-M2-B**

12.2 Thermal Management

Certain operation scenarios may prompt the use of an external heat dissipation solution.
To handle intensive applications where thermal management is required, Variscite offers a heat sink designed for the VAR-SOM-AM62 family:

Variscite PN: VHP-AM62

DISCLAIMER:
Implemented solution may vary depending on the device operation scenario as well as its mechanical design. Thermal solution must be evaluated.

12.3 SOM Dimensions

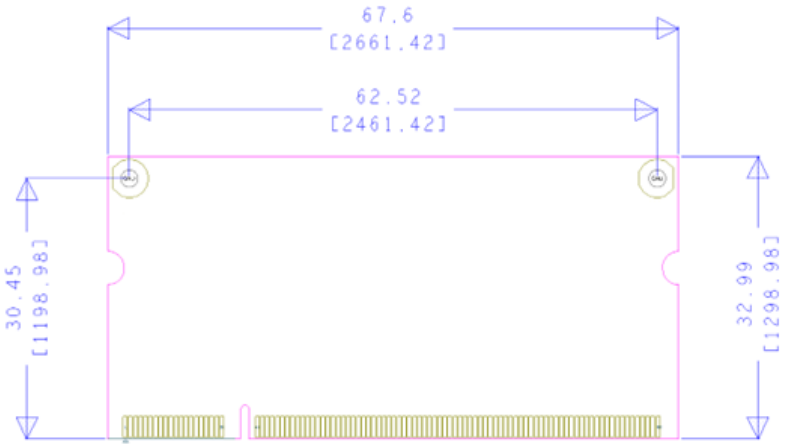


Figure 5: VAR-SOM-AM62 Mechanics in millimeters [mils]

12.3.1 CAD Files

CAD files are available for download at http://www.variscite.com/

13. Legal Notice

Variscite Ltd. ("Variscite") products and services are sold subject to Variscite terms and conditions of sale, delivery and payment supplied at the time of order acknowledgement.

Variscite warrants performance of its products to the specifications in effect at the date of shipment. Variscite reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant product information from Variscite to verify that their reference is current.

Testing and other quality control techniques are utilized to the extent that Variscite deems necessary to support its warranty.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

In order to minimize risks associated with customer applications, the customer must use adequate design and operating safeguards to minimize inherent or procedural hazards. Variscite is not liable for applications assistance or customer product design. The customer is solely responsible for its selection and use of Variscite products. Variscite is not liable for such selection or use or for use of any circuitry other than circuitry entirely embodied in a Variscite product.

Variscite products are not intended for use in life support systems, appliances, nuclear systems or systems where malfunction can reasonably be expected to result in personal injury, death or severe property or environmental damage. Any use of products by the customer for such purposes is at the customer's own risk.

Variscite does not grant any license (express or implied) under any patent right, copyright, mask work right or other intellectual property right of Variscite covering or relating to any combination, machine, or process in which its products or services might be or are used. Any provision or publication of any third party's products or services does not constitute Variscite's approval, license, warranty or endorsement thereof. Any third-party trademarks contained in this document belong to the respective third-party owner.

Reproduction of information from Variscite datasheets is permissible only if reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices (including this notice) and conditions. Variscite is not liable for any un-authorized alteration of such information or for any reliance placed thereon.

Any representations made, warranties given, and/or liabilities accepted by any person which differ from those contained in this datasheet or in Variscite's standard terms and conditions of sale, delivery and payment are made, given and/or accepted at that person's own risk. Variscite is not liable for any such representations, warranties or liabilities or for any reliance placed thereon by any person.

14. Warranty Terms

Variscite guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Variscite's sole liability shall be for Variscite, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Disclaimer of Warranty

THIS WARRANTY IS MADE IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL VARISCITE BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL VARISCITE BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT. BY ORDERING THE SOM, THE CUSTOMER APPROVES THAT THE VARISCITE SOM, HARDWARE AND SOFTWARE, WAS THOROUGHLY TESTED AND HAS MET THE CUSTOMER'S REQUIREMETS AND SPECIFICATIONS.

15. Contact Information

Headquarters:
Variscite Ltd.

9, Hamelacha Street
Lod
P.O.B 1121
Airport City, 70100
ISRAEL

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

Sales: sales@variscite.com

Technical Support: support@variscite.com

Corporate Website: www.variscite.com