



CONTENT

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Disclaimer:

Schematics are for reference only.
 Variscite LTD provides no warranty for the use of these schematics.
 Schematics are subject to change without notice.

Revision History

Document	Carrier	
1.0	1.0	Initial
1.1	1.1	Released
1.2	1.1	Updated Block Diagrams Added SH1 wire short symbol Updated Compatibility value for SOM pins 68,69,176 Updated SOM pin 22 net name Fixed U29_B1, C113_1 net name Fixed R1-R2,R35-R38 net name
1.3	1.2	Removed SH1 wire short, J1.68 routed to capacitive touch Changed R29 to C185 Changed R123,R127 to N.C. Added resistors R130-132 Removed ADC_Nxx alternate function from VAR-SOM-MX8 Symbol Updated PCIe resistor assembly note
1.4	1.2	Updated Parallel Camera/HDMI/DP Note Fixed ETH pin names VAR-SOM-MX8X Symbol
1.5	1.2A	Disconnected R129
1.6	1.2A	Added VAR-SOM-MX8M-MINI Block Diagram and Symbol PRE-RELEASE VERSION !!!!! Subject to change without notice
1.7	1.2B	Fixed VAR-SOM-MX8M-MINI Symbol Changed U29,U30,U31 to P/N: PPF2193 Changed R60 to 47K
1.8	1.2C	Update VAR-SOM-MX8M-MINI Symbol to V1.1 with side notes for v1.08(Early access customers) Update VAR-SOM-MX8M-MINI Block Diagram POR circuitry fed by VCC_SOM; see U7 R60 R61 R40 R60 D5 Removed
1.9	1.2D	Raise VCC_3V3 to Nominal 3.30V for VAR-SOM-MX8M-MINI/NANO power up threshold voltage requirement of >3.35V
1.10	1.2E	Reference for new designs: (changes not implemented in V1.2 BRD) * Added x2 studs for heat plate support * Base_per_3v3 added slow rate limit * U7 (Base POR circuit) added CB_WDOG resistor assembly options * U29,U30,U31 - Added assembly note * VAR-SOM-MX8M-NANO pages added with symbol pinout * VAR-SOM-MX8 Connector update - added NC on P7 assembly options * Power switch in OFF position discharge of Custom rails added * Ethernet magnetics - support two Manf: Pulse & UDE; * Base R445 LEDs matched to SOM behaviour
1.11	1.3	* Added VAR-SOM-MX8M-PLUS Preliminary Symbol and Block Diagram * Updated VAR-SOM-MX8M-PLUS Block Diagram * All C1210 capacitor footprint updated to C1210_v0 * MS1 to MS6 not assembled
1.12	1.3A	* ETH1 PHY clock filter U9 replaced with 49.9 Ohm 0603 resistor * Added design note for ETH1 switches U8 and U10.
1.13	1.4	* MS5 and MS6 location adopted to heatplate design - Layout * Update J1 Manufacturer P/N, NAME and footprint to represent the assembled part * Replace PCIe AG caps on RX lines with 0 ohm resistors * Updated VAR-SOM-MX8M-PLUS Symbol pins 1 58 80, swap pins 41 43 and 84 147 * J19 Modify Camera connector orientation * Remove U8 U10 analog switches on ETH1 * U9 revert to GM filter on RGMII_RX clock line * Added RN1 RN2 RN3 R151 R136 isolating stubs on ETH1 RGMII signals * U26 footprint updated to DS * Y1 C58 C67 updated * Support for VAR-SOM-6UL boot: - BOOT_MODE1 - R117 assembled - BOOT_MODE0 - Added PD R149 - USB# FWR to HOST J23 always enabled * Remove R39 on pin J1_156 to support SOM-MX8MP 2nd MIPI-CSI Lane2 routing * J3 J30 pinout change
1.14	1.4A	* Support for VAR-SOM-MX8MP USB OTG - - Changed U5_P4 Pull for board identification, U21.9 connected to GPIO; - Changed R43,R130,R106 to N.C. - Changed R44,R132 to Assembled * Changed Q4 P/N from: TPS27082L (EOL) to -> TPS27081A * Updated VAR-SOM-MX8M-PLUS Block Diagram, Symbol pins 36,38 names * Added notes for SOM pins 29,79,84
1.15	1.4A	Changes in v1.14/1.4A for R43,R44 were not implemented (part of board identification) and only appear in revision history. Board identification implemented via EEPROM US. Board identification required for QS to identify method of OTG ID used: PTN5150 or GPIO
1.16	1.5	* Modified VCC_3V3 to 3.35V nominal for all SOMs. For VAR-SOM-MX8M-MINI/NANO, power up threshold voltage requirement of >3.35V is implemented using Q10,R152 * Added note for VAR-SOM-MX8M-MINI/NANO pin 91
1.17	1.5	* Updated note for I2C#6 pull up resistors
1.18	1.5	* Updated note for PTN36043BXY chip
1.19	1.5A	* Q10 changed to 2N7002P.215 Transistor Q10 changed to 2N7002P to stabilize the SOM voltage in the OFF state. Old transistor leakage current (IDG) changed the feedback current and increased the SOM voltage. 2N7002P does not have SG diode that allowed IDSS to flow into the Gate * SOM Pin 84 Note changed
1.20	1.6	Ethernet PHY replaced to ADIN1300 R22,R23,R35,R36 assembled with Ferrite Bead C185 assembled with 10K resistor, R30 not assembled U2 changed to C8TL02043B USB3 crossover switch changed to C8TL02043B
1.21	1.6A	Due to EOL: U35 changed to NFL18ZT07H1A3D Due to allocation problems: U13 changed to SN65HVD232QDR
1.22	1.6B	Due to allocation problems: U22,U29,U30,U31 changed to P/N: PPF2194
1.23	1.6C	Added VAR-SOM-AM62 Block Diagram and Symbol
1.24	1.7	Added VAR-SOM-MX93 Block Diagram and Symbol Temporary removed compatibility notes Added hand wired EXP_MDIO_EN line.
1.25	1.7A	Due to allocation problems: U22,U29,U30,U31 changed to P/N: PPF2193
1.26	1.7B	J29 changed to USB3090-30-A
1.27	1.7C	Due to allocation problems: U2,U54 changed to P/N: YC7PC0R215MT
1.28	1.7D	C14, C15, C16, C17 Are NC due to compatibility issues with VAR-SOM-MX93 Rev 2.0, WBE Assembly option.
1.29	1.7D	Added VAR-SOM-MX91 Block Diagram and Symbol

For cross probing between SOM symbol and the specific SOM Connector used, set the "Implementation" property value in SOM port symbol to one of the following:

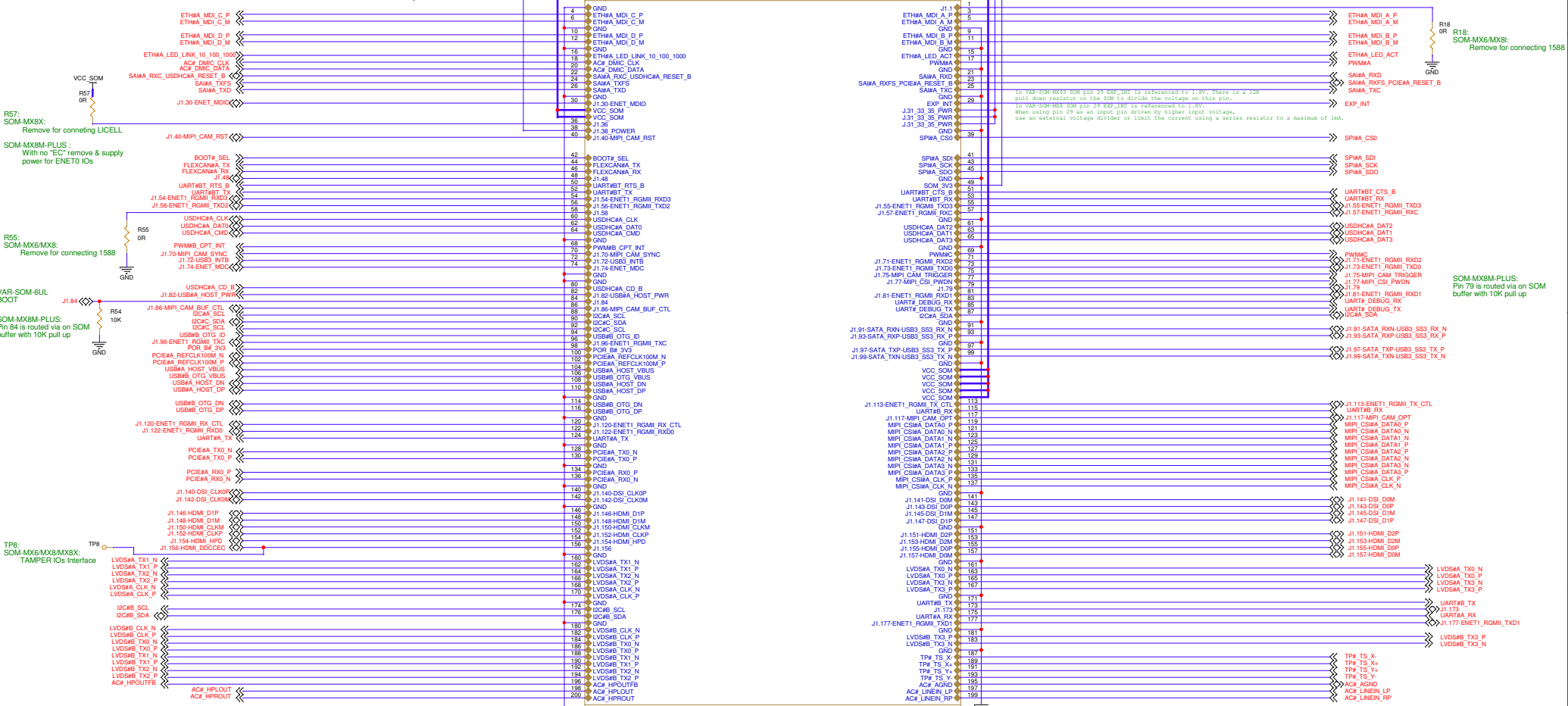
1. VAR-SOM-MX6
2. VAR-SOM-MX8
3. VAR-SOM-MX8X
4. VAR-SOM-MX8M-MINI
5. VAR-SOM-MX8M-NANO
6. VAR-SOM-MX8M-PLUS
7. VAR-SOM-MX93
8. VAR-SOM-MX91
9. VAR-SOM-AM62

For complete alternate function per pin and specific SOM: please refer to "VAR-SOMs Compatibility and Pinout.XLS" located at: ftp://ftp.variscite.com/SOM_Compatibility

OFF PAGE CONNECTOR INDEX:

1. Function# :Interface common to ALL SOMs
2. J1.xxx-Function :Interface common to certain SOMs or Used for carrier board common function
3. J1.xxx :No common interface

Compatibility list
Describes the ALT per SOM for compatibility.
Order of names: (MX6/MX8/MX8X/MX8MM/MX8MN/MX8MP)
Note: single name means identical name for all.



R57: SCM-MX8X: Remove for connecting LICELL

SOM-MX8M-PLUS: With no "EC" remove & supply power for ENET0 IOs

R55: SOM-MX6/MX8: Remove for connecting 1588

VAR-SOM-GUL BOOT: J1.84

SOM-MX8M-PLUS: Pin 84 is routed via on SOM buffer with 10K pull up

TP8: SOM-MX6/MX8/MX8X: TAMPER IOs Interface

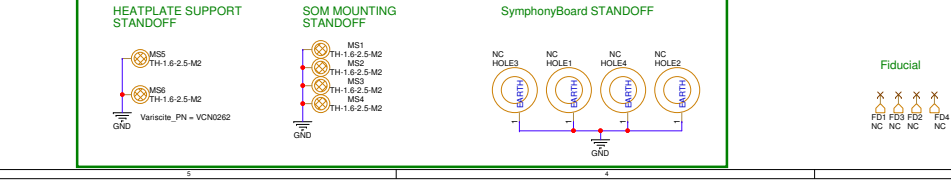
Implementation = VAR-SOM-AM62

SOM_3V3 Output from SOM Used to enable base peripherals power

R18 OR R18: SOM-MX6/MX8: Remove for connecting 1588

SOM-MX8M-PLUS: Pin 79 is routed via on SOM buffer with 10K pull up

MECHANICS



Variscite

File: 03_SOM

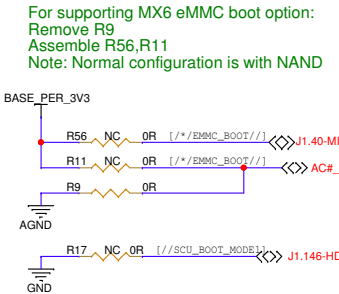
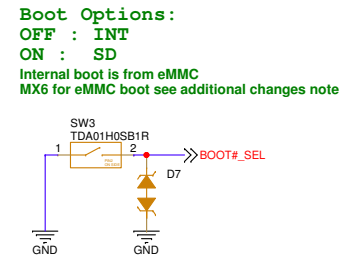
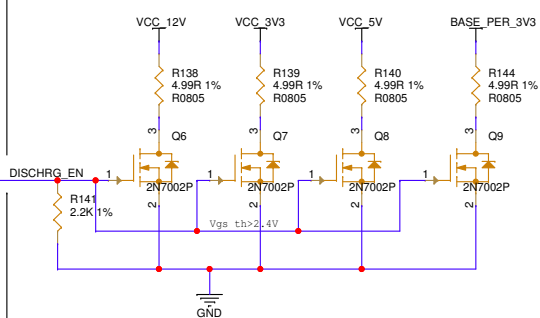
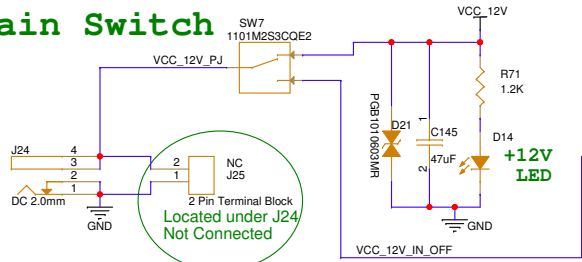
Size: A3	Document Number: Symphony Board	Project: Symphony Board	Rev: 1.70
Date: Sunday, April 06, 2025	Author: H	Approved By:	Sheet 2 of 24

05. Power, Reset, Boot, RTC, EEPROM

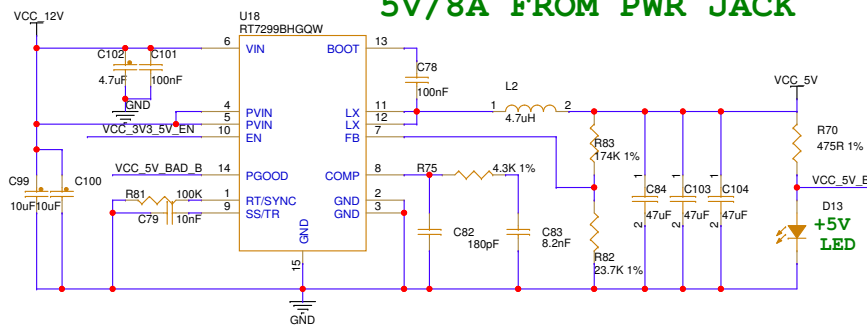
POWER DISCHARGE

SOM BOOTSTRP

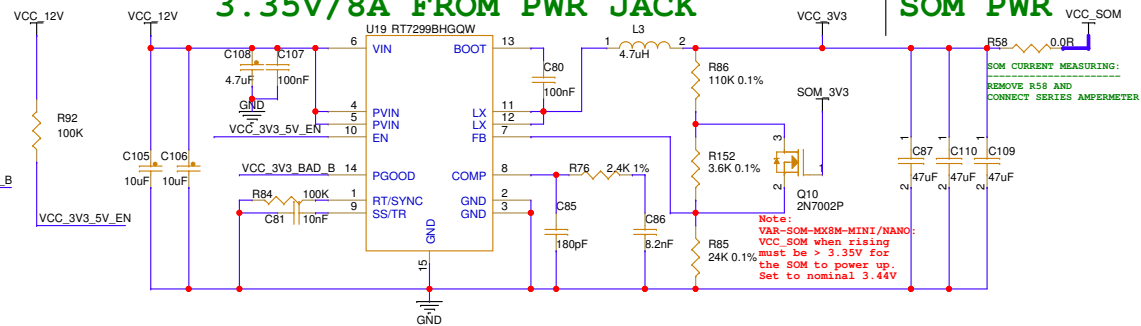
12VDC INPUT Main Switch



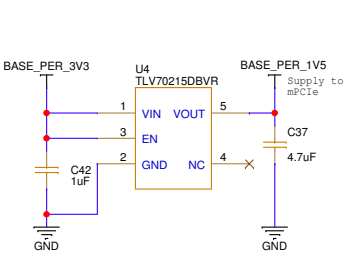
5V/8A FROM PWR JACK



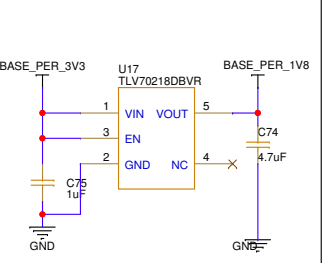
3.35V/8A FROM PWR JACK



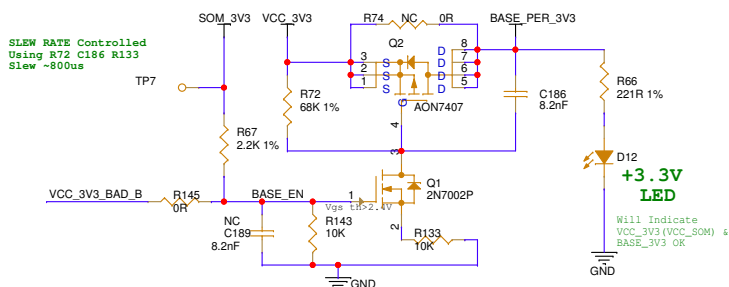
1.5V BASE



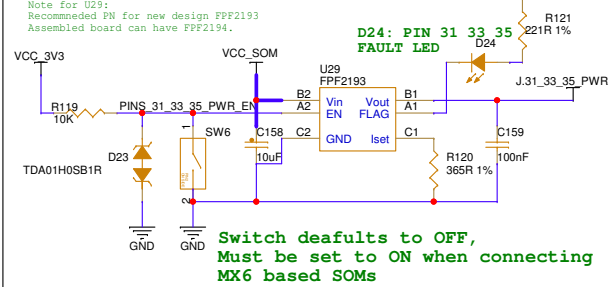
1.8V BASE



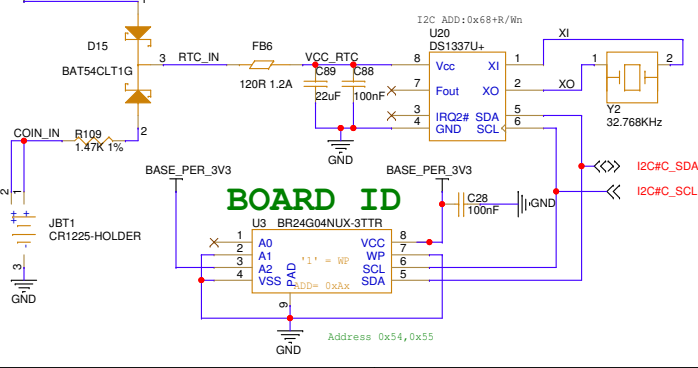
BASE_3V3



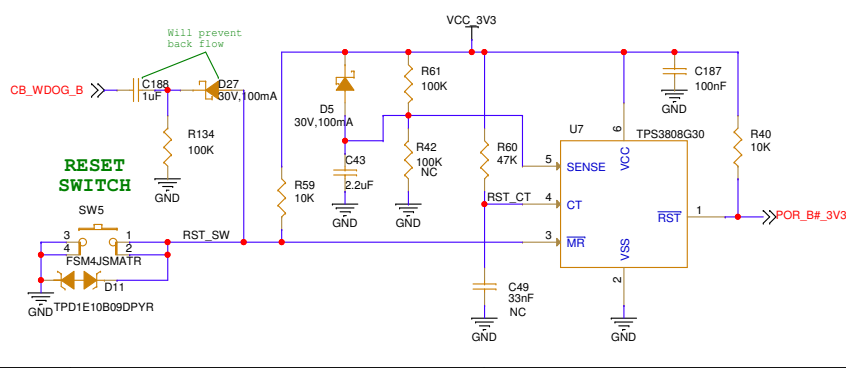
PINS 31 33 35 POWER



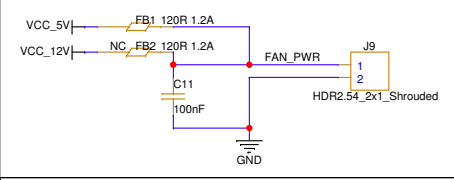
RTC BATTERY



RESET CIRCUITRY



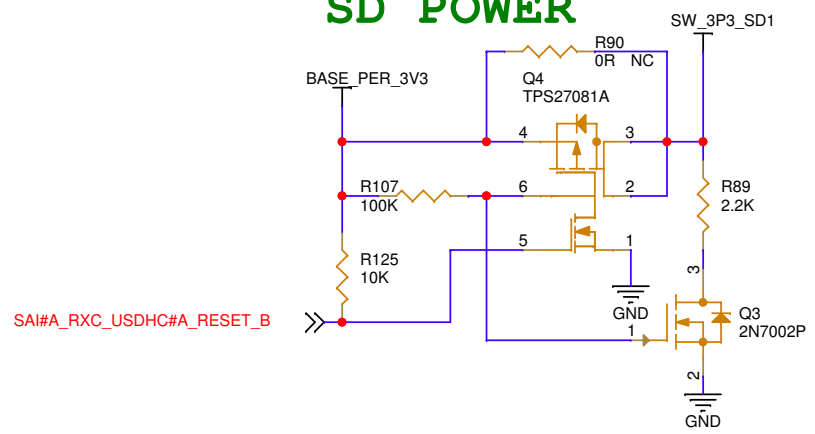
FAN PWR



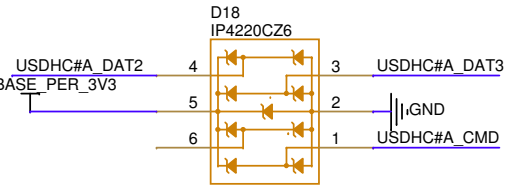
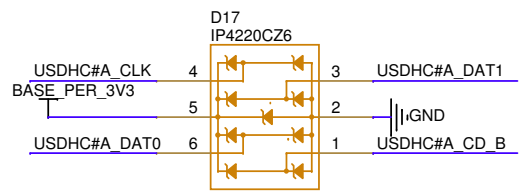
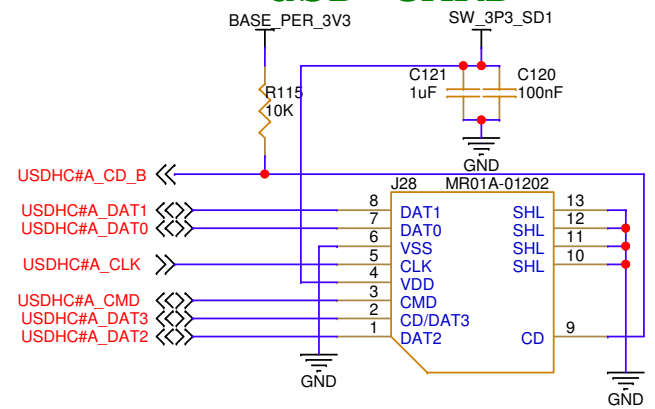
Title: 05. Power,Reset,Boot,RTC,EEPROM			
Size: A3	Document Number:	Project:	Rev: 1.7D_R1.29
Designer: Aviad H.	Date: Sunday, April 06, 2025	Approved By:	Sheet 3 of 24

06. uSD, Audio, CAN

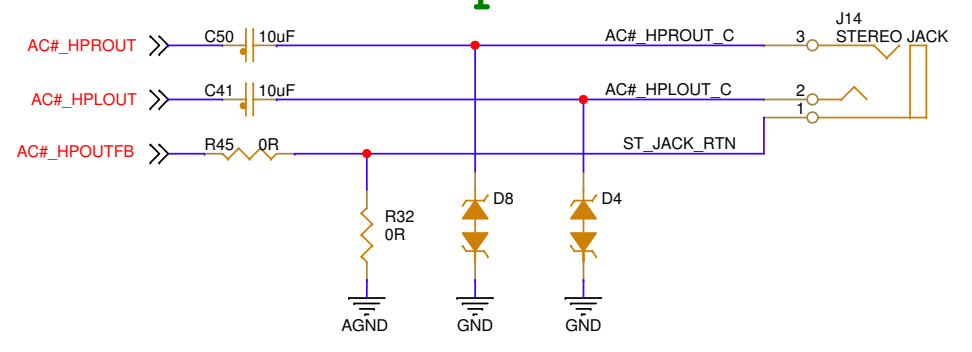
SD POWER



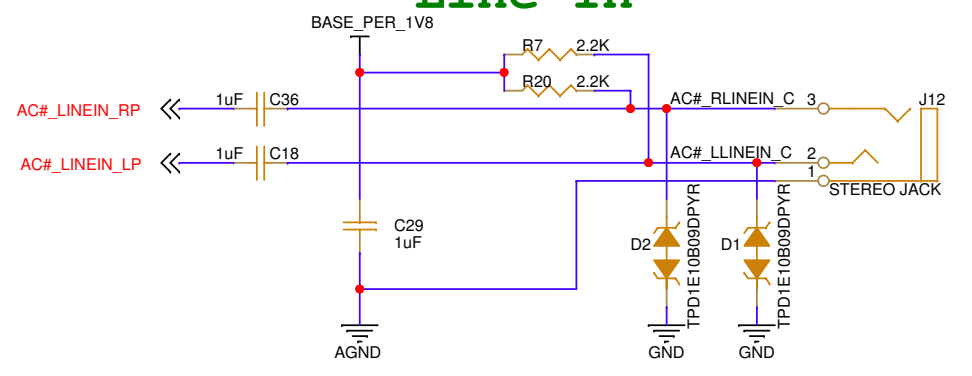
uSD CARD



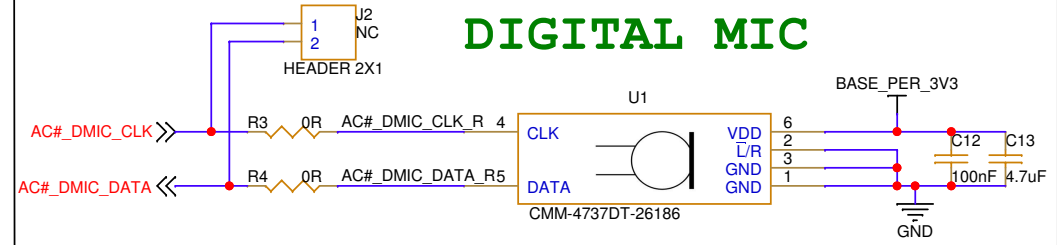
Headphones



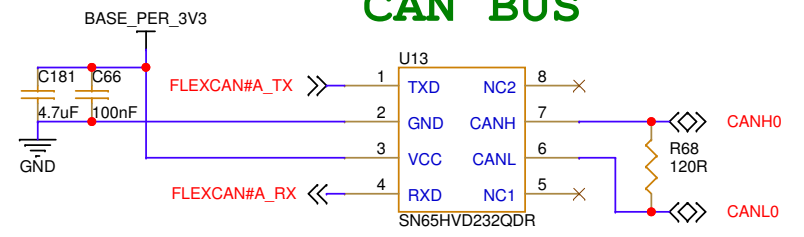
Line In



DIGITAL MIC

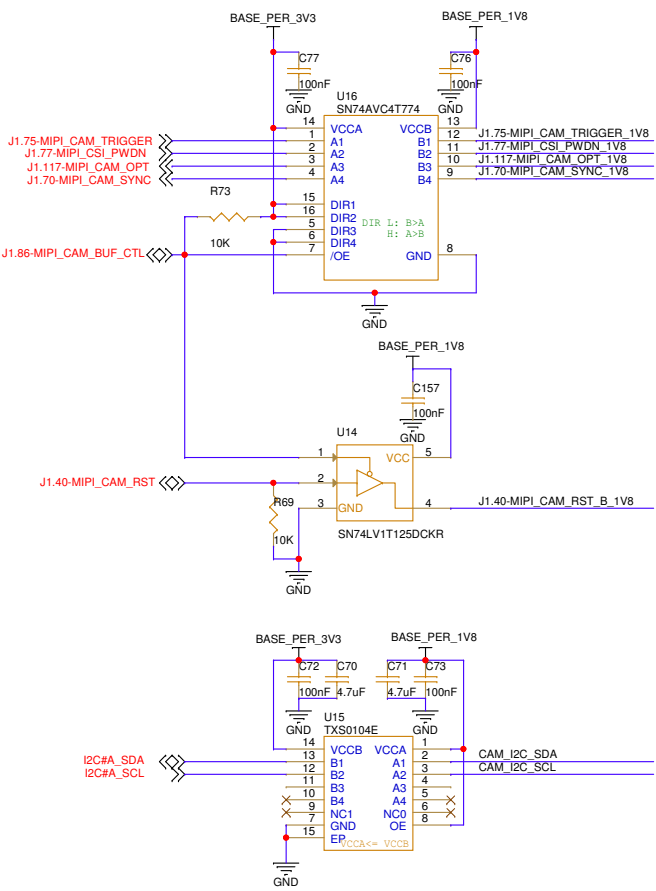


CAN BUS

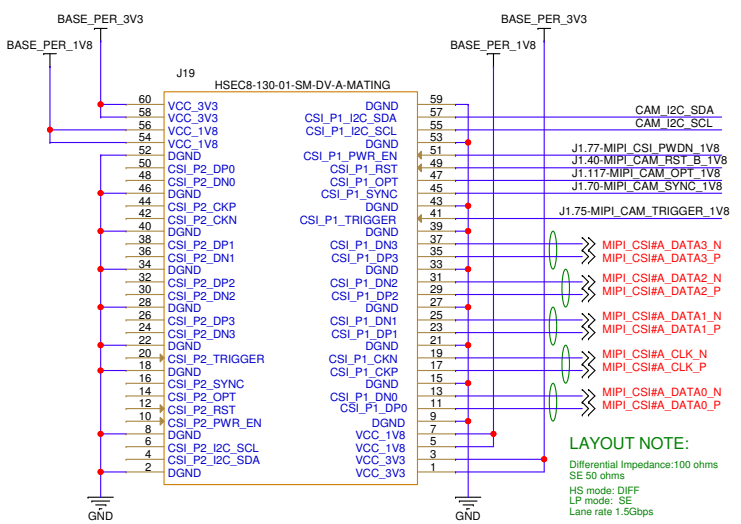


Title 06. uSD, Audio, CAN			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 4 of 24	

07. Camera, HDMI, DP



MIPI-CSI



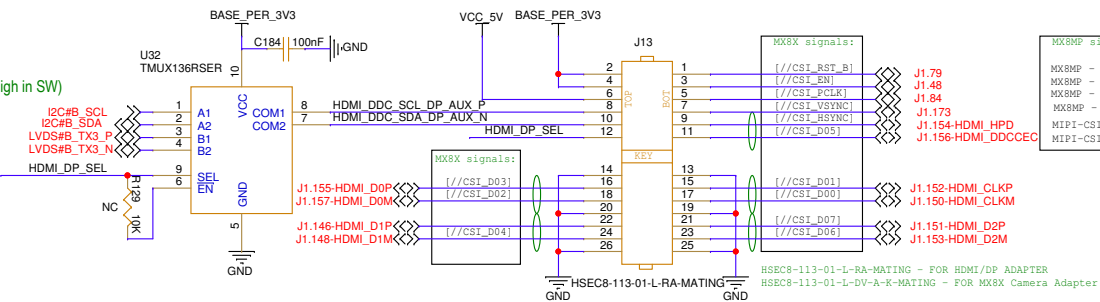
LAYOUT NOTE:
 Differential Impedance: 100 ohms
 SE 50 ohms
 HS mode: DIFF
 LP mode: SE
 Lane rate: 1.5Gbps

Note:
 MIPI_CSI#A signals appears on bottom side of J19
 as of SymphonyBoard V1.4.

Note for U32 (analog switch):
 Switch is to enable support for the following adapters:
 Parallel camera, HDMI, DisplayPort and second MIPI-CSI.

J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

- Switch select controlled on adaptor will select between:
- 1) I2C#B which can export
 - VAR-SOM-MX8X: I2C3 Used by parallel camera
 - VAR-SOM-MX8: HDMI DDC Used by HDMI (GPIO1_22 in should be set High in SW)
 - 2) LVDS#B_TX3 which can export:
 - VAR-SOM-MX8(DP assembly option): HDMI AUX used by DP
- Switch can be omitted when designing for only one of the the above interfaces.



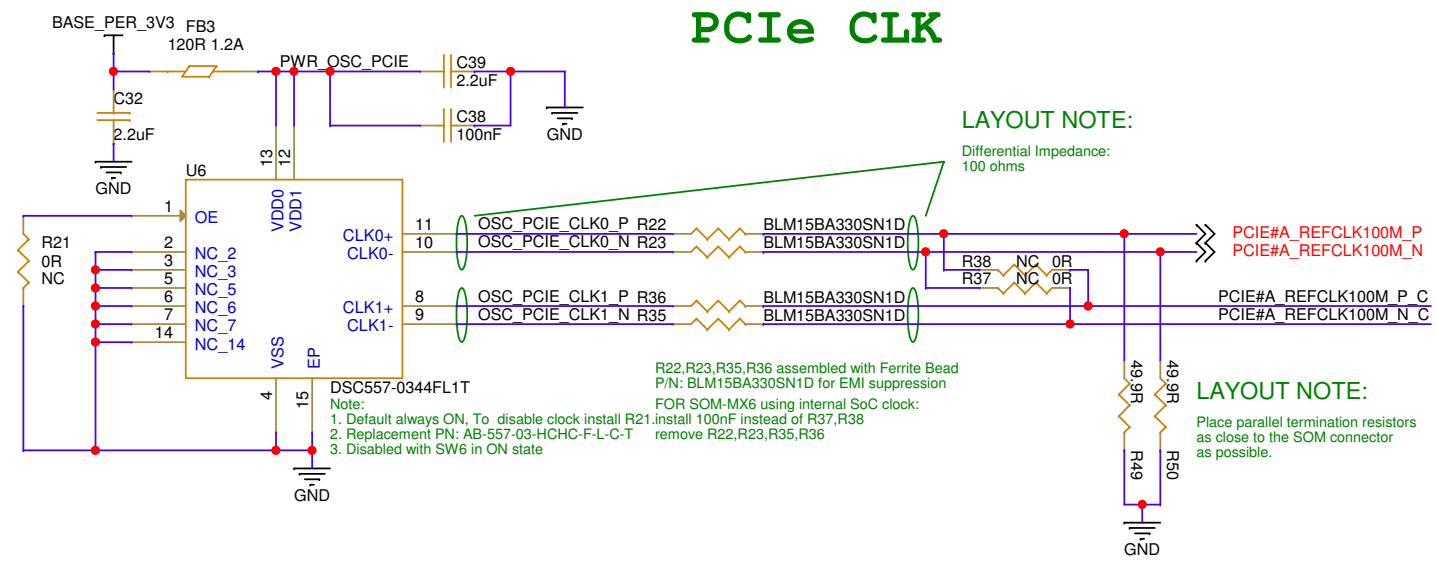
MX8MP signal note:
 MX8MP - via 50Mbps buffer on SOM
 MX8MP - SOC IO
 MX8MP - via 50Mbps buffer on SOM
 MX8MP - SOC IO
 MIPI-CSI-D3_P diff. pair for MX8MP
 MIPI-CSI-D3_N diff. pair for MX8MP



Title 07. Camera, HDMI, DP			
Size A3	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D_R1.29
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 5 of 24	

09. PCIe

PCIe CLK



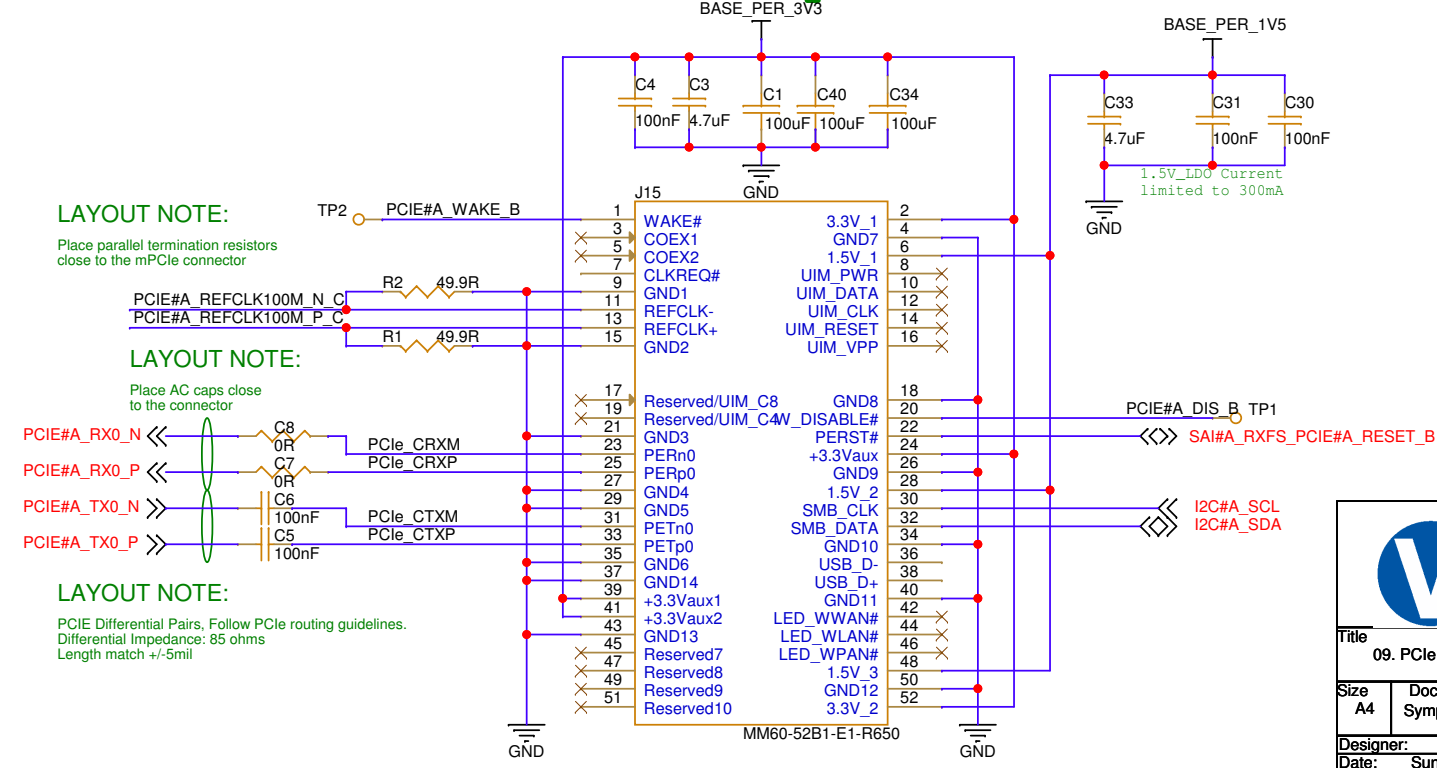
LAYOUT NOTE:
Differential Impedance: 100 ohms

SOM-6UL NAND signals should not be driven

LAYOUT NOTE:
Place parallel termination resistors as close to the SOM connector as possible.

R22,R23,R35,R36 assembled with Ferrite Bead
P/N: BLM15BA330SN1D for EMI suppression
FOR SOM-MX6 using internal SoC clock:
1. Default always ON, To disable clock install R21.install 100nF instead of R37,R38
2. Replacement PN: AB-57-03-HCHC-F-L-C-T remove R22,R23,R35,R36
3. Disabled with SW6 in ON state

mPCIexp



LAYOUT NOTE:
Place parallel termination resistors close to the mPCIe connector

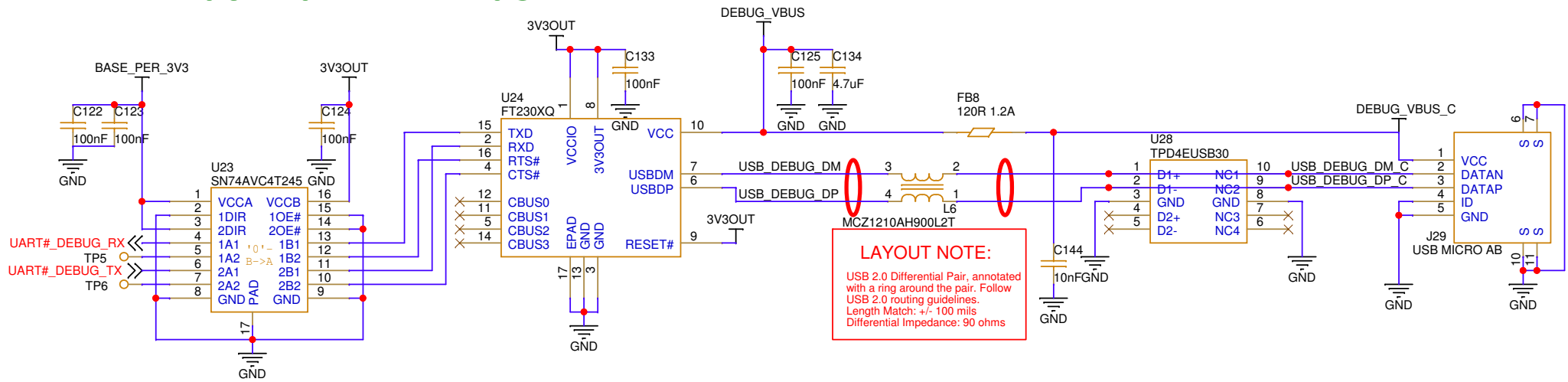
LAYOUT NOTE:
Place AC caps close to the connector

LAYOUT NOTE:
PCIe Differential Pairs, Follow PCIe routing guidelines.
Differential Impedance: 85 ohms
Length match +/-5mil

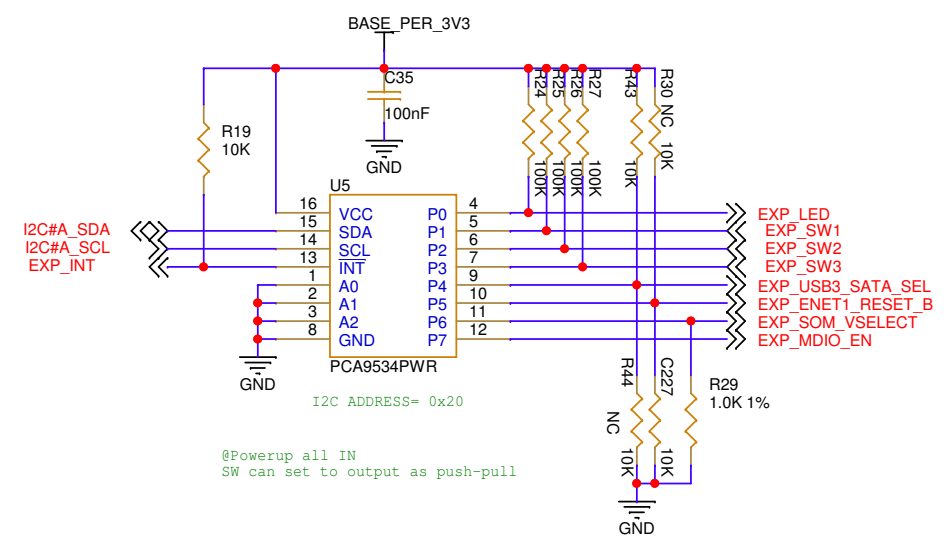
Title			
09. PCIe			
Size	Document Number	Project	Rev
A4	Symphony-Board		1.7D_P1.2
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 7 of 24	

10. Debug, GPIO Exp, Buttons, LED

USB UART DEBUG



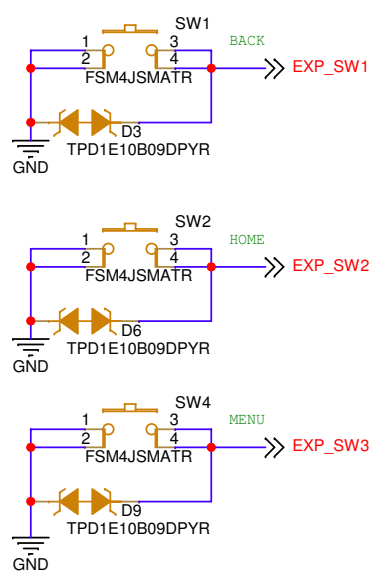
GPIO EXPANDER



@Powerup all IN
SW can set to output as push-pull

In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V.
When using pin 29 as an input pin driven by higher input voltage,
use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

GP BUTTON



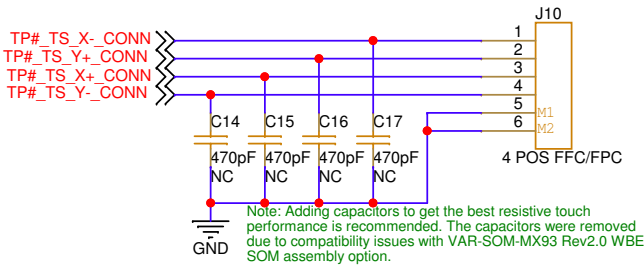
GP LED



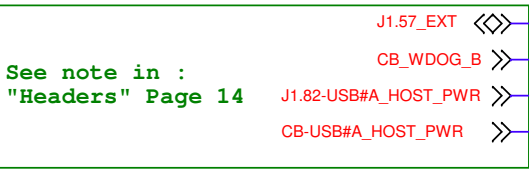
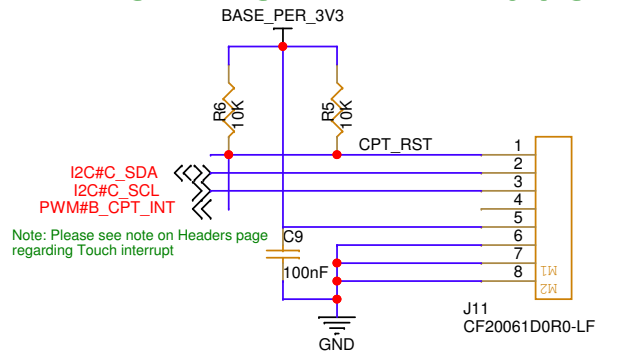
Title 10. Debug, GPIO Exp, Buttons, LED			
Size A4	Document Number Symphony-Board	Project	Rev 1.7D_P1.2
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 8 of 24	

11. LVDS, DSI, Touch

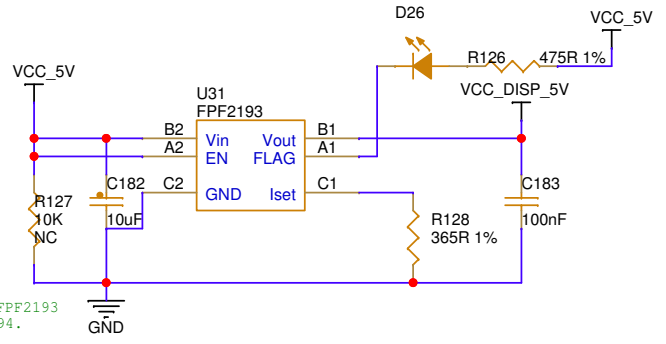
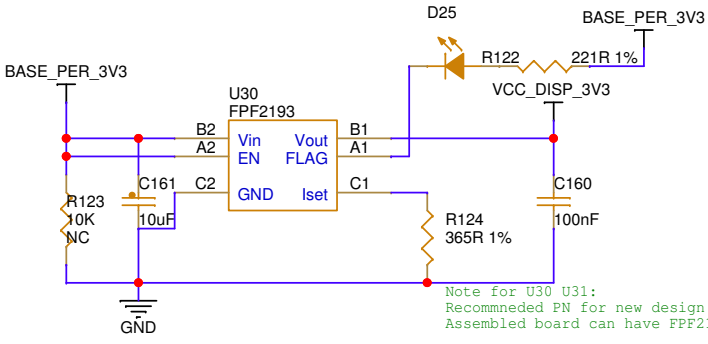
RESISTIVE TOUCH



CAPACITIVE TOUCH



Short circuit protection

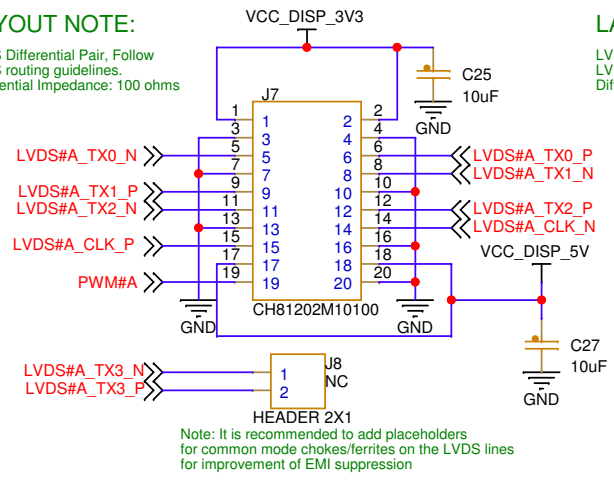


Note for U30 U31:
Recommended PN for new design FPF2193
Assembled board can have FPF2194.

LVDS DISPLAY A

LAYOUT NOTE:

LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

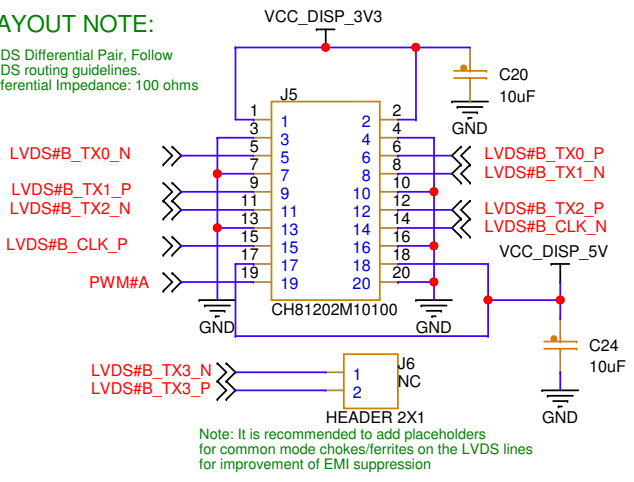


Note: It is recommended to add placeholders for common mode chokes/ferrites on the LVDS lines for improvement of EMI suppression

LVDS DISPLAY B

LAYOUT NOTE:

LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

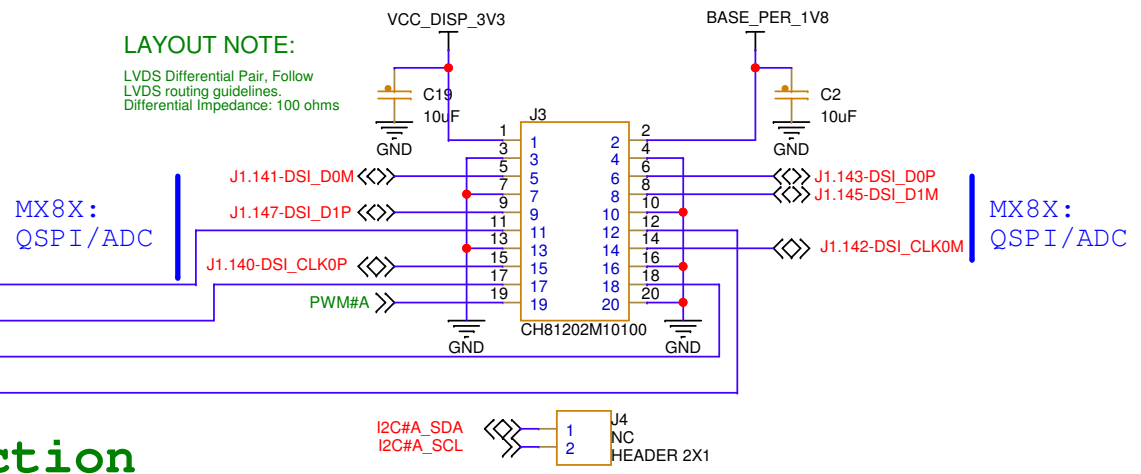


Note: It is recommended to add placeholders for common mode chokes/ferrites on the LVDS lines for improvement of EMI suppression

MIPI DSI DISPLAY

LAYOUT NOTE:

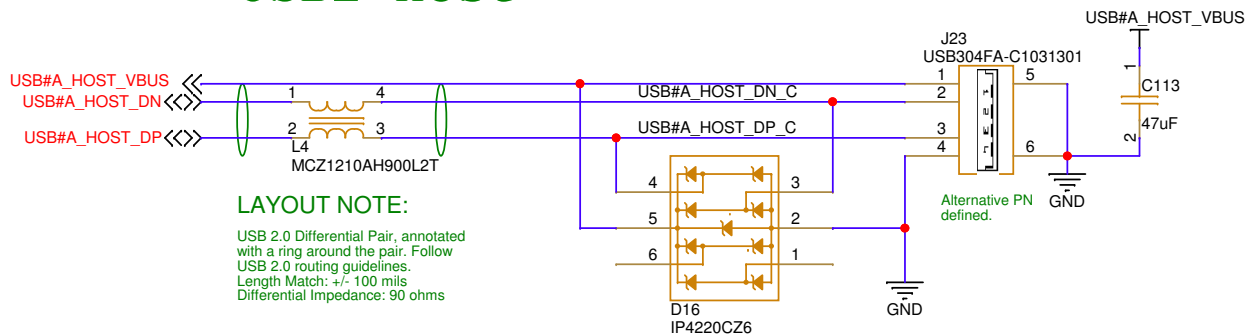
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms



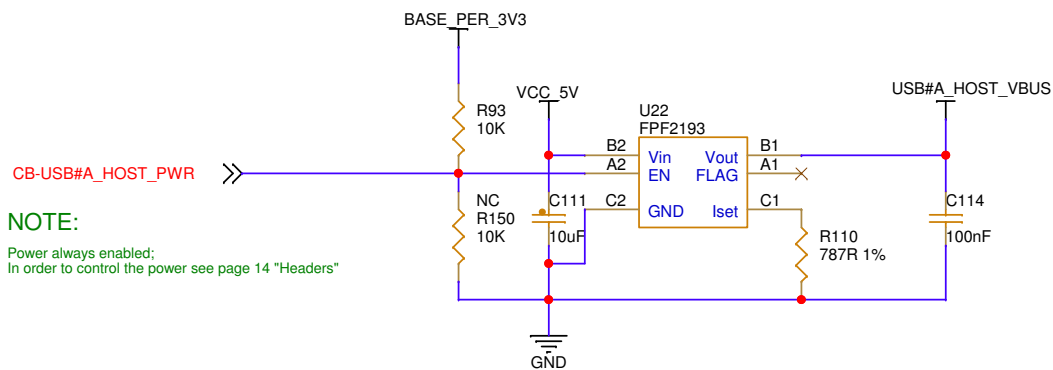
Title 11. LVDS, DSI, Touch			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 9 of 24	

12. USB2 Host

USB2 Host



LAYOUT NOTE:
 USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines.
 Length Match: +/- 100 mils
 Differential Impedance: 90 ohms



NOTE:
 Power always enabled;
 In order to control the power see page 14 "Headers"



Title 12. USB2 Host			
Size A4	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D
Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 10 of 24	

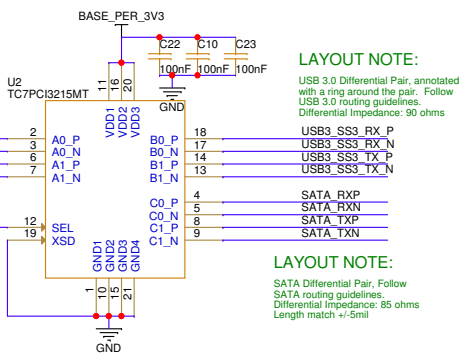
13. USB3, uSATA

SATA/USB select

J1.93-SATA_RXP-USB3_SS3_RX_P
 J1.91-SATA_RXN-USB3_SS3_RX_N
 J1.97-SATA_TXP-USB3_SS3_TX_P
 J1.99-SATA_TXN-USB3_SS3_TX_N

EXP_USB3_SATA_SEL

SEL = LOW: A <-> B
 SEL = HIGH: A <-> C
 XSD = LOW: ON
 XSD = HIGH: OFF
 By default, lines routed to SATA



LAYOUT NOTE:
 USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 85 ohms

LAYOUT NOTE:
 SATA Differential Pair. Follow SATA routing guidelines. Differential Impedance: 85 ohms Length match ~5mil

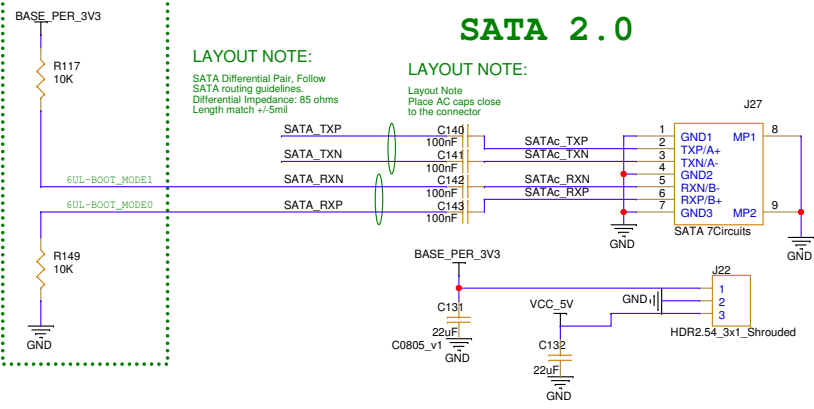
SATA 2.0

LAYOUT NOTE:

SATA Differential Pair, Follow SATA routing guidelines. Differential Impedance: 85 ohms Length match ~5mil

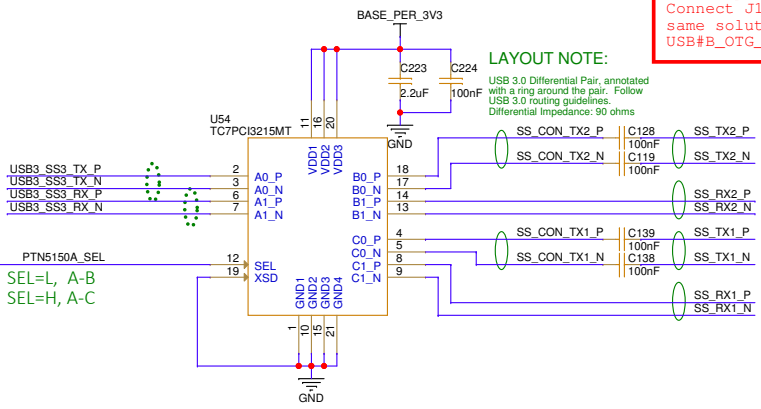
LAYOUT NOTE:

Layout Note Place AC caps close to the connector



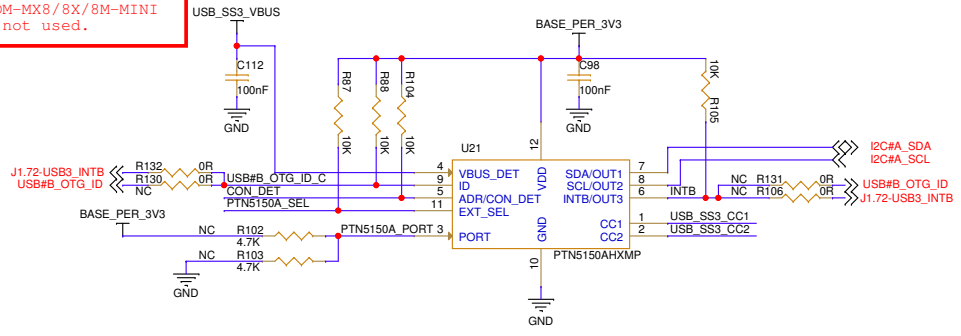
USB TYPE C Circuitry

Usage of native USB_ID for iMX8MP requires patches not included in the formal release, pull up should be to 1.8V. For simple OTG function for VAR-SOM-MX8M-PLUS Connect J1.72 GPIO to U22 PTN ID output - same solution applies also for VAR-SOM-MX8/8X/8M-MINI USB#B_OTG_ID can be left floating if not used.

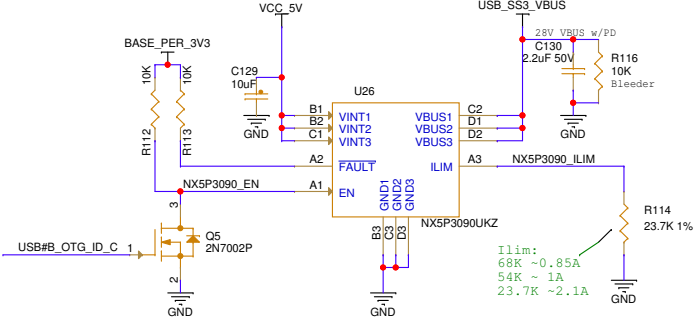


LAYOUT NOTE:
 USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 90 ohms

Config Channel Logic Detection & Indication of Plug Orientation



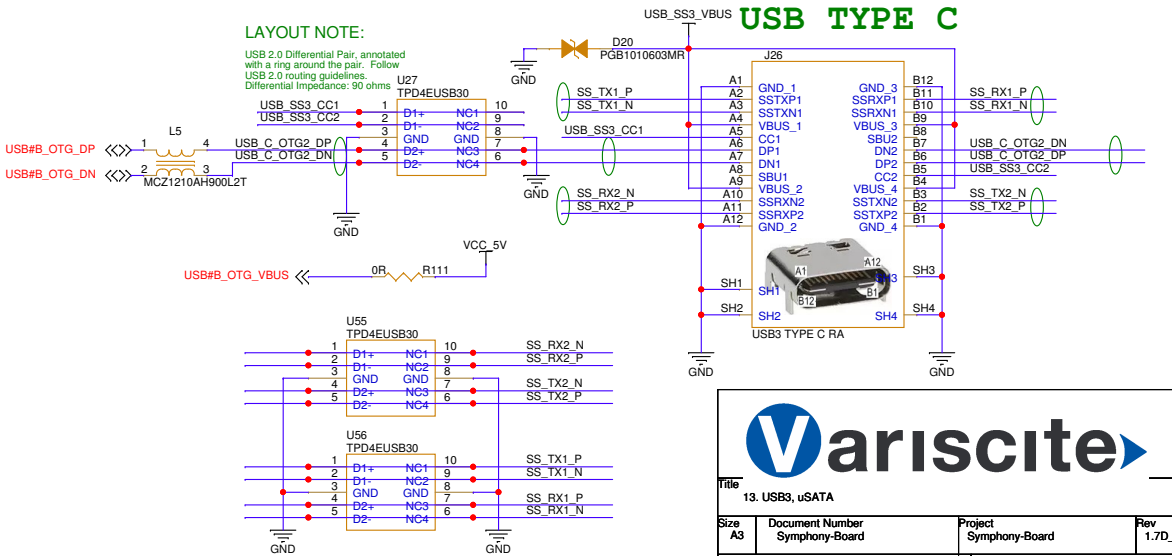
5V Source Load Switch



USB Profile 1 = 5 V @ 2.1 A

LAYOUT NOTE:

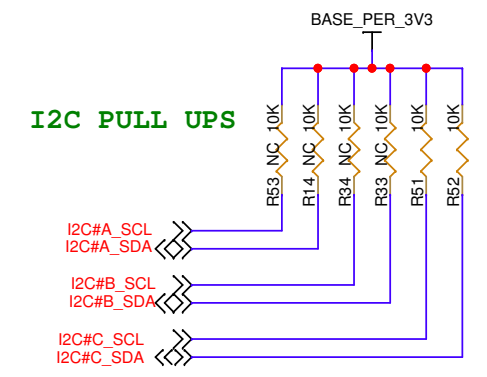
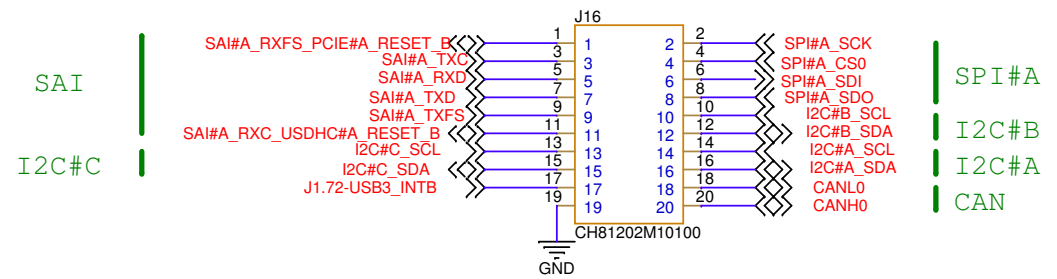
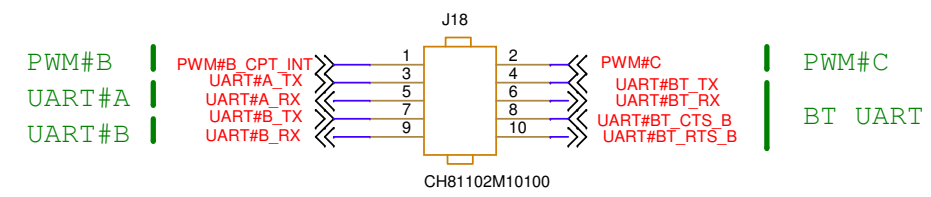
USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines. Differential Impedance: 90 ohms



13. USB3, uSATA			
Size A3	Document Number Symphony-Board	Project Symphony-Board	Rev 1.7D
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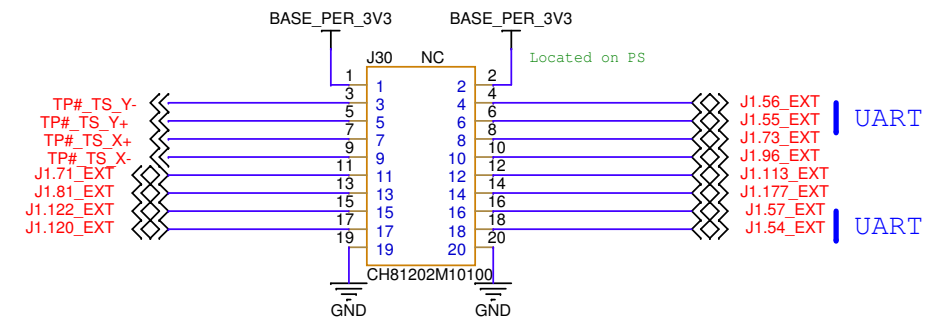
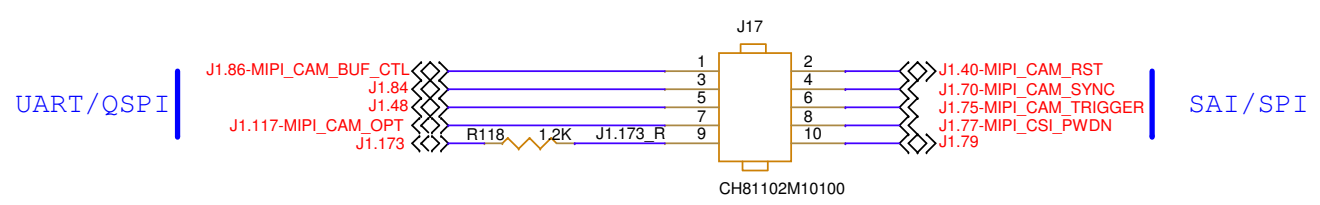
14. Headers

Headers arranged for compatible alternate function



I2C_A has internal pulls in Camera buffer
 I2C_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.
 For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Headers arranged for partial compatible alternate function



COLD RESET ON WDOG_B EVENT for MX6/SOLO and 6UL SOMs

Listed above SOMs require short on headers to get "reboot" to function.
 For all other watch dog looped on SOM

CB_WDOG_B	>>	Symphony Board reset circuitry watch dog input	See J3.17
J1.57_EXT	>>	SOM_6UL: PIN57 WDOG1_B	See J3.11
PWM#B_CPT_INT	>>	MX6/SOLO: PIN68 WDOG1_B	See J18.1

USB#A Host VBUS power control

In order to control the USB#A HOST VBUS power a short is required:

CB-USB#A_HOST_PWR	>>	Symphony Board U22 control input	See J3.12
J1.82-USB#A_HOST_PWR	>>		See J3.18

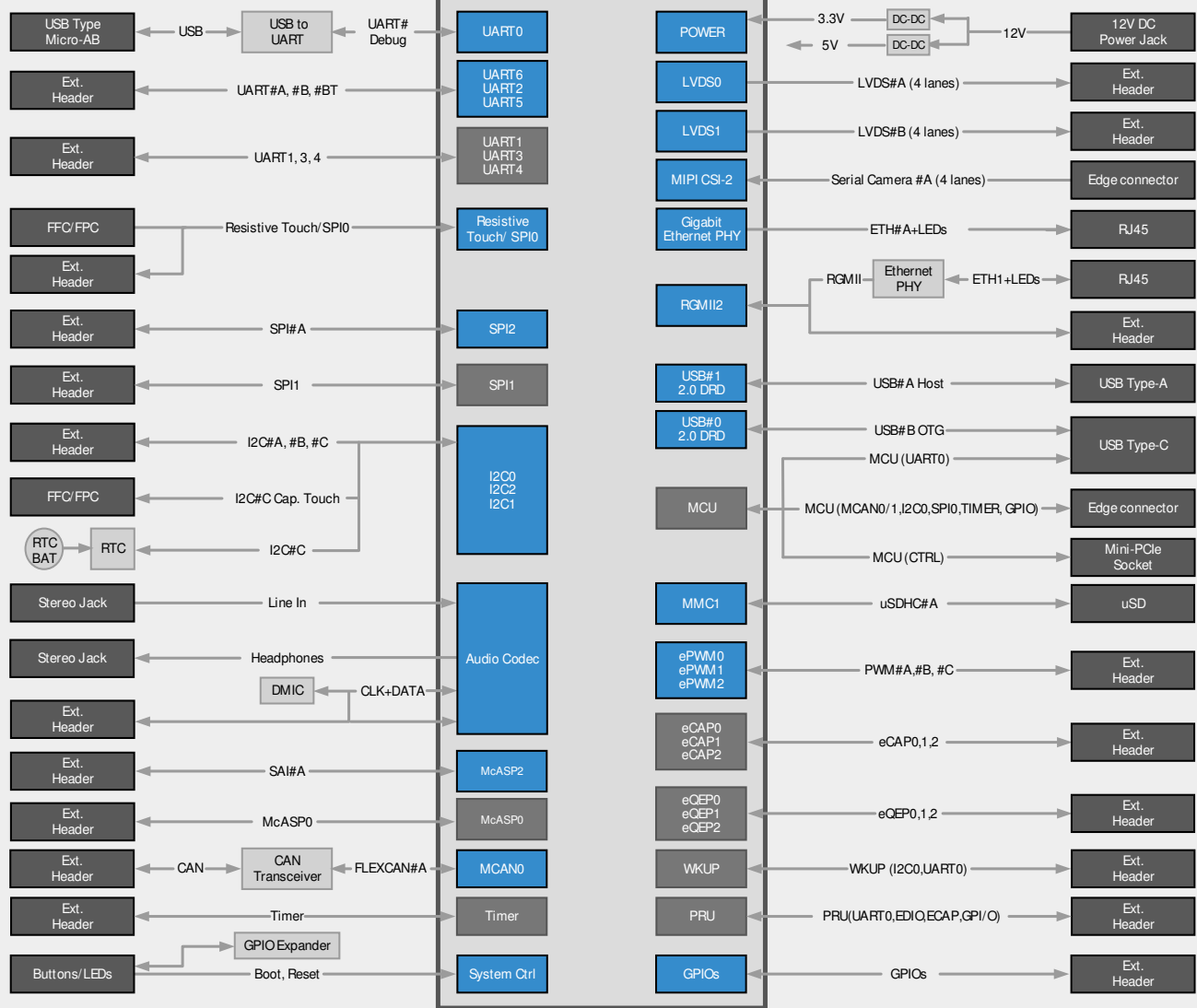
For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS" located at:
ftp://ftp.variscite.com/SOM_Compatibility

Title 14. Headers			
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Designer: Aviad H.		Approved By:	
Date: Sunday, April 06, 2025		Sheet 12 of 24	

02. Block Diagram VAR-SOM-AM62

Symphony-Board Doc rev 1.0

VAR-SOM-AM62



Pin-compatible with other modules from the VAR-SOM Pin2Pin family

No pin2pin compatibility

Title: 02. Block Diagram VAR-SOM-AM62
 Size: A3 | Document Number: Symphony-Board | Project: Symphony-Board | Rev: 1.7D
 Designer: Aviad H. | Approved By: | Date: Sunday, April 06, 2025 | Sheet: 21 of 24

VAR-SOM-AM62

