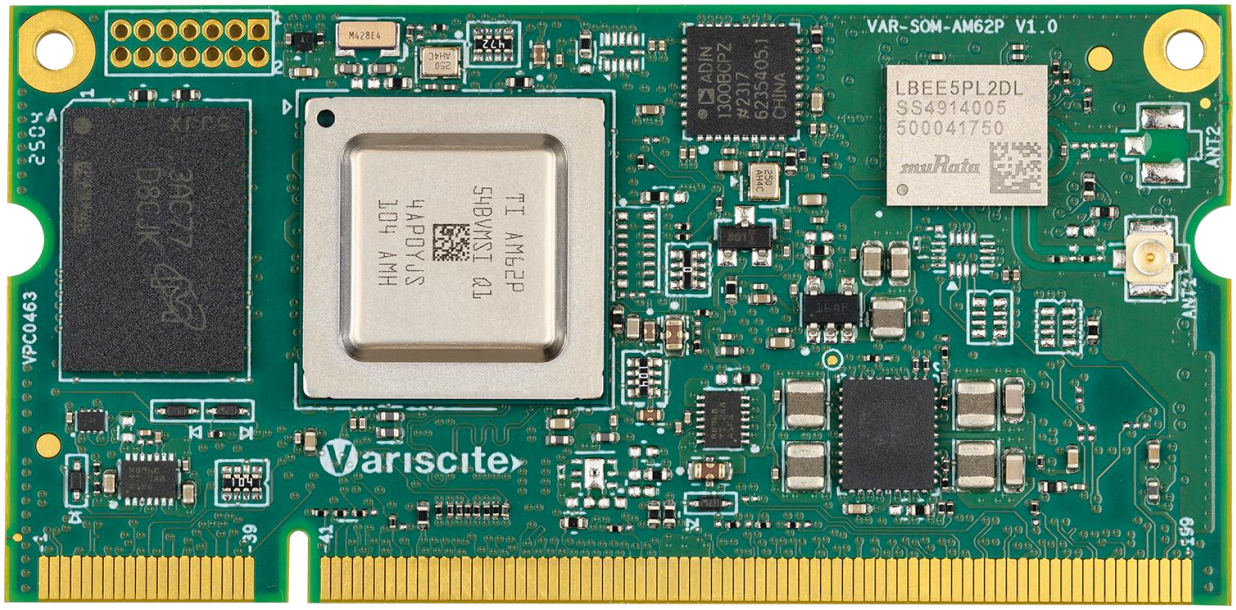
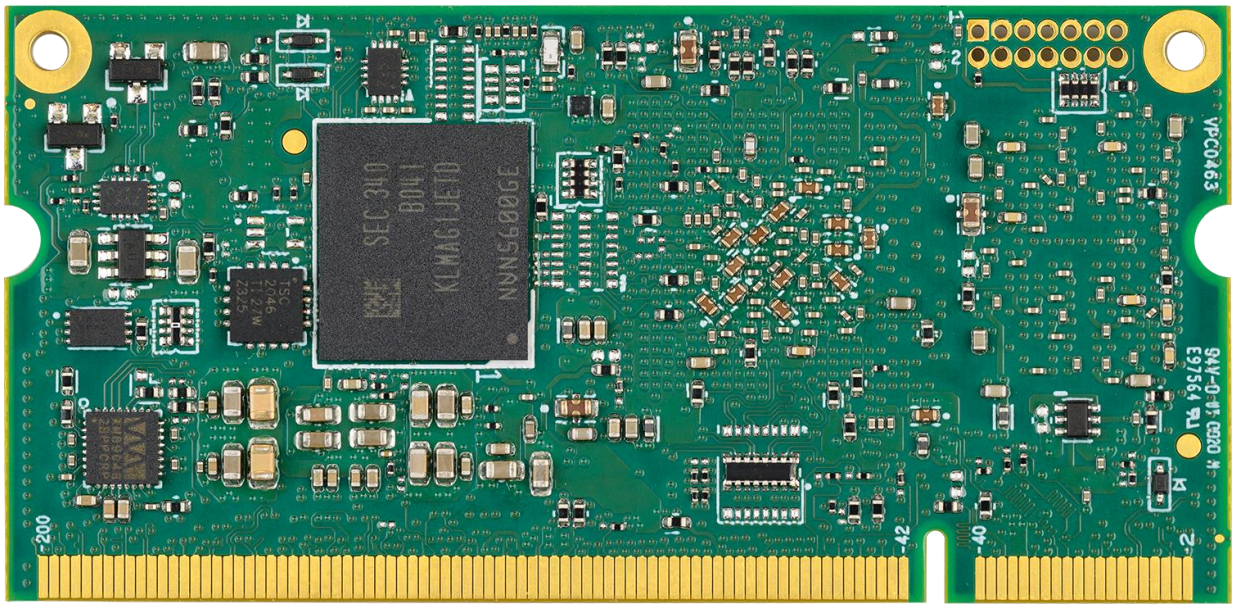
VARISCITE LTD.

VAR-SOM-AM62P V1.x Datasheet

TI Sitara™ AM62Px - based System-on-Module





VARISCITE LTD.

VAR-SOM-AM62P Datasheet

Variscite Ltd.
4, Hamelacha Street
Lod
P.O.B 1121
Airport City, 70100
ISRAEL

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

1. Document Revision History

Revision	Date	Notes
1.0	March 11, 2025	Initial - Preliminary

2. Table of Contents

3. List of Tables

4. Overview

4.1 General Information

The VAR-SOM-AM62P offers a high-performance processing for a low-power System-on-Module. The product is based on the AM62Px Sitara™ MPU family of application processors.

The AM62Px (P = Plus) is an extension of the existing Sitara™ AM62Px low-cost family of application processors built for high-performance embedded 3D display applications. Scalable Arm® Cortex®-A53 performance and embedded features, such as: multi-screen high-definition display support, 3D-graphics acceleration, 4K video acceleration, and extensive peripherals make the AM62Px well-suited for a broad range of automotive and industrial applications, including automotive digital instrumentation, automotive displays, industrial HMI, and
more.

The VAR-SOM-AM62P provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

- Symphony-Board – evaluation board
  - ✓ Carrier Board, compatible with VAR-SOM-AM62P
  - ✓ Schematics
- VAR-DVK-AM62P full development kit, including:
  - ✓ Symphony-Board
  - ✓ VAR-SOM-AM62P
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

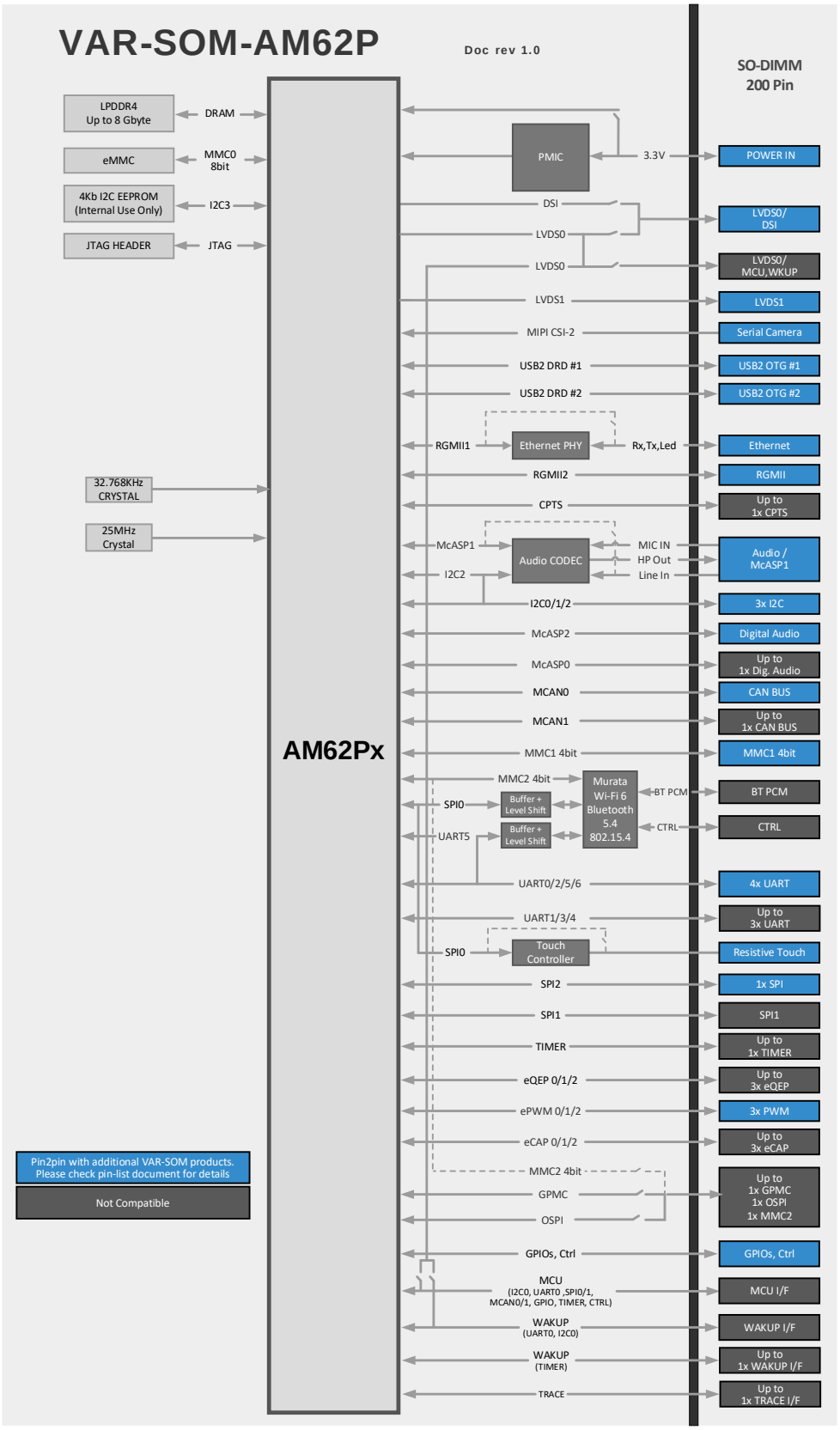
Contact Variscite support services for further information: support@variscite.com.

4.2 Feature Summary

- TI AM62Px Sitara series SOC
  - Up to 4x Cortex A53 @ 1.4 GHz
  - 1x Cortex R5F up to @ 800 MHz (MCU)
  - 1x Cortex R5F up to @ 800 MHz (Device management)
- Graphics Processing Unit
  - 3D GPU with OpenGL ES 3.2 & Vulkan1.2
  - 2D graphics capable
- Memory
  - Up to 8GB LPDDR4-3733
  - 8-bit up to 128GB eMMC boot and storage
- Display Support
  - 2x OLDI/LVDS interface 4-lane each - supporting up to 3840x1080@60fps 24-bit
  - 1x MIPI-DSI 4-lane - supporting up to 3840 x 1080 24-bit
- Networking
  - 2x 10/100/1000 Mbit/s Ethernet Interface
  - Certified Wi-Fi 802.11a/b/g/n/ac/ax
  - Bluetooth: 5.4/BLE
- Camera
  - 1x MIPI CSI-2 – CMOS Serial camera Interface 4 lanes
  - Support for 1,2,3 or 4 data lane mode up to 1.5Gbps per lane
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - Up to 3x Digital audio (McASP)
- USB
  - 2x USB 2.0 Host/Device
- Media and data storage
  - SDIO/MMC
  - OSPI/QSPI
  - GPMC parallel bus
- Other Interfaces
  - Resistive touch controller
  - Serial interfaces (SPI, I2C, UART, ePWM, eCAP, eQEP, CAN-FD, JTAG)
  - GPIOs
- Single power supply: 3.3V
- Dimensions (W x L x H): 67.6 mm x 33 mm x 3.4 mm
- Industrial temperature range: -40°C to 85°C

4.3 Block Diagram

Figure 1 : VAR-SOM-AM62P Block Diagram



5. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-AM62P.

5.1 AM62Px Sitara™ MPU

5.1.1 Overview

The AM62Px (P = Plus) is an extension of the existing Sitara™ AM62x low-cost family of application processors built for high-performance embedded 3D display applications. Scalable Arm® Cortex®-A53 performance and embedded features, such as: multi-screen high-definition display support, 3D-graphics acceleration, 4K video acceleration, and extensive peripherals make the AM62Px well-suited for a broad range of automotive and industrial applications, including automotive digital instrumentation, automotive displays, industrial HMI, and more.

Key features and benefits:

- Focus on innovation and fast development with Linux® and Android™ SDKs accompanied with real-time functional safety and security SDKs.
- Address next wave of HMI designs with new generation of 3D GPU and 4K video acceleration.
- Enhance your design connectivity with an extensive set of automotive and high-speed IOs, including: 4x CAN-FD, 3-port Gigabit Ethernet switch (two external ports) with TSN support, and two USB2.0 ports.
- Supports the latest cybersecurity requirements with the built-in Hardware Security Module (HSM).
- Provides intelligent features, such as: facial recognition and touchless HMI with Arm® Cortex®-A53 CPUs and open-source AI software and tools.

5.1.2 AM62Px Sitara Block Diagram

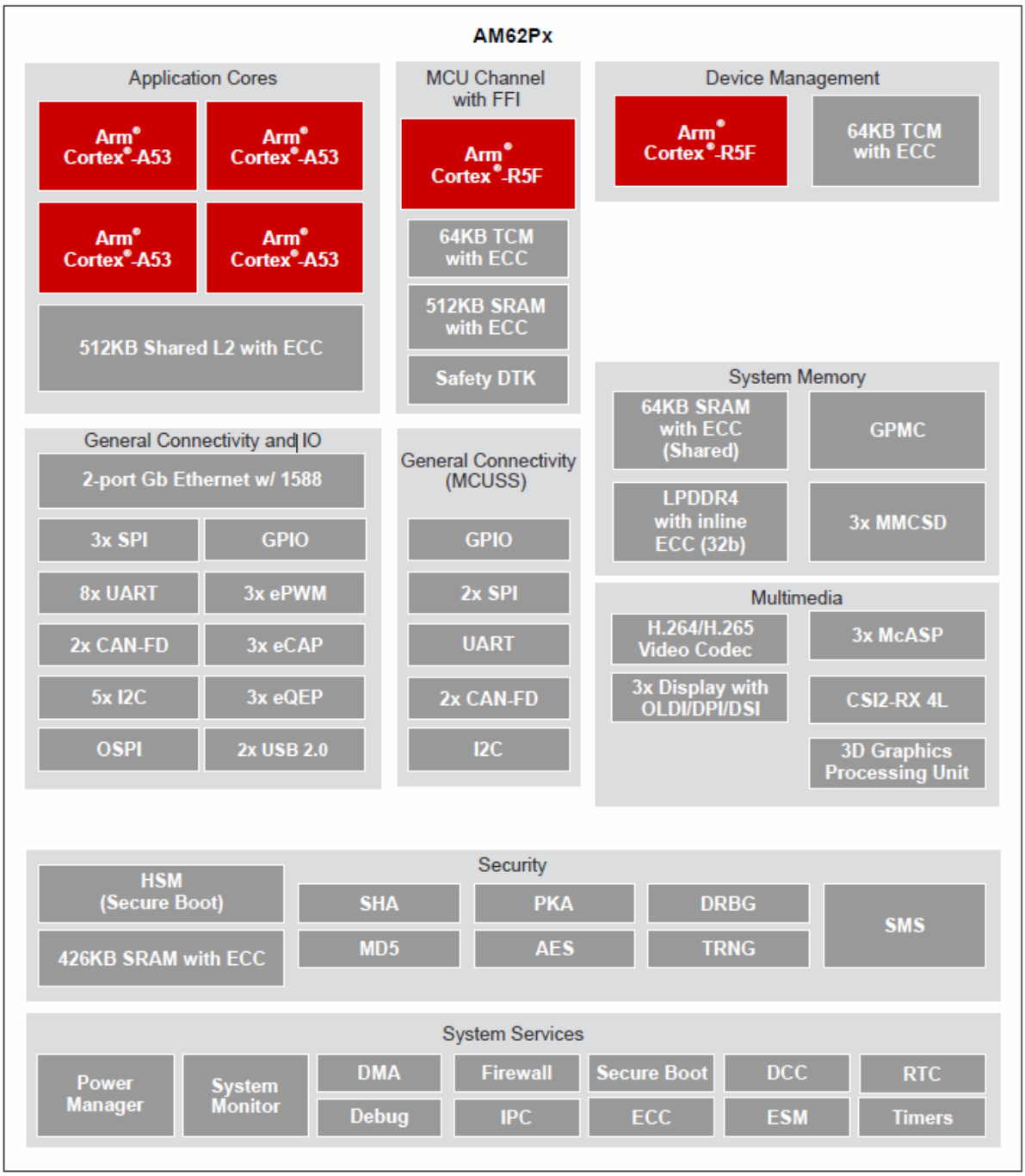


Figure 2 AM62Px Sitara Block Diagram

5.1.3 Arm Cortex-A53 Subsystem (A53SS)

- Up to Quad 64-bit Arm® Cortex®-A53 microprocessor subsystem at up to 1.4GHz
  - Quad-core Cortex-A53 cluster with 512KB L2 shared cache with SECDED ECC
  - Each A53 core has 32KB L1 DCache with SECDED ECC and 32KB L1 ICache with Parity protection

5.1.4 MCU Arm Cortex-R5F Processor (MCU_R5FSS)

- Single-core Arm® Cortex®-R5F at up to 800MHz,integrated as part of MCU Channel with FFI
  - 32KB ICache, 32KB L1 DCache, and 64KB TCM with SECDED ECC on all memories
  - 512KB SRAM with SECDED ECC

The MCU_R5FSS is an Arm® Cortex®-R5F based subsystem that can run safety processing or be used as a general purpose MCU

5.1.5 Arm Cortex-R5F Processor (R5FSS)

- Armv7-R architecture
- R5FSS Memory System
  - 32KB Instruction Cache
    - 4x ways
    - SECDED ECC protected per 64 bits
  - Data Cache
    - 4x ways
    - SECDED ECC protected per 32 bits
  - 64KB tightly-coupled memory (TCM) per CPU
    - SECDED ECC protected per 32 bits
    - TCM hard error cache Implemented in CPU
    - Readable/writable from system
    - 32KB TCMA (ATCM)
    - 16KB TCMB0 (B0TCM)
    - 16KB TCMB1 (B1TCM)
- Full-precision Floating Point (VFPv3)
- 16-region Memory Protection Unit (MPU)
- 8 breakpoints, 8 watch points
- CoreSight Debug Access Port (DAP)
- CoreSight ETM-R5 interface (CTI, ETM)
- Performance Monitoring Unit (PMU)
- 32-bit to 36-bit Region-based Address Translation (RAT) on memory access initiators
- Integrated Vectored Interrupt Manager (VIM) per core with 256 Interrupt Inputs each
  - Programmable interrupt priority (4-bit)
  - Programmable interrupt enable mask
  - Software-generated interrupts
  - Synchronous clock domain crossing on all core interfaces

Note: CORE0 has 64KB of TCM.

5.1.6 Multimedia

- Display subsystem
  - Triple display support over OLDI (LVDS) (1x OLDI-DL, 1x or 2x OLDI-SL), DSI or DPI
    - OLDI-SL (Single Link): up to 1920 x 1080 at 60fps (165MHZ Pixel Clock)
    - OLDI-DL (Dual Link): up to 3840 x 1080 at60fps (150MHz Pixel Clock)
    - MIPI® DSI: with 4 Lane MIPI® D-PHY supports up to 3840 x 1080 at 60fps (300MHz Pixel Clock)
    - DPI (24-bit RGB parallel interface): up to 1920 x 1080 at 60fps (165MHz pixel clock)
  - Four display pipelines with hardware overlay support. A maximum of two display pipelines may be used per display.
  - Supports safety features such as freeze frame detection and data correctness check
- 3D Graphics Processing Unit
  - IMG BXS-4-64 with 256KB cache
  - Up to 50GFLOPS
  - Single shader core
  - OpenGL ES3.2 and Vulkan 1.2 API support
- One Camera Serial Interface (CSI-2) Receiver with 4 Lane D-PHY
  - MIPI® CSI-2 v1.3 Compliant + MIPI D-PHY 1.2
  - Support for 1,2,3 or 4 data lane mode up to 1.5Gbps per lane
  - ECC verification/correction with CRC check + ECC on RAM
  - Virtual Channel support (up to 16)
  - Ability to write stream data directly to DDR via DMA
- Video Encoder/Decoder
  - Support for HEVC (H.265) Main profiles at Level 5.1 High-tier
  - Support for H.264 BaseLine/Main/High Profiles at Level 5.2
  - Support for up to 4K UHD resolution (3840 × 2160)
    - Up to 300MPixels/s operation, with reduced clocking options available for lower power applications with lower performance needs

5.1.7 Memory Subsystem:

- Up to 1.09MB of On-chip RAM
  - 64KB of On-Chip RAM (OCRAM) with SECDED ECC, can be divided into smaller banks in increments of 32KB for as many as
  - 2 separate memory banks 256KB of On-Chip RAM with SECDED ECC in SMS Subsystem
  - 176KB of On-Chip RAM with SECDED ECC in SMS Subsystem for TI security firmware
  - 512KB of On-chip RAM with SECDED ECC in Cortex-R5F MCU Subsystem
  - 64KB of On-chip RAM with SECDED ECC in Device Manager Subsystem
- DDR Subsystem (DDRSS)
  - Supports LPDDR4 memory type
  - 32-bit data bus with inline ECC
  - Supports speeds up to 3733MT/s
  - Max size of 8GB

5.1.8 Functional Safety

- Functional Safety-Compliant targeted [Industrial]
  - Developed for functional safety applications
  - Documentation will be available to aid IEC 61508 functional safety system design
  - Systematic capability up to SIL 3 targeted
  - Hardware Integrity up to SIL 2 targeted
  - Safety-related certification
    - IEC 61508 by TUV SUD planned
- Functional Safety-Compliant targeted [Automotive]
  - Developed for functional safety applications
  - Documentation will be available to aid ISO 26262 functional safety system design
  - Systematic capability up to ASIL D targeted
  - Hardware integrity up to ASIL B targeted
  - Safety-related certification
    - ISO 26262 by TÜV SÜD planned
- AEC-Q100 qualified [Automotive]

5.1.9 Security

- Secure boot supported
  - Hardware-enforced Root-of-Trust (RoT)
  - Support to switch RoT via backup key
  - Support for takeover protection, IP protection, and anti-roll back protection
- Trusted Execution Environment (TEE) supported
  - Arm TrustZone® based TEE
  - Extensive firewall support for isolation
  - Secure watchdog/timer/IPC
  - Secure storage support
  - Replay Protected Memory Block (RPMB) support
- Dedicated Security Controller with user programmable HSM core and dedicated security DMA & IPC subsystem for isolated processing
- Cryptographic acceleration supported
  - Session-aware cryptographic engine with ability to auto-switch key-material based on incoming data stream
  - Supports cryptographic cores
    - AES – 128-/192-/256-Bit key sizes
    - SHA2 – 224-/256-/384-/512-Bit key sizes
    - DRBG with true random number generator
    - PKA (Public Key Accelerator) to Assist in RSA/ECC processing for secure boot
- Debugging security
  - Secure software controlled debug access
  - Security aware debugging

5.1.10 High-Speed Interfaces

- Integrated Ethernet switch supporting (total 2 external ports)
    - RMII (10/100) or RGMII (10/100/1000)
    - IEEE1588 (Annex D, Annex E, Annex F with 802.1AS PTP)
    - Clause 45 MDIO PHY management
    - Packet Classifier based on ALE engine with 512 classifiers
    - Priority based flow control
    - Time sensitive networking (TSN) support
    - Four CPU H/W interrupt Pacing
    - IP/UDP/TCP checksum offload in hardware
- Two USB2.0 Ports
    - Port configurable as USB host, USB peripheral, or USB Dual-Role Device (DRD mode)
    - Integrated USB VBUS detection

5.1.11 General Connectivity

- 9x Universal Asynchronous Receiver-Transmitters (UART)
- 5x Serial Peripheral Interface (SPI) controllers
- 5x Inter-Integrated Circuit (I2C) ports
- 3x Multichannel Audio Serial Ports (McASP)
    - Transmit and Receive Clocks up to 50 MHz
    - Up to 4/6/16 Serial Data Pins across 3x McASP with Independent TX and RX Clocks
    - Supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and Similar Formats
    - Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 Formats)
    - FIFO Buffers for Transmit and Receive (256 Bytes)
    - Support for audio reference output clock
- 3x enhanced PWM modules (ePWM)
- 3x enhanced Quadrature Encoder Pulse modules (eQEP)
- 3x enhanced Capture modules (eCAP)
- General-Purpose I/O (GPIO), All LVCMOS I/O can be configured as GPIO
- 4x Controller Area Network (CAN) modules with CAN-FD support
    - Conforms w/ CAN Protocol 2.0 A, B and ISO11898-1
    - Full CAN FD support (up to 64 data bytes)
    - Parity/ECC check for Message RAM
    - Speed up to 8Mbps

5.1.12 Media and Data Storage

- 3x Multi-Media Card/Secure Digital® (MMC/SD®/SDIO) interfaces
    - 1x 8-bit eMMC interface up to HS400 speed
    - 2x 4-bit SD/SDIO interfaces up to UHS-I
    - Compliant with eMMC 5.1, SD 3.0, and SDIO Version 3.0
- 1× General-Purpose Memory Controller (GPMC) up to 133 MHz
    - Flexible 8- and 16-bit Asynchronous Memory Interface with up to four Chip (22-bit address) Selects (NAND)
    - Uses BCH Code to Support 4-, 8-, or 16-BitECC
    - Uses Hamming Code to Support 1-Bit ECC
    - Error Locator Module (ELM)

        - Used With the GPMC to Locate Addresses of Data Errors From Syndrome Polynomials Generated Using a BCH Algorithm
        - Supports 4-, 8-, and 16-Bit Per 512-Byte Block Error Location Based on BCH Algorithms
- OSPI/QSPI with DDR / SDR support
    - Support for Serial NAND and Serial NOR flash devices
    - 4GBytes memory address support
    - XIP mode with optional on-the-fly encryption

5.1.13 Power Management

- Low-power modes supported by Device Manager:
    - Partial IO support for CAN/GPIO/UART wakeup
    - I/O Only + DDR in Self Refresh for Suspend to RAM
    - DeepSleep
    - MCU Only
    - Standby
    - Dynamic frequency scaling

5.2 Memory

5.2.1 RAM

The VAR-SOM-AM62P is available with up to 8 GB of DDR4-3733 memory.

5.2.2 Non-volatile Storage Memory

The VAR-SOM-AM62P is available with a non-volatile MLC eMMC storage memory with optional densities of up to 128GB. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.

5.3 Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4 Wi-Fi + BT + LR-WPAN

The VAR-SOM-AM62P module can be assembled with one of the following Wi-Fi modules:

- Murata Type 2EL - 2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Module based on NXP IW612 chipset
- Murata Type 2DL -2.4GHz & 5GHz Wi-Fi® + Bluetooth® Module based on NXP IW611 chipset

Both realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port or may be ordered with dual antenna ports.
The SOM can be ordered with 802.15.4 low-rate wireless personal area network (LR-WPAN)

5.4.1 Murata Type 2EL/2DL Module

Wi-Fi Key Features:

- 1x1 2.4/5 GHz, up to 80 MHz channel
- UL/DL MU-MIMO and OFDMA
- Target Wake Time, Dual Carrier Modulation, Extended Range
- 802.11az accurate ranging
- WPA3 security

Bluetooth Key Features:

- Supports Bluetooth 5.4
- Integrated high power PA up to +20 dBm transmit power
- Full featured Bluetooth baseband
- SCO/eSCO links with hardware accelerated audio signal processing
- Bluetooth LE 2 Mbit/s, Long Range, Advertising Extensions
- LE Audio with Isochronous channels (I2S/PCM)

802.15.4 Key Features (available in 2EL Only):

- IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band
- Integrated high power PA up to +20 dBm transmit power
- Shared transmitter and antenna pin with Bluetooth
- Simultaneous receive with Bluetooth

One of the two options can be assembled:

5.4.1.1 VAR-SOM-MX8M-MINI 2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Option (WBE)

The VAR-SOM-MX8M-MINI contains Murata's certified high-performance Type 2EL Module based upon the NXP IW612 chipset supporting Wi-Fi® 11a/b/g/n/ac/ax + Bluetooth® 5.4 + 802.15.4 wireless connectivity.

5.4.1.2 VAR-SOM-MX8M-MINI 2.4GHz & 5GHz Wi-Fi® + Bluetooth® Option (WBD)

The VAR-SOM-MX8M-MINI contains Murata's certified high-performance Type 2DL Module based upon the NXP IW611 chipset supporting Wi-Fi® 11a/b/g/n/ac/ax + Bluetooth® 5.4 wireless connectivity.

5.5 PMIC

The VAR-SOM-AM62P features TI's TPS6522430 chip as a Power Management Integrated circuit (PMIC) designed specifically for use with TI's AM62Px Sitara family of application processors. The TPS6522430 regulates power rails required on SOM from a single 3.3V power supply.
The PMIC is programmable via the I2C interface and associated register map.

5.6 10/100/1000 Mbps Ethernet Transceiver

The VAR-SOM-AM62P features on board an Integrated Ethernet Transceiver Analog Devices ADIN1300.

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.
- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover
- Auto-negotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

5.7 Resistive Touch Controller (TSC2046)

The VAR-SOM-AM62P features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

5.8 EEPROM

The SOM uses a serial EEPROM to store memory calibration and manufacturing parameters.
This EEPROM is connected to I2C3 bus and intended only for holding the above information.
The SOM may not boot if the contents of EEPROM device are corrupted.

6. VAR-SOM-AM62P Hardware Configuration

The table below lists the Hardware configurations options orderable for the VAR-SOM-AM62P.

Table 1 Hardware Configuration Options

Option	Description
EC	Ethernet PHY assembled on SOM, 2nd Ethernet port always available over RGMII2/RMII2
AC	Audio Codec assembled on SOM
WBE	2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Module assembled on SOM (Murata 2EL) Available only when TP option is not assembled [1]
WBD	2.4GHz & 5GHz Wi-Fi® + Bluetooth® Module assembled on SOM (Murata 2DL)
BTPCM	In WBE or WBD configuration, expose Bluetooth® PCM lines [2]
RFCNTL	In WBE or WBD configuration, expose 2.4GHz & 5GHz Wi-Fi® RF_CNTL lines [2]
COEX	In WBE or WBD configuration, expose WCI-2 coexistence management lines [2]
ANT2	In WBE or WBD configuration, Dual antenna mode. ANT1 for Wi-Fi, ANT2 for BT and 802.15.4 [2]
TP	Resistive Touch controller assembled on SOM (note: capacitive touch is always available via I2C)
DSI	DSI bus signals are exported via SOM connector pins instead of LVDS0 signals
LD0	In DSI configuration, optional export of LVDS0 bus signals via SOM connector pins instead of MCU/WKUP signals.
GPMC/ OSPI/ MMC2	OSPI – Extra Octal/Quad SPI signals exported via SOM connector pins GPMC – Parallel bus signals exported via SOM connector pins MMC2 – Additional SD/MMC2 signals exported via SOM connector pins, available only when Wi-Fi/BT chip is not assembled
RG2CM	Switching from the default 3.3V to 1.8V over RGMII2/RMII2, RGMII1/RMII1 signals exported via SOM

NOTE

[1] The utilization of the same SPI channel by WBE and TP assembly choices makes it unfeasible to assemble them simultaneously.
[2] This assembly option was not tested yet; for further support, please contact sales@variscite.com

Note: Other orderable options are available and are not part of this datasheet.
Please refer to Variscite official website for full list of configuration options.

7. External Connectors

7.1 Board to Board Connector

The VAR-SOM-AM62P exposes a 200-pin SO-DIMM connector.

- The recommended mating connectors for baseboard interfacing are:
  1. Concraft - 0701A0BE52E
  2. Tyco Electronics -1565917-4

7.2 Wi-Fi & BT Connector

- Modules with Wi-Fi ***"WBD", "WBE" Configuration*** **-** a combined Wi-Fi + BT antenna connector is assembled.
- In case of Modules with Wi-Fi ***"WBD", "WBE" Configuration & "ANT2" Configuration*** **-** dual Antenna connectors are assembled.
- Connector type: U.FL JACK connector
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 JTAG Header

In addition to the 200-pin SO-DIMM interface, the SOM exposes JTAG interface via an optional header.

7.4 VAR-SOM-AM62P Connector Pin-out

Table 2: VAR-SOM-AM62P J1 Pinout

Pin	Assembly	Pin name	Notes	GPIO	Ball
1	no EC	RGMII1_TX_CTL	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	GPIO0_73	B18
1	EC	NC	With "EC" configuration this pin is Not Connected		NC
2		GND	Digital Ground		GND
3	no EC	RGMII1_TD3	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_78	C16
3	EC	ETH0_MDI_A_P	Signal source is Ethernet PHY		ADIN1300.12
4	no EC	RGMII1_RD0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_81	B15
4	EC	ETH0_MDI_C_P	Signal source is Ethernet PHY		ADIN1300.16
5	no EC	RGMII1_TD2	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_77	A17
5	EC	ETH0_MDI_A_M	Signal source is Ethernet PHY		ADIN1300.13
6	no EC	RGMII1_RD1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_82	B16
6	EC	ETH0_MDI_C_M	Signal source is Ethernet PHY		ADIN1300.17
7		GND	Digital Ground		GND
8		GND	Digital Ground		GND
9	no EC	RGMII1_TD1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_76	C17
9	EC	ETH0_MDI_B_P	Signal source is Ethernet PHY		ADIN1300.14
10	no EC	RGMII1_RD2	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_83	A14
10	EC	ETH0_MDI_D_P	Signal source is Ethernet PHY		ADIN1300.18
11	no EC	RGMII1_TD0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_75	A18
11	EC	ETH0_MDI_B_M	Signal source is Ethernet PHY		ADIN1300.15
12	no EC	RGMII1_RD3	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_84	B14
12	EC	ETH0_MDI_D_M	Signal source is Ethernet PHY		ADIN1300.19
13		GND	Digital Ground		GND
14		GND	Digital Ground		GND
15	no EC	RGMII1_RX_CTL	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_79	A15
15	EC	ETH0_LED_ACT	Signal source is Ethernet PHY		ADIN1300.21

Pin	Assembly	Pin name	Notes	GPIO	Ball
16	no EC	RGMII1_RXC	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series EMI filter;	GPIO0_80	A16
16	EC	ETH0_LED_LINK_10_100_1000	Signal source is Ethernet PHY		ADIN1300.26 via inv. FET
17		MCASP0_AXR1		GPIO1_9	E24
18	no AC & no GPMC	GPMC0_WEN	Available in SOM without "AC" and without "GPMC" configuration	GPIO0_34	T25
18	no AC & GPMC	NC	Signal source is Audio Codec		NC
18	AC	DMIC_CLK	Signal source is Audio Codec		WM8904.1
19		GND	Digital Ground		GND
20	no AC & no GPMC	GPMC0_WPN	Available in SOM without "AC" and without "GPMC" configuration	GPIO0_39	P24
20	no AC & GPMC	NC	Signal source is Audio Codec		NC
20	AC	DMIC_DATA	Signal source is Audio Codec		WM8904.27
21		GPMC0_AD10	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_25	AA25
22		GPMC0_AD15	BOOTMODE15 pin, has 100K PU on SOM for compatibly with VAR-SOM-AM62; For boot enablement, Pin is Pulled low internally on SOM during boot. Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_30	AC24
23		GPMC0_AD14	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_29	AB24
24		GPMC0_AD12	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_27	Y24
25		GPMC0_AD13	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_28	AD25
26		GPMC0_AD11	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_26	W24
27		GND	Digital Ground		GND
28		GND	Digital Ground		GND
29		EXT_REFCLK1		GPIO1_30	C25
30		MDIO0_MDIO	Pin is referenced to 3.3V, and has an internal 1.47K Pull Up. In "RG2CM" configuration pin is routed via on SOM 1.8<->3.3V voltage translator. Do not alter pinmux with "EC" configuration	GPIO0_85	F16
31	no GPMC & no OSPI & no MMC2	NC			NC
31	GPMC & no MMC2 & no OSPI	GPMC0_AD0	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_15	U22
31	OSPI & no MMC2 & no GPMC	OSPI_CLK	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_0	P23
31	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_DAT3	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_65	L21
32		VCC_SOM	SOM Power		VCC_SOM
33	no GPMC & no OSPI & no MMC2	NC			NC

Pin	Assembly	Pin name	Notes	GPIO	Ball
33	GPMC & no MMC2 & no OSPI	GPMC0_AD1	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_16	U21
33	OSPI & no MMC2 & no GPMC	OSPI0_LBCLKO	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_1	N23
33	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_DAT2	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_66	L20
34		VCC_SOM	SOM Power		VCC_SOM
35	no GPMC & no OSPI & no MMC2	NC			NC
35	GPMC & no MMC2 & no OSPI	GPMC0_DIR	Available in SOM with "GPMC" configuration;	GPIO0_40	P25
35	OSPI & no MMC2 & no GPMC	OSPI0_D1	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_4	N24
35	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_DAT1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_67	K22
36	no GPMC & no OSPI & no MMC2	VCC_SOM	SOM Power		VCC_SOM
36	GPMC & no MMC2 & no OSPI	GPMC0_OEN_REN	Available in SOM with "GPMC" configuration;	GPIO0_33	R24
36	OSPI & no MMC2 & no GPMC	OSPI0_DQS	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_2	P22
36	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	VDDSHV6	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)		1B10
37		GND	Digital Ground		GND
38		NC			NC
39		MCASP0_AFSR		GPIO1_13	G23
40		GPMC0_AD7	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_22	W25
41		MCASP0_AXR2		GPIO1_8	E25
42		BOOT_SEL	Controls internal OR external boot source; Internal signal pulled up to SOM_PGOOD using 1K resistor;		BOOT_SEL
43		MCASP0_ACLKR		GPIO1_14	G20
44		MCAN0_TX		GPIO1_24	B23
45		MCASP0_AXR3		GPIO1_7	D25
46		MCAN0_RX		GPIO1_25	F20
47	no GPMC & no OSPI & no MMC2	GND	Digital Ground		GND
47	GPMC & no MMC2 & no OSPI	GPMC0_BE1N	Available in SOM with "GPMC" configuration;	GPIO0_36	T24

Pin	Assembly	Pin name	Notes	GPIO	Ball
47	OSPI & no MMC2 & no GPMC	OSPI0_CSN3	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_14	L23
47	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_SDCD	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_71	J25
48		GPMC0_AD5	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_20	T21
49		SOM_PGOOD	SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw allowed.		SOM_PGOOD
50		VOUT0_DATA12	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	GPIO0_57	AD21
51		VOUT0_DATA13	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	GPIO0_58	AC21
52		VOUT0_DATA7	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	GPIO0_52	AE23
53		VOUT0_DATA6	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	GPIO0_51	AC23
54		RGMII2_RD3	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO1_6	C19
55		RGMII2_TD3	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO1_0	A19
56		RGMII2_TD2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_91	D17
57		RGMII2_RXC	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO1_2	D19
58	no BTPCM	MCU_UART0_CTSN		MCU_GPIO0_7	B8
58	BTPCM	BT_PCM_IN_1V8	Available in SOM with "BTPCM" configuration;		LBES5PL2xL.93
59	no GPMC & no OSPI & no MMC2	GND	Digital Ground		GND
59	GPMC & no MMC2 & no OSPI	GPMC0_CLK	Available in SOM with "GPMC" configuration;	GPIO0_31	Y25
59	OSPI & no MMC2 & no GPMC	OSPI0_D3	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_6	M24
59	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_SDWP	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_72	K25
60		MMC1_CLK	Bank voltage set on SOM 1.8V/3.3V	GPIO1_46	J24
61		MMC1_DAT2	Bank voltage set on SOM 1.8V/3.3V	GPIO1_43	H22
62		MMC1_DAT0	Bank voltage set on SOM 1.8V/3.3V	GPIO1_45	H21
63		MMC1_DAT1	Bank voltage set on SOM 1.8V/3.3V	GPIO1_44	H23
64		MMC1_CMD	Bank voltage set on SOM 1.8V/3.3V	GPIO1_47	H20
65		MMC1_DAT3	Bank voltage set on SOM 1.8V/3.3V	GPIO1_42	H25
66		GND	Digital Ground		GND
67		GND	Digital Ground		GND
68		SPI0_CS1		GPIO1_16	E20

Pin	Assembly	Pin name	Notes	GPIO	Ball
69		MCASP0_AXR0		GPIO1_10	F23
70		OSPI0_D6	Pin referenced to 1.8V in SOM with "OSPI" configuration;	GPIO0_9	P21
71		RGMII2_RD2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO1_5	E17
72		MCASP0_AFSX		GPIO1_12	F25
73		RGMII2_TD0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_89	B19
74		MDIO0_MDC	Pin is referenced to 3.3V. In "RG2CM" configuration pin is routed via on SOM 1.8<->3.3V voltage translator; Do not alter pinmux with "EC" configuration	GPIO0_86	F17
75		OSPI0_D5	Pin referenced to 1.8V in SOM with "OSPI" configuration;	GPIO0_8	N22
76	no GPMC & no OSPI & no MMC2	GND	Digital Ground		GND
76	GPMC & no MMC2 & no OSPI	GPMC0_AD2	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_17	U20
76	OSPI & no MMC2 & no GPMC	OSPI0_D0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_3	L25
76	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_CLK	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_69	K21
77		OSPI0_D7	Pin referenced to 1.8V in SOM with "OSPI" configuration;	GPIO0_10	N20
78		GND	Digital Ground		GND
79		OSPI0_D4	Pin referenced to 1.8V in SOM with "OSPI" configuration;	GPIO0_7	N21
80		MMC1_SDCD	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	GPIO1_48	D23
81		RGMII2_RD1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO1_4	E16
82		USB1_DRVVBUS		GPIO1_51	G21
83		UART0_RXD	Used as debug UART on Variscite base board	GPIO1_20	A22
84		GPMC0_AD4	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_19	T20
85		UART0_TXD	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	GPIO1_21	B22
86		GPMC0_AD6	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_21	V24
87		I2C0_SDA		GPIO1_27	A24
88		I2C0_SCL		GPIO1_26	B25
89		GND	Digital Ground		GND
90		I2C1_SDA		GPIO1_29	B24
91	no BTPCM	MCU_UART0_RXD		MCU_GPIO0_5	B6
91	BTPCM	BT_PCM_CLK_1V8	Available in SOM with "BTPCM" configuration;		LBES5PL2xL.57
92		I2C1_SCL		GPIO1_28	C24
93	no BTPCM	MCU_UART0_RTSN		MCU_GPIO0_8	B7

Pin	Assembly	Pin name	Notes	GPIO	Ball
93	BTPCM	BT_PCM_OUT_1V8	Available in SOM with "BTPCM" configuration;		LBES5PL2xL.59
94		USB0_DRVVBUS		GPIO1_50	G22
95		GND	Digital Ground		GND
96		RGMII2_TXC	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series 33R resistor;	GPIO0_88	D16
97	no EC	RGMII1_TXC	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series 33R resistor;	GPIO0_74	B17
97	EC	NC	With "EC" configuration this pin is Not Connected		NC
98		SYS_NRSTIN_3V3	SOM reset input pin. Internally pulled up. Connected via diode to internal (not exposed) 1.8V MCU_PORz ball. Once it is asserted low, CPU MCU and MAIN domains perform cold reset.		H6 (via diode)
99	no BTPCM	MCU_UART0_TXD		MCU_GPIO0_6	C8
99	BTPCM	BT_PCM_SYNC_1V8	Available in SOM with "BTPCM" configuration;		LBES5PL2xL.61
100	no GPMC & no OSPI & no MMC2	NC			NC
100	GPMC & no MMC2 & no OSPI	GPMC0_CSN0	Available in SOM with "GPMC" configuration;	GPIO0_41	T23
100	OSPI & no MMC2 & no GPMC	OSPI0_D2	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_5	N25
100	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_CMD	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_70	K24
101		GND	Digital Ground		GND
102	no GPMC & no OSPI & no MMC2	NC			NC
102	GPMC & no MMC2 & no OSPI	GPMC0_CSN1	Available in SOM with "GPMC" configuration;	GPIO0_42	U23
102	OSPI & no MMC2 & no GPMC	OSPI0_CSN0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	GPIO0_11	M25
102	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_DAT0	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	GPIO0_68	K23
103		VCC_SOM	SOM Power		VCC_SOM
104		USB1_VBUS			Y10
105		VCC_SOM	SOM Power		VCC_SOM
106		USB0_VBUS			Y7
107		VCC_SOM	SOM Power		VCC_SOM
108		USB1_DM			AE10
109		VCC_SOM	SOM Power		VCC_SOM
110		USB1_DP			AE9
111		VCC_SOM	SOM Power		VCC_SOM

Pin	Assembly	Pin name	Notes	GPIO	Ball
112		GND	Digital Ground		GND
113		RGMII2_TX_CTL	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_87	A20
114		USB0_DM			AE8
115		GPMC0_AD8	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_23	AC25
116		USB0_DP			AE7
117		MCASP0_ACLKX		GPIO1_11	F24
118		GND	Digital Ground		GND
119		CSI0_RXP0			AB10
120		RGMII2_RX_CTL	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO1_1	F19
121		CSI0_RXN0			AB11
122		RGMII2_RD0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO1_3	E19
123		CSI0_RXN1			AC10
124		MMC1_SDWP		GPIO1_49	D24
125		CSI0_RXP1			AC9
126		GND	Digital Ground		GND
127		CSI0_RXP2			AA9
128		MCU_RESETSTATZ		MCU_GPIO0_21	F14
129		CSI0_RXN2			AA10
130		MCU_RESETZ			F11
131		CSI0_RXN3			AD9
132		GND	Digital Ground		GND
133		CSI0_RXP3			AD8
134		RESET_REQZ			G24
135		CSI0_RXCLKP			AE11
136		MCU_ERRORN	Pin is referenced to 1.8V; Connected also to PMIC via on SOM 1.8<->3.3V voltage translator		G6
137		CSI0_RXCLKN			AE12
138		GND	Digital Ground		GND
139		GND	Digital Ground		GND
140	no LD0	WKUP_I2C0_SCL	Used for WKUP_I2C function, connected also to PMIC	MCU_GPIO0_19	A13
140	DSI & LD0	OLDI0_A0N	Available in SOM with “DSI” and LD0” configuration;		AE20
141	no LD0	WKUP_I2C0_SDA	Used for WKUP_I2C function, connected also to PMIC	MCU_GPIO0_20	C11
141	DSI & LD0	OLDI0_A1N	Available in SOM with “DSI” and LD0” configuration;		AC19
142	no LD0	WKUP_UART0_CTSN		MCU_GPIO0_11	C7
142	DSI & LD0	OLDI0_A0P	Available in SOM with “DSI” and LD0” configuration;		AD20
143	no LD0	WKUP_UART0_RTSN		MCU_GPIO0_12	C6
143	DSI & LD0	OLDI0_A1P	Available in SOM with “DSI” and LD0” configuration;		AD19
144		GND	Digital Ground		GND

Pin	Assembly	Pin name	Notes	GPIO	Ball
145	no LD0	WKUP_UART0_RXD		MCU_GPIO0_9	D8
145	DSI & LD0	OLDI0_A2N	Available in SOM with “DSI” and LD0” configuration;		AA19
146	no COEX	MCU_I2C0_SCL	Used for MCU_I2C function, connected also to PMIC	MCU_GPIO0_17	E11
146	COEX	COEX_SIN_1V8	Available in “COEX” and “WBE” or ”WBD” configuration. Signal source is WIFI module, connected to “WCI-2_SIN” signal. Pin referenced to 1.8V.		LBES5PL2xL.69
147	no LD0	WKUP_UART0_TXD		MCU_GPIO0_10	D7
147	DSI & LD0	OLDI0_A2P	Available in SOM with “DSI” and LD0” configuration;		AB19
148	no COEX	MCU_I2C0_SDA	Used for MCU_I2C function, connected also to PMIC	MCU_GPIO0_18	D11
148	COEX	COEX_SOUT_1V8	Available in “COEX” and “WBE” or ”WBD” configuration. Signal source is WIFI module, connected to “WCI-2_OUT” signal, Pin referenced to 1.8V		LBES5PL2xL.70
149		GND			GND
150	no LD0	MCU_SPI0_CLK		MCU_GPIO0_2	C10
150	DSI & LD0	OLDI0_CLK0N	Available in SOM with “DSI” and LD0” configuration;		AE18
151	no LD0	MCU_SPI0_D0		MCU_GPIO0_3	B11
151	DSI & LD0	OLDI0_A3N	Available in SOM with “DSI” and LD0” configuration;		AD18
152	no LD0	MCU_SPI0_D1		MCU_GPIO0_4	D10
152	DSI & LD0	OLDI0_CLK0P	Available in SOM with “DSI” and LD0” configuration;		AE17
153	no LD0	MCU_SPI0_CS1		MCU_GPIO0_1	E10
153	DSI & LD0	OLDI0_A3P	Available in SOM with “DSI” and LD0” configuration;		AE19
154	no RFCNTL	MCU_MCAN1_RX		MCU_GPIO0_16	E7
154	RFCNTL	RF_CNTL3_1V8	Available in SOM with "RFCNTL” configuration;		LBES5PL2xL.25
155	no RFCNTL	MCU_MCAN0_RX		MCU_GPIO0_14	D6
155	RFCNTL	RF_CNTL0_1V8	Available in SOM with "RFCNTL” configuration;		LBES5PL2xL.27
156	no RFCNTL	MCU_MCAN1_TX		MCU_GPIO0_15	F8
156	RFCNTL	RF_CNTL4_1V8	Available in SOM with "RFCNTL” configuration;		LBES5PL2xL.24
157	no RFCNTL	MCU_MCAN0_TX		MCU_GPIO0_13	E8
157	RFCNTL	RF_CNTL1_1V8	Available in SOM with "RFCNTL” configuration;		LBES5PL2xL.26
158		GND	Digital Ground		GND
159		GND	Digital Ground		GND
160	DSI	DSI0_TXN1	Available in SOM with "DSI" configuration;		AB13
160	no DSI	OLDI0_A1N			AC19
161	DSI	DSI0_TXN0	Available in SOM with "DSI" configuration;		AD11
161	no DSI	OLDI0_A0N			AE20
162	DSI	DSI0_TXP1	Available in SOM with "DSI" configuration;		AB14
162	no DSI	OLDI0_A1P			AD19
163	DSI	DSI0_TXP0	Available in SOM with "DSI" configuration;		AD12
163	no DSI	OLDI0_A0P			AD20

Pin	Assembly	Pin name	Notes	GPIO	Ball
164	DSI	DSI0_TXN2	Available in SOM with "DSI" configuration;		AC12
164	no DSI	OLDI0_A2N			AA19
165	DSI	DSI0_TXN3	Available in SOM with "DSI" configuration;		AE14
165	no DSI	OLDI0_A3N			AD18
166	DSI	DSI0_TXP2	Available in SOM with "DSI" configuration;		AC13
166	no DSI	OLDI0_A2P			AB19
167	DSI	DSI0_TXP3	Available in SOM with "DSI" configuration;		AE15
167	no DSI	OLDI0_A3P			AE19
168	DSI	DSI0_TXCLKN	Available in SOM with "DSI" configuration;		AA12
168	no DSI	OLDI0_CLK0N			AE18
169		GND	Digital Ground		GND
170	DSI	DSI0_TXCLKP	Available in SOM with "DSI" configuration;		AA13
170	no DSI	OLDI0_CLK0P			AE17
171		GPMC0_AD9	BOOTMODE09 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_24	AB25
172		GND	Digital Ground		GND
173		GPMC0_AD3	BOOTMODE03 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	GPIO0_18	V25
174		GPMC0_CSN2	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	GPIO0_43	T22
175		GPMC0_WAIT1		GPIO0_38	AD24
176		GPMC0_CSN3	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	GPIO0_44	U25
177		RGMII2_TD1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	GPIO0_90	A21
178		GND	Digital Ground		GND
179		GND	Digital Ground		GND
180		OLDI0_CLK1N			AD15
181		OLDI0_A7P			AA16
182		OLDI0_CLK1P			AD14
183		OLDI0_A7N			AB16
184		OLDI0_A4N			AD17
185		GND	Digital Ground		GND
186		OLDI0_A4P			AD16
187	no TP	SPI0_D0	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_RXD” signal.	GPIO1_18	B20, LBES5PL2XL.6 (“WBE” or ”WBD”)
187	TP	TS_X-	Signal source is Resistive Touch controller		TSC2046.8
188		OLDI0_A5N			AB17
189	no TP	SPI0_CLK	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_CLK” signal.	GPIO1_17	B21, LBES5PL2XL.8 (“WBE” or ”WBD”)
189	TP	TS_X+	Signal source is Resistive Touch controller		TSC2046.6

Pin	Assembly	Pin name	Notes	GPIO	Ball
190		OLDI0_A5P			AC17
191	no TP	SPI0_CS0	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_FRM” signal and cannot be used externally	GPIO1_15	D20, LBES5PL2XL.4 (“WBE” or ”WBD”)
191	TP	TS_Y+	Signal source is Resistive Touch controller		TSC2046.7
192		OLDI0_A6N			AC16
193	no TP	SPI0_D1	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_TXD” signal.	GPIO1_19	C21, LBES5PL2XL.7 (“WBE” or ”WBD”)
193	TP	TS_Y-	Signal source is Resistive Touch controller		TSC2046.9
194		OLDI0_A6P			AC15
195	AC	AGND	Audio Ground		AGND
195	no AC	NC	Audio Ground		AGND
196	AC	HPOUTFB	Signal source is Audio Codec		WM8904.14
196	no AC & GPMC	GPMC0_WEN	Available in SOM without "AC” and with "GPMC" configuration	GPIO0_34	T25
196	no AC & no GPMC	NC			NC
197	AC	LINEIN1_LP	Signal source is Audio Codec		WM8904.26
197	no AC & GPMC	GPMC0_WPN	Available in SOM without "AC” and with "GPMC" configuration	GPIO0_39	P24
197	no AC & no GPMC	NC			NC
198	no AC	GPMC0_ADVN_ALE	Available in SOM without "AC” configuration	GPIO0_32	R25
198	AC	HPLOUT	Signal source is Audio Codec		R25
199	no AC	GPMC0_WAIT0	Available in SOM without "AC” configuration	GPIO0_37	AA24
199	AC	LINEIN1_RP	Signal source is Audio Codec		AA24
200	no AC	GPMC0_BE0N_CLE	Available in SOM without "AC” configuration	GPIO0_35	U24
200	AC	HPROUT	Signal source is Audio Codec		WM8904.15

7.5 VAR-SOM-AM62P Connector Pin Mux

Table 3: VAR-SOM-AM62P PINMUX

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
1	no EC	B18	RGMII1_TX_CTL	RMII1_TX_EN						GPIO0_73			
3	no EC	C16	RGMII1_TD3	CLKOUT0						GPIO0_78			
4	no EC	B15	RGMII1_RD0	RMII1_RXD0						GPIO0_81			
5	no EC	A17	RGMII1_TD2							GPIO0_77			
6	no EC	B16	RGMII1_RD1	RMII1_RXD1						GPIO0_82			
9	no EC	C17	RGMII1_TD1	RMII1_TXD1						GPIO0_76			
10	no EC	A14	RGMII1_RD2							GPIO0_83			
11	no EC	A18	RGMII1_TD0	RMII1_TXD0						GPIO0_75			
12	no EC	B14	RGMII1_RD3							GPIO0_84			
15	no EC	A15	RGMII1_RX_CTL	RMII1_RX_ER						GPIO0_79			
16	no EC	A16	RGMII1_RXC	RMII1_REF_CLK						GPIO0_80			
17		E24	MCASP0_AXR1	SPI2_CS2	ECAP1_IN_APWM_OUT			MAIN_ERRORn	EHRPWM1_A	GPIO1_9	EQEP0_S		
18	no AC & no GPMC	T25	GPMC0_WEn		MCASP1_AXR0				TRC_DATA9	GPIO0_34			
20	no AC & no GPMC	P24	GPMC0_WPn	AUDIO_EXT_REFCLK1	GPMC0_A22	UART6_TXD			TRC_DATA13	GPIO0_39			
21		AA25	GPMC0_AD10	VOUT0_DATA18	UART3_RXD	MCASP2_AXR2				GPIO0_25	OBSCLK0		BOOTMODE 10
22		AC24	GPMC0_AD15	VOUT0_DATA23	UART5_TXD	MCASP2_ACLKR	MCASP2_AXR5		TRC_DATA19	GPIO0_30	UART2_RTSn		BOOTMODE 15
23		AB24	GPMC0_AD14	VOUT0_DATA22	UART5_RXD	MCASP2_AFSR	MCASP2_AXR4		TRC_DATA20	GPIO0_29	UART2_CTSn		BOOTMODE 14
24		Y24	GPMC0_AD12	VOUT0_DATA20	UART4_RXD	MCASP2_AFSX			TRC_DATA22	GPIO0_27			BOOTMODE 12
25		AD25	GPMC0_AD13	VOUT0_DATA21	UART4_TXD	MCASP2_ACLKX			TRC_DATA21	GPIO0_28			BOOTMODE 13
26		W24	GPMC0_AD11	VOUT0_DATA19	UART3_TXD	MCASP2_AXR3			TRC_DATA23	GPIO0_26			BOOTMODE 11

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
29		C25	EXT_REFCLK1	SYNC1_OUT	SPI2_CS3	SYSCLKOUT0	TIMER_IO4	CLKOUT0	CP_GEMAC_CPTS0_RFT_CLK	GPIO1_30	ECAP0_IN_APWM_OUT		
30		F16	MDIO0_MDIO							GPIO0_85			
31	GPMC & no MMC2 & no OSPI	U22	GPMC0_AD0			MCASP2_AXR4			TRC_CLK	GPIO0_15			BOOTMODE00
31	OSPI & no MMC2 & no GPMC	P23	OSPI0_CLK							GPIO0_0			
31	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	L21	MMC2_DAT3	MCASP1_AXR3		UART5_RXD	EHRPWM0_A			GPIO0_65			
33	GPMC & no MMC2 & no OSPI	U21	GPMC0_AD1			MCASP2_AXR5			TRC_CTL	GPIO0_16			BOOTMODE01
33	OSPI & no MMC2 & no GPMC	N23	OSPI0_LBCLKO					UART5_RTSn		GPIO0_1			
33	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	L20	MMC2_DAT2	MCASP1_AXR2		UART5_TXD	EHRPWM0_B	I2C2_SDA		GPIO0_66			
35	GPMC & no MMC2 & no OSPI	P25	GPMC0_DIR			MCASP2_AXR13		MAIN_ERRORn	TRC_DATA14	GPIO0_40	EQEP2_S		
35	OSPI & no MMC2 & no GPMC	N24	OSPI0_D1							GPIO0_4			
35	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	K22	MMC2_DAT1	MCASP1_AXR1			EHRPWM1_A	I2C2_SDA		GPIO0_67			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
36	GPMC & no MMC2 & no OSPI	R24	GPMC0_OEn_REn		MCASP1_AXR1				TRC_DATA8	GPIO0_33			
36	OSPI & no MMC2 & no GPMC	P22	OSPI0_DQS					UART5_CTSn		GPIO0_2			
39		G23	MCASP0_AFSR	SPI2_CS0	UART1_RXD				EHRPWM0_A	GPIO1_13	EQEP1_S		
40		W25	GPMC0_AD7			MCASP2_AXR11			TRC_DATA5	GPIO0_22			BOOTMODE07
41		E25	MCASP0_AXR2	SPI2_D1	UART1_RTSn	UART6_TXD		ECAP2_IN_APWM_OUT		GPIO1_8	EQEP0_B		
43		G20	MCASP0_ACLKR	SPI2_CLK	UART1_TXD				EHRPWM0_B	GPIO1_14	EQEP1_I		
44		B23	MCAN0_TX	UART5_RXD	TIMER_IO2	SYNC2_OUT	UART1_DTRn	EQEP2_I		GPIO1_24	MCASP2_AXR0	EHRPWM_TZn_IN3	
45		D25	MCASP0_AXR3	SPI2_D0	UART1_CTSn	UART6_RXD		ECAP1_IN_APWM_OUT		GPIO1_7	EQEP0_A		
46		F20	MCAN0_RX	UART5_TXD	TIMER_IO3	SYNC3_OUT	UART1_RIn	EQEP2_S		GPIO1_25	MCASP2_AXR1	EHRPWM_TZn_IN4	
47	GPMC & no MMC2 & no OSPI	T24	GPMC0_BE1n			MCASP2_AXR12			TRC_DATA11	GPIO0_36			
47	OSPI & no MMC2 & no GPMC	L23	OSPI0_CSn3	OSPI0_RESET_OUT0	OSPI0_ECC_FAIL	MCASP1_ACLKR	MCASP1_AXR3	UART5_TXD		GPIO0_14			
47	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	J25	MMC2_SDCD	MCASP1_ACLKX		UART4_RXD	EHRPWM2_A	EHRPWM_TZn_IN1		GPIO0_71			
48		T21	GPMC0_AD5			MCASP2_AXR9			TRC_DATA3	GPIO0_20			BOOTMODE05
50		AD21	VOUT0_DATA12	GPMC0_A12			UART5_RTSn			GPIO0_57			
51		AC21	VOUT0_DATA13	GPMC0_A13			UART5_CTSn			GPIO0_58			
52		AE23	VOUT0_DATA7	GPMC0_A7			UART5_TXD	EQEP2_B		GPIO0_52			
53		AC23	VOUT0_DATA6	GPMC0_A6			UART5_RXD	EQEP2_A		GPIO0_51			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
54		C19	RGMII2_RD3		AUDIO_EXT_REFCLK0					GPIO1_6	EQEP2_B		
55		A19	RGMII2_TD3	CLKOUT0	MCASP2_ACLKX					GPIO1_0	EQEP2_S		
56		D17	RGMII2_TD2		MCASP2_AFSX					GPIO0_91	EQEP2_I		
57		D19	RGMII2_RXC	RMII2_REF_CLK	MCASP2_AXR1					GPIO1_2			
58	no BTPCM	B8	MCU_UART0_CTSn	MCU_TIMER_IO0		MCU_SPI1_D0				MCU_GPIO0_7			
59	GPMC & no MMC2 & no OSPI	Y25	GPMC0_CLK		MCASP1_AXR3	GPMC0_FCLK_MUX			TRC_DATA6	GPIO0_31			
59	OSPI & no MMC2 & no GPMC	M24	OSPI0_D3							GPIO0_6			
59	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	K25	MMC2_SDWP	MCASP1_AFSX		UART4_TXD	EHRPWM2_B	EHRPWM_TZn_IN2		GPIO0_72			
60		J24	MMC1_CLK		TIMER_IO4	UART3_RXD		SPI1_CS0	SPI2_CS2	GPIO1_46			
61		H22	MMC1_DAT2	CP_GEMAC_CPTS0_TS_SYNC	TIMER_IO1	UART2_TXD	MCAN1_RX	SPI1_D1	SPI2_CS3	GPIO1_43			
62		H21	MMC1_DAT0	CP_GEMAC_CPTS0_HW2TSPUSH	TIMER_IO3	UART2_CTSn	ECAP2_IN_APWM_OUT		SPI2_D1	GPIO1_45			
63		H23	MMC1_DAT1	CP_GEMAC_CPTS0_HW1TSPUSH	TIMER_IO2	UART2_RTSn	ECAP1_IN_APWM_OUT	SPI1_CS2	SPI2_D0	GPIO1_44			
64		H20	MMC1_CMD		TIMER_IO5	UART3_TXD		SPI1_CLK	SPI2_CS0	GPIO1_47			
65		H25	MMC1_DAT3	CP_GEMAC_CPTS0_TS_COMP	TIMER_IO0	UART2_RXD	MCAN1_TX	SPI1_D0	SPI2_CS1	GPIO1_42			
68		E20	SPI0_CS1	CP_GEMAC_CPTS0_TS_COMP	EHRPWM0_B	ECAP0_IN_APWM_OUT		MAIN_ERRORn		GPIO1_16		EHRPWM_TZn_IN5	
69		F23	MCASP0_AXR0		AUDIO_EXT_REFCLK0				EHRPWM1_B	GPIO1_10	EQEP0_I		
70		P21	OSPI0_D6	SPI1_D0	MCASP1_ACLKX	UART6_RTSn				GPIO0_9			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
71		E17	RGMII2_RD2		MCASP2_AXR0					GPIO1_5	EQEP2_A		
72		F25	MCASP0_AFSX	SPI2_CS3	AUDIO_EXT_REFCLK1					GPIO1_12	EQEP1_B		
73		B19	RGMII2_TD0	RMII2_TXD0	MCASP2_AXR6					GPIO0_89			
74		F17	MDIO0_MDC							GPIO0_86			
75		N22	OSPI0_D5	SPI1_CLK	MCASP1_AXR0	UART6_TXD				GPIO0_8			
76	GPMC & no MMC2 & no OSPI	U20	GPMC0_AD2			MCASP2_AXR6			TRC_DATA0	GPIO0_17			BOOTMODE02
76	OSPI & no MMC2 & no GPMC	L25	OSPI0_D0							GPIO0_3			
76	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	K21	MMC2_CLK	MCASP1_ACLKR	MCASP1_AXR5	UART6_RXD	EHRPWM0_SYNCI		I2C3_SCL	GPIO0_69			
77		N20	OSPI0_D7	SPI1_D1	MCASP1_AFSX	UART6_CTSn				GPIO0_10			
79		N21	OSPI0_D4	SPI1_CS0	MCASP1_AXR1	UART6_RXD				GPIO0_7			
80		D23	MMC1_SDCD	UART6_RXD	TIMER_IO6	UART3_RTSn	MCAN1_TX	SPI1_CS3	SPI2_CLK	GPIO1_48			
81		E16	RGMII2_RD1	RMII2_RXD1	MCASP2_AFSR			MCASP2_AXR7		GPIO1_4			
82		G21	USB1_DRVVBUS							GPIO1_51			
83		A22	UART0_RXD	ECAP1_IN_APWM_OUT	SPI2_D0	EHRPWM2_A				GPIO1_20			
84		T20	GPMC0_AD4			MCASP2_AXR8			TRC_DATA2	GPIO0_19			BOOTMODE04
85		B22	UART0_TXD	ECAP2_IN_APWM_OUT	SPI2_D1	EHRPWM2_B				GPIO1_21			
86		V24	GPMC0_AD6			MCASP2_AXR10			TRC_DATA4	GPIO0_21			BOOTMODE06
87		A24	I2C0_SDA		SPI2_CS2	TIMER_IO5	UART1_DSRn	EQEP2_B	EHRPWM_SOCB	GPIO1_27	ECAP2_IN_APWM_OUT		
88		B25	I2C0_SCL		SYNC0_OUT	OBSCLK1	UART1_DCDn	EQEP2_A	EHRPWM_SOCA	GPIO1_26	ECAP1_IN_APWM_OUT	SPI2_CS0	

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
90		B24	I2C1_SDA	UART1_TXD	TIMER_IO1	SPI2_CLK	EHRPWM0_SYNCO			GPIO1_29	EHRPWM2_B	MMC2_SDWP	
91	no BTPCM	B6	MCU_UART0_RXD							MCU_GPIO0_5			
92		C24	I2C1_SCL	UART1_RXD	TIMER_IO0	SPI2_CS1	EHRPWM0_SYNCI			GPIO1_28	EHRPWM2_A	MMC2_SDCD	
93	no BTPCM	B7	MCU_UART0_RTSn	MCU_TIMER_IO1		MCU_SPI1_D1				MCU_GPIO0_8			
94		G22	USB0_DRVVBUS							GPIO1_50			
96		D16	RGMII2_TXC	RMII2_CRS_DV	MCASP2_AXR5					GPIO0_88			
97	no EC	B17	RGMII1_TXC	RMII1_CRS_DV						GPIO0_74			
99	no BTPCM	C8	MCU_UART0_TXD							MCU_GPIO0_6			
100	GPMC & no MMC2 & no OSPI	T23	GPMC0_CSn0			MCASP2_AXR14			TRC_DATA15	GPIO0_41			
100	OSPI & no MMC2 & no GPMC	N25	OSPI0_D2							GPIO0_5			
100	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	K24	MMC2_CMD	MCASP1_AFSR	MCASP1_AXR4	UART6_TXD	EHRPWM0_SYNCO	EHRPWM_TZn_IN0	I2C3_SDA	GPIO0_70			
102	GPMC & no MMC2 & no OSPI	U23	GPMC0_CSn1			MCASP2_AXR15			TRC_DATA16	GPIO0_42			
102	OSPI & no MMC2 & no GPMC	M25	OSPI0_CSn0							GPIO0_11			
102	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	K23	MMC2_DAT0	MCASP1_AXR0			EHRPWM1_B	I2C2_SCL		GPIO0_68			
113		A20	RGMII2_TX_CTL	RMII2_TX_EN	MCASP2_AXR4					GPIO0_87			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
115		AC25	GPMC0_AD8	VOUT0_DATA16	UART2_RXD	MCASP2_AXR0				GPIO0_23			BOOTMODE 08
117		F24	MCASP0_ACLKX	SPI2_CS1	ECAP2_IN_APWM_OUT					GPIO1_11	EQEP1_A		
120		F19	RGMII2_RX_CTL	RMII2_RX_ER	MCASP2_AXR3					GPIO1_1			
122		E19	RGMII2_RD0	RMII2_RXD0	MCASP2_AXR2					GPIO1_3			
124		D24	MMC1_SDWP	UART6_TXD	TIMER_IO7	UART3_CTSn	MCAN1_RX	SPI1_CS1		GPIO1_49			
128		F14	MCU_RESETSTATz							MCU_GPIO0_21			
140	no LD0	A13	WKUP_I2C0_SCL							MCU_GPIO0_19			
141	no LD0	C11	WKUP_I2C0_SDA							MCU_GPIO0_20			
142	no LD0	C7	WKUP_UART0_CTSn	WKUP_TIMER_IO0		MCU_SPI1_CS0				MCU_GPIO0_11			
143	no LD0	C6	WKUP_UART0_RTSn	WKUP_TIMER_IO1		MCU_SPI1_CLK				MCU_GPIO0_12			
145	no LD0	D8	WKUP_UART0_RXD		MCU_SPI0_CS2					MCU_GPIO0_9			
146	no COEX	E11	MCU_I2C0_SCL							MCU_GPIO0_17			
147	no LD0	D7	WKUP_UART0_TXD		MCU_SPI1_CS2					MCU_GPIO0_10			
148	no COEX	D11	MCU_I2C0_SDA							MCU_GPIO0_18			
150	no LD0	C10	MCU_SPI0_CLK							MCU_GPIO0_2			
151	no LD0	B11	MCU_SPI0_D0							MCU_GPIO0_3			
152	no LD0	D10	MCU_SPI0_D1							MCU_GPIO0_4			
153	no LD0	E10	MCU_SPI0_CS1	MCU_OBSCLK0	MCU_SYSCLKOUT0	MCU_EXT_REFCLK0	MCU_TIMER_IO1			MCU_GPIO0_1			
154	no RFCNTL	E7	MCU_MCAN1_RX	MCU_TIMER_IO3	MCU_SPI0_CS2	MCU_SPI1_CS2	MCU_SPI1_CLK			MCU_GPIO0_16			
155	no RFCNTL	D6	MCU_MCAN0_RX	MCU_TIMER_IO0	MCU_SPI1_CS3					MCU_GPIO0_14			

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	BOOTSTRAP
156	no RFCNTL	F8	MCU_MCAN1_TX	MCU_TIMER_IO2		MCU_SPI1_CS1	MCU_EXT_REFCLK0			MCU_GPIO0_15			
157	no RFCNTL	E8	MCU_MCAN0_TX	WKUP_TIMER_IO0	MCU_SPI0_CS3					MCU_GPIO0_13			
171		AB25	GPMC0_AD9	VOUT0_DATA17	UART2_TXD	MCASP2_AXR1				GPIO0_24			BOOTMODE09
173		V25	GPMC0_AD3			MCASP2_AXR7			TRC_DATA1	GPIO0_18			BOOTMODE03
174		T22	GPMC0_CSn2	I2C2_SCL	MCASP1_AXR4	UART4_RXD		MCAN1_TX	TRC_DATA17	GPIO0_43	MCASP1_AFSR		
175		AD24	GPMC0_WAIT1	VOUT0_EXTPCLKIN	GPMC0_A21	UART6_RXD				GPIO0_38	EQEP2_I		
176		U25	GPMC0_CSn3	I2C2_SDA	GPMC0_A20	UART4_TXD	MCASP1_AXR5	MCAN1_RX	TRC_DATA18	GPIO0_44	MCASP1_ACLKR		
177		A21	RGMII2_TD1	RMII2_TXD1	MCASP2_ACLKR			MCASP2_AXR8		GPIO0_90			
187	no TP	B20	SPI0_D0	CP_GEMAC_CPTS0_HW1TSPUSH	EHRPWM1_B					GPIO1_18			
189	no TP	B21	SPI0_CLK	CP_GEMAC_CPTS0_TS_SYNC	EHRPWM1_A					GPIO1_17			
191	no TP	D20	SPI0_CS0		EHRPWM0_A					GPIO1_15			
193	no TP	C21	SPI0_D1	CP_GEMAC_CPTS0_HW2TSPUSH	EHRPWM_TZn_IN0					GPIO1_19			
196	no AC & GPMC	T25	GPMC0_WEn		MCASP1_AXR0				TRC_DATA9	GPIO0_34			
197	no AC & GPMC	P24	GPMC0_WPn	AUDIO_EXT_REFCLK1	GPMC0_A22	UART6_TXD			TRC_DATA13	GPIO0_39			
198	no AC	R25	GPMC0_ADVn_ALE		MCASP1_AXR2				TRC_DATA7	GPIO0_32			
199	no AC	AA24	GPMC0_WAIT0		MCASP1_AFSX				TRC_DATA12	GPIO0_37			
200	no AC	U24	GPMC0_BE0n_CLE		MCASP1_ACLKX				TRC_DATA10	GPIO0_35			

8. SOM's Interfaces

8.1 Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 4: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, MIPI CSI, MIPI DSI, LVDS	100 Ω Differential

8.2 Display Interfaces

8.2.1 OLDI/LVDS

The VAR-SOM-AM62P exports the AM62Px Sitara's two single-link Open LVDS Display Interface transmitters (OLDITX) provided by the Display Subsystem (DSS) with the following main features:

- OLDI-SL (Single Link): up to 1920 x 1080 at 60fps (165-MHZ Pixel Clock)
- OLDI-DL (Dual Link): up to 3840 x 1080 at 60 fps (150-MHz Pixel Clock)
- Two single-link (duplicate) OLDI output link mode.
- 18-bit or 24-bit output with OLDI mapping modes (three or four LVDS data channels, one clock channel) per instance.
- LVDS signaling: Compliant with ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits).

8.2.1.1 LVDS0 Signals

Table 5: LVDS0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
161	no DSI	OLDI0_A0N		LVDS0 Data0 Differential Pair Negative side	AE20
163	no DSI	OLDI0_A0P		LVDS0 Data0 Differential Pair Positive side	AD20
160	no DSI	OLDI0_A1N		LVDS0 Data1 Differential Pair Negative side	AC19
162	no DSI	OLDI0_A1P		LVDS0 Data1 Differential Pair Positive side	AD19
164	no DSI	OLDI0_A2N		LVDS0 Data2 Differential Pair Negative side	AA19
166	no DSI	OLDI0_A2P		LVDS0 Data2 Differential Pair Positive side	AB19
165	no DSI	OLDI0_A3N		LVDS0 Data3 Differential Pair Negative side	AD18
167	no DSI	OLDI0_A3P		LVDS0 Data3 Differential Pair Positive side	AE19
168	no DSI	OLDI0_CLK0N		LVDS0 clock Differential Pair Negative side	AE18
170	no DSI	OLDI0_CLK0P		LVDS0 clock Differential Pair Positive side	AE17

Note: In case of “DSI” and “LD0” configuration, LVDS0 signals will be exported via SOM connector pins instead of the default MCU/WKUP signals.

Pin#	Assy	Pin Function	Alt#	Notes	Ball
140	DSI & LD0	OLDI0_A0N		Available in SOM with “DSI” and LD0” configuration; LVDS0 Data0 Differential Pair Negative side	AE20
142	DSI & LD0	OLDI0_A0P		Available in SOM with “DSI” and LD0” configuration; LVDS0 Data0 Differential Pair Positive side	AD20
141	DSI & LD0	OLDI0_A1N		Available in SOM with “DSI” and LD0” configuration; LVDS0 Data1 Differential Pair Negative side	AC19
143	DSI & LD0	OLDI0_A1P		Available in SOM with “DSI” and LD0” configuration; LVDS0 Data1 Differential Pair Positive side	AD19
145	DSI & LD0	OLDI0_A2N		Available in SOM with “DSI” and LD0” configuration; LVDS0 Data2 Differential Pair Negative side	AA19
147	DSI & LD0	OLDI0_A2P		Available in SOM with “DSI” and LD0” configuration; LVDS0 Data2 Differential Pair Positive side	AB19
151	DSI & LD0	OLDI0_A3N		Available in SOM with “DSI” and LD0” configuration; LVDS0 Data3 Differential Pair Negative side	AD18
153	DSI & LD0	OLDI0_A3P		Available in SOM with “DSI” and LD0” configuration; LVDS0 Data3 Differential Pair Positive side	AE19
150	DSI & LD0	OLDI0_CLK0N		Available in SOM with “DSI” and LD0” configuration; LVDS0 clock Differential Pair Negative side	AE18
152	DSI & LD0	OLDI0_CLK0P		Available in SOM with “DSI” and LD0” configuration; LVDS0 clock Differential Pair Positive side	AE17

8.2.1.2 LVDS1 Signals

Table 6: LVDS1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
184		OLDI0_A4N		LVDS1 Data0 Differential Pair Negative side	AD17
186		OLDI0_A4P		LVDS1 Data0 Differential Pair Positive side	AD16
188		OLDI0_A5N		LVDS1 Data1 Differential Pair Negative side	AB17
190		OLDI0_A5P		LVDS1 Data1 Differential Pair Positive side	AC17
192		OLDI0_A6N		LVDS1 Data2 Differential Pair Negative side	AC16
194		OLDI0_A6P		LVDS1 Data2 Differential Pair Positive side	AC15
183		OLDI0_A7N		LVDS1 Data3 Differential Pair Negative side	AB16
181		OLDI0_A7P		LVDS1 Data3 Differential Pair Positive side	AA16
180		OLDI0_CLK1N		LVDS1 clock Differential Pair Negative side	AD15
182		OLDI0_CLK1P		LVDS1 clock Differential Pair Positive side	AD14

8.2.2 DSI

The VAR-SOM-AM62P exports the AM62Px Sitara's MIPI® DSI with 4 Lane MIPI® D-PHY which supports up to 3840 x 1080 at 60 fps (300-MHz Pixel Clock).

Note: In "DSI" configuration, "LD0" configuration can be chosen making it possible to export also LVDS0 signals via SOM connector pins instead of the default MCU/WKUP signals.

Table 7: DSI Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
168	DSI	DSI0_TXCLKN		Available in SOM with "DSI" configuration; DSI0 clock Differential Pair Negative side	AA12
170	DSI	DSI0_TXCLKP		Available in SOM with "DSI" configuration; DSI0 clock Differential Pair Positive side	AA13
161	DSI	DSI0_TXN0		Available in SOM with "DSI" configuration; DSI0 Data0 Differential Pair Negative side	AD11
160	DSI	DSI0_TXN1		Available in SOM with "DSI" configuration; DSI0 Data1 Differential Pair Negative side	AB13
164	DSI	DSI0_TXN2		Available in SOM with "DSI" configuration; DSI0 Data2 Differential Pair Negative side	AC12
165	DSI	DSI0_TXN3		Available in SOM with "DSI" configuration; DSI0 Data3 Differential Pair Negative side	AE14
163	DSI	DSI0_TXP0		Available in SOM with "DSI" configuration; DSI0 Data0 Differential Pair Positive side	AD12
162	DSI	DSI0_TXP1		Available in SOM with "DSI" configuration; DSI0 Data1 Differential Pair Positive side	AB14
166	DSI	DSI0_TXP2		Available in SOM with "DSI" configuration; DSI0 Data2 Differential Pair Positive side	AC13
167	DSI	DSI0_TXP3		Available in SOM with "DSI" configuration; DSI0 Data3 Differential Pair Positive side	AE15

8.3 Camera Interface

8.3.1 MIPI CSI-2

The VAR-SOM-AM62P exports one Camera Serial interface 4 Lane with DPHY provided by the AM62Px CSI_RX_IF module.

The CSI_RX_IF deals with the processing of the pixel data coming from an external image sensor and supports the following features:

- Compliant to MIPI CSI-2 v1.3
- Supports up to 16 virtual channels per input (partial MIPI CSI v2.0 feature)
- Data rate up to 1.5 Gbps per lane
- Supports 1, 2, 3, or 4 Data Lane connection to DPHY_RX
- Programmable formats including YUV420, YUV422, RGB, Raw, and User Defined (over 25 different formats supported)
- One independent (simultaneous) output stream:
    - One (up to 32 Channels) DMA interface through a 128-bit PSI_L connection to DMSS for transfers to memory:
        - Byte packed (32x4) format, elastic buffer mode
        - Max rate 1 data cycle every 4 main clocks
        - ByteValid per byte in Last Data Phase (LDP)
        - 32 thread ID's supported (virtual channel & data type combinations); Flexible number of threads (32 Max)
        - Virtual channels and data types mapped via mmr to PSI_L thread ID's
        - Internal FF based FIFO; RAM based buffer (2kx128)
- Functional and data path error interrupts
- ECC support

8.3.1.1 MIPI-CSI2 Signals

Table 8: MIPI-CSI2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
137		CSI0_RXCLKN		CSI Clock Differential Pair Negative side	AE12
135		CSI0_RXCLKP		CSI Clock Differential Pair Positive side	AE11
121		CSI0_RXN0		CSI Data0 Differential Pair Negative side	AB11
119		CSI0_RXP0		CSI Data0 Differential Pair Positive side	AB10
123		CSI0_RXN1		CSI Data1 Differential Pair Negative side	AC10
125		CSI0_RXP1		CSI Data1 Differential Pair Positive side	AC9
129		CSI0_RXN2		CSI Data2 Differential Pair Negative side	AA10
127		CSI0_RXP2		CSI Data2 Differential Pair Positive side	AA9
131		CSI0_RXN3		CSI Data3 Differential Pair Negative side	AD9
133		CSI0_RXP3		CSI Data3 Differential Pair Positive side	AD8

8.4 Ethernet Interface

The AM62Px device has an integrated one 3-port Gigabit Ethernet Switch subsystem into device MAIN domain named CPSW0. The 3-port Gigabit Ethernet Switch (CPSW0) subsystem provides Ethernet packet communication for the device and can be configured as an Ethernet switch.

The 3-port CPSW0 subsystem provides the following features:

- Two Ethernet ports (port 1 and 2) with selectable RGMII and RMII interfaces and an internal Communications
- Port Programming Interface (CPPI) port (port 0)
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Cut through switch support
- Eight priority level Quality Of Service (QOS) support (802.1p)
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
    - Timestamp module capable of time stamping external timesync events like Pulse-Per-Second and also generating Pulse-Per-Second outputs
    - CPTS module that supports time stamping for IEEE1588 with support for 4 hardware push events and generation of compare output pulses
- DSCP Priority Mapping (IPv4 and IPv6)
- Energy Efficient Ethernet (EEE) support (802.3az)
- Flow Control Support (802.3x)
- Wire rate switching (802.1d)
- Non-Blocking switch fabric
- Time Sensitive Network Support
    - IEEE P802.3br Interspersing Express Traffic
    - IEEE 802.1Qbv Enhancements for Scheduled Traffic
- Address Lookup Engine (ALE)
    - 512 ALE table entries
    - Configurable number of addresses plus VLANs
    - Wire rate lookup
    - Host controlled time-based aging and/or auto-aging
    - Spanning tree support
    - L2 address lock and L2 filtering support
    - MAC authentication (802.1x)
    - Receive-based or destination-based Multicast and Broadcast rate limits
    - MAC address blocking
    - Source port locking
    - OUI (Vendor ID) host accept/deny feature
    - Configurable number of classifier/policers (32)
    - VLAN support
        - 802.1Q compliant:
          Auto add port VLAN for untagged frames on ingress
          Auto VLAN removal on egress and auto pad to minimum frame size
- EtherStats and 802.3Stats Remote Network Monitoring (RMON) statistics gathering (per port statistics)
- Ethernet Mac transmit to Ethernet Mac receive Loopback mode (digital loopback) supported
- CPSGMII Loopback Modes (transmit to receive)

- Maximum frame size of 2024 bytes
- Management Data Input/Output (MDIO) module for PHY Management with Clause 45 support
- Programmable interrupt control with selected interrupt pacing
- Host port CPPI Streaming Packet Interface (CPPI_GCLK)
- Digital loopback and FIFO loopback modes supported
- Emulation support
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps modes only.
- RAM Error Detection and Correction (SECDED)

8.4.1 RGMII1/RMII1

The SOM can be ordered in one of the following configurations:

- **"EC" configuration** – The VAR-SOM-AM62P includes an on SOM a Gigabit PHY Analog Devices ADIN1300 connected to RGMII1 interface signals.
  External connector and magnetics should be implemented on carrier board to complete the interface to the media.
- **"no EC" configuration** - The VAR-SOM-AM62P exposes the RGMII1/RMII1 interface signals to the SO-DIMM connector, pins will be referenced to voltage level depending on "RG2CM" configuration:
  - In **"no RG2CM" configuration** – RGMII1/RMII1 pins will be referenced to 3.3V
  - In **"RG2CM" configuration** – RGMII1/RMII1 pins will be referenced to 1.8V

8.4.1.1 Ethernet PHY

The on-SOM Analog Devices ADIN1300 Gigabit PHY in conjunction with the external magnetics on carrier board complete the interface to the media.
PHY LINK LEDs 10/100 and 1000 combined on SOM to one signal 10/100/1000.

The Following External Gigabit magnetics are required to complete the Ethernet PHY interface to the media.

Table 9: Gigabit Ethernet Magnetics

Vendor	P/N	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

Table 10: Ethernet PHY Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
15	EC	ETH0_LED_ACT		Signal source is Ethernet PHY Ethernet PHY Activity LED, active low	ADIN1300.21
16	EC	ETH0_LED_LINK_10_100_1000		Signal source is Ethernet PHY Ethernet PHY Link LED, active low	ADIN1300.26 via inv. FET
5	EC	ETH0_MDI_A_M		Signal source is Ethernet PHY	ADIN1300.13
3	EC	ETH0_MDI_A_P		Differential Pair Positive side Signal source is Ethernet PHY	ADIN1300.12
11	EC	ETH0_MDI_B_M		Signal source is Ethernet PHY	ADIN1300.15
9		ETH0_MDI_B_P		Differential Pair Positive side	ADIN1300.14
6	EC	ETH0_MDI_C_M		Signal source is Ethernet PHY	ADIN1300.17
4	EC	ETH0_MDI_C_P		Differential Pair Positive side Signal source is Ethernet PHY	ADIN1300.16
12	EC	ETH0_MDI_D_M		Signal source is Ethernet PHY	ADIN1300.19
10	EC	ETH0_MDI_D_P		Differential Pair Positive side Signal source is Ethernet PHY	ADIN1300.18
1	EC	NC		With "EC" configuration this pin is Not Connected	NC
97	EC	NC		With "EC" configuration this pin is Not Connected	NC

Table 11: ADIN1300 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100_1000	ON	ON	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

8.4.1.2 RGMII1/RMII1 Signals

Table 12: RGMII1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
4	no EC	RGMII1_RD0	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	B15
6	no EC	RGMII1_RD1	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	B16
10	no EC	RGMII1_RD2	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	A14
12	no EC	RGMII1_RD3	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	B14
15	no EC	RGMII1_RX_CTL	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Receive Control signal	A15
16	no EC	RGMII1_RXC	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series EMI filter; RGMII - Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL;	A16
11	no EC	RGMII1_TD0	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	A18
9	no EC	RGMII1_TD1	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	C17
5	no EC	RGMII1_TD2	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	A17
3	no EC	RGMII1_TD3	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	C16
1	no EC	RGMII1_TX_CTL	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input! RGMII - Transmit Control signal	B18
97	no EC	RGMII1_TXC	0	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series 33R resistor; RGMII - Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	B17

Table 13: RMII1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
3	no EC	CLKOUT0	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	C16
29		CLKOUT0	5	RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	C25
55		CLKOUT0	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	A19
97	no EC	RMII1_CRS_DV	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series 33R resistor; RGMII - Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	B17
16	no EC	RMII1_REF_CLK	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series EMI filter; RGMII - Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL;	A16
15	no EC	RMII1_RX_ER	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Receive Control signal	A15
4	no EC	RMII1_RXD0	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	B15
6	no EC	RMII1_RXD1	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	B16
1	no EC	RMII1_TX_EN	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input! RGMII - Transmit Control signal	B18
11	no EC	RMII1_TXD0	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V,	A18

Pin#	Assy	Pin Function	Alt#	Notes	Ball
				In "RG2CM" configuration referenced to 1.8V; RGMII Data out	
9	no EC	RMII1_TXD1	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	C17

8.4.2 RGMII2/RMII2

RGMII2/RMII2 interface signals are always exported through SO-DIMM connector.
Signals, in conjunction to MDIO signals exported from SO-DIMM connector, they can be used to interface an external Ethernet PHY.

Voltage level depends on “RG2CM” configuration:

- In **“no RG2CM” configuration** – RGMII2/RMII2 pins will be referenced to 3.3V
- In **“RG2CM” configuration** – RGMII2/RMII2 pins will be referenced to 1.8V

8.4.2.1 RGMIII2/RMII2 Signals

Table 14: RGMII2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
122		RGMII2_RD0	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	E19
81		RGMII2_RD1	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	E16
71		RGMII2_RD2	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	E17
54		RGMII2_RD3	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	C19
120		RGMII2_RX_CTL	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Receive Control signal	F19
57		RGMII2_RXC	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL;	D19
73		RGMII2_TD0	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	B19
177		RGMII2_TD1	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	A21
56		RGMII2_TD2	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	D17
55		RGMII2_TD3	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	A19
113		RGMII2_TX_CTL	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Transmit Control signal	A20

Pin#	Assy	Pin Function	Alt#	Notes	Ball
96		RGMII2_TXC	0	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series 33R resistor; RGMII - Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	D16

Table 15: RMII2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
3	no EC	CLKOUT0	1	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	C16
29		CLKOUT0	5	RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	C25
55		CLKOUT0	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	A19
96		RMII2_CRS_DV	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series 33R resistor; RGMII - Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	D16
57		RMII2_REF_CLK	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL;	D19
120		RMII2_RX_ER	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Receive Control signal	F19
122		RMII2_RXD0	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	E19
81		RMII2_RXD1	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMI Data in	E16
113		RMII2_TX_EN	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII - Transmit Control signal	A20
73		RMII2_TXD0	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	B19
177		RMII2_TXD1	1	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; RGMII Data out	A21

8.4.3 RGMII1/RMII1 & RGMIII2/RMII2 Control Signals

Table 16: RGMII1/RMII1 & RGMIII2/RMII2 control Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
74		MDIO0_MDC	0	Pin is referenced to 3.3V. In "RG2CM" configuration pin is routed via on SOM 1.8<->3.3V voltage translator; Do not alter pinmux with "EC" configuration	F17
30		MDIO0_MDIO	0	Pin is referenced to 3.3V, and has an internal 1.47K Pull Up. In "RG2CM" configuration pin is routed via on SOM 1.8<->3.3V voltage translator. Do not alter pinmux with "EC" configuration	F16

8.4.4 Common Platform Time Sync (CPTS)

The Common Platform Time Sync (CPTS) module is used to facilitate host control of time sync operations. It enables compliance with the IEEE 1588-2008 standard for a precision clock synchronization protocol.

Main features of CPTS module are:

- Supports the selection of multiple external clock sources
- Software control of time sync events via interrupt or polling
- Supports up to 8 hardware timestamp push inputs
- Supports timestamp counter compare output (CPTS_COMP)
- Supports timestamp counter bit output (CPTS_SYNC)
- Supports a configurable number of timestamp Generator bit outputs (CPTS_GENFn).
- Supports Ethernet Enhanced Scheduled Traffic Operations (CPTS_ESTFn).
- 32-bit and 64-bit timestamp modes with PPM and nudge adjustment.

NOTE

CPTS has one or more signals which can be exported from more than one pin.
However, only specific pin combinations known as IOSETs are valid.
These are defined in TI's SysConfig-PinMux Tool.
The below tables present the valid IOSETs

Table 17: CPTS Signal Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		CP_GEMAC_CPTS0_RFT_CLK	6	CPTS Reference Clock Input	C25
88		SYNC0_OUT	2	CPTS Time Stamp Generator Bit 0 Output from Time Sync Router	B25
29		SYNC1_OUT	1	CPTS Time Stamp Generator Bit 1 Output from Time Sync Router	C25
44		SYNC2_OUT	3	CPTS Time Stamp Generator Bit 2 Output from Time Sync Router	B23
46		SYNC3_OUT	3	CPTS Time Stamp Generator Bit 3 Output from Time Sync Router	F20

Table 18: CPTS Signal IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
187	no TP	CP_GEMAC_CPTS0_HW1TSPUSH	1	CPTS Hardware Time Stamp Push Input to Time Sync Router Available in SOM without TP	B20
193	no TP	CP_GEMAC_CPTS0_HW2TSPUSH	1	CPTS Hardware Time Stamp Push Input to Time Sync Router Available in SOM without TP	C21
68		CP_GEMAC_CPTS0_TS_COMP	1	CPTS Time Stamp Counter Compare Output from CPSW3G0 CPTS	E20
189	no TP	CP_GEMAC_CPTS0_TS_SYNC	1	CPTS Time Stamp Counter Bit Output from CPSW3G0 CPTS Available in SOM without TP	B21

Table 19: CPTS Signal IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
63		CP_GEMAC_CPTS0_HW1TSPUSH	1	CPTS Hardware Time Stamp Push Input to Time Sync Router Bank voltage set on SOM 1.8V/3.3V	H23
62		CP_GEMAC_CPTS0_HW2TSPUSH	1	CPTS Hardware Time Stamp Push Input to Time Sync Router Bank voltage set on SOM 1.8V/3.3V	H21
65		CP_GEMAC_CPTS0_TS_COMP	1	CPTS Time Stamp Counter Compare Output from CPSW3G0 CPTS Bank voltage set on SOM 1.8V/3.3V	H25
61		CP_GEMAC_CPTS0_TS_SYNC	1	CPTS Time Stamp Counter Bit Output from CPSW3G0 CPTS Bank voltage set on SOM 1.8V/3.3V	H22

8.5 Wi-Fi & BT

VAR-SOM-AN62P module can be assembled with one of the following Wi-Fi modules:

- Murata Type 2EL - 2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Module based on NXP IW612 chipset
- Murata Type 2DL -2.4GHz & 5GHz Wi-Fi® + Bluetooth® Module based on NXP IW611 chipset

8.5.1 Murata Type 2EL/2DL Module key features:

- Wi-Fi® 802.11a/b/g/n/ac/ax
- Bluetooth® 5.4 BR/EDR/LE
- 802.15.4
- Modules have an antenna connection through a U. FL JACK connector
- Antenna cable connected to module must have 50-Ω impedance

Error! Reference source not found. illustrates the VAR-SOM-MX8M-MINI internal Wi-Fi and BT c onnectivity.

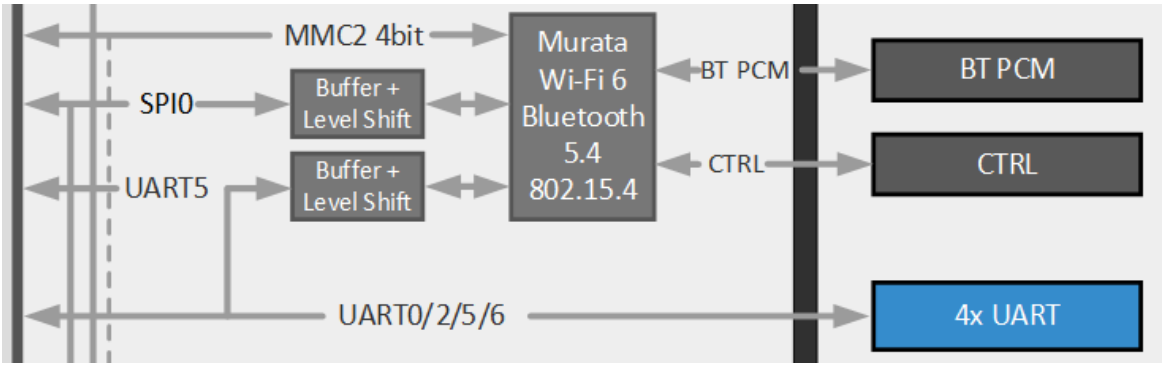


Figure 3: VAR-SOM-AM62P Wi-Fi & BT Internal Connection

NOTE

BT, BT UART buffer are controlled using GPIO0_60.

- Logic “High” enables the BT and buffer.
- Logic “Low” disables them and releases the BT UART signals to be used via SOM connector.

802.15.4 buffer is controlled using SPI0_D0 (GPIO1_18)

- Logic “High” disables the buffer
- Logic “Low” the buffe enables the buffer.

8.5.2 Interface Implementation Options

8.5.2.1 Module Configuration with “WBD” Option (Murata Type 2DL)

- System use**: Wi-Fi and Bluetooth**.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT buffer (using GPIO0_60) and BT function.

    - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi.**
    - Disable Wi-Fi function.
    - Enable the BT buffer (using GPIO0_60) and BT function.

8.5.2.2 Module Configuration with "WBE" Option (Murata Type 2EL)

- System use: **Wi-Fi and Bluetooth and 802.15.4**.
    - BT UART external interface pins should be left floating.
    - TP SPI pins can be used in SPI mode only
- System use: **Wi-Fi and no BT no 802.15.4**.
    - In this case, disable the BT and 802.15.4 module (using GPIO0_60 and GPIO1_18)
    - BT UART and TP SPI interface pins can be used externally with any of the alternate functions.
- System use: **BT and 802.15.4 and no Wi-Fi.**
    - Disable Wi-Fi function.
    - Enable the BT and 802.15.4 module (using GPIO0_60 and GPIO1_18).

8.5.2.3 Module Configuration without "WBD" or "WBE" Option

- System use: **no Wi-Fi and no BT**.
    - BT UART and TP SPI interface pins accessible externally with any of its alternative functions.

8.5.3 Bluetooth UART Interface Signals

Table 20: BT UART Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
50		UART5_RTSn	4	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled Always exposed;	AD21
51		UART5_CTSn	4	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled Always exposed;	AC21
52		UART5_TXD	4	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled Always exposed;	AE23
53		UART5_RXD	4	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled Always exposed;	AC23

8.5.4 Bluetooth PCM Interface signals

Table 21: BT PCM interface signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
91	BTPCM	BT_PCM_CLK_1V8		Available in SOM with "BTPCM" configuration; Signal source is WIFI module. Available in "BTPCM" configuration; Pin referenced to 1.8V	LBES5PL2xL.57
58	BTPCM	BT_PCM_IN_1V8		Available in SOM with "BTPCM" configuration; Signal source is WIFI module. Available in "BTPCM" configuration; Pin referenced to 1.8V	LBES5PL2xL.93
93	BTPCM	BT_PCM_OUT_1V8		Available in SOM with "BTPCM" configuration; Signal source is WIFI module. Available in "BTPCM" configuration; Pin referenced to 1.8V	LBES5PL2xL.59
99	BTPCM	BT_PCM_SYNC_1V8		Available in SOM with "BTPCM" configuration; Signal source is WIFI module. Available in "BTPCM" configuration; Pin referenced to 1.8V	LBES5PL2xL.61

NOTE

This assembly option was not tested yet; for further support, please contact sales@variscite.com

8.5.5 802.15.4. SPI Interface signals

Table 22: 802.15.4 SPI interface signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
193	no TP	SPI0_D1	0	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_TXD” signal.	C21, LBES5PL2XL.7 (“WBE” or ”WBD”)
189	no TP	SPI0_CLK	0	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_CLK” signal.	B21, LBES5PL2XL.8 (“WBE” or ”WBD”)
187	no TP	SPI0_D0	0	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_RXD” signal.	B20, LBES5PL2XL.6 (“WBE” or ”WBD”)
191	no TP	SPI0_CS0	0	"Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_FRM” signal and cannot be used externally"	D20, LBES5PL2XL.4 (“WBE” or ”WBD”)

8.5.6 WLAN/BT Wake Interface signals

The SOM has internal GPIOs connected to the WIFI/BT module host/device wake signals

Table 23: WLAN/BT Host/Device Wake signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
Int.	WBE or WBD	GPIO0_71	7	WIFI_HOST_WAKE	J25, LBES5PL2XL.73 (“WBE” or ”WBD”)
Int.	WBE or WBD	GPIO0_72	7	BT_HOST_WAKE	K25, LBES5PL2XL.76 (“WBE” or ”WBD”)
Int.	WBE or WBD	GPIO0_55	7	BT_DEV_WAKE	W22, LBES5PL2XL.75 (“WBE” or ”WBD”)

8.5.7 WIFI control signals

Table 24: WIFI control Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
146	COEX	COEX_SIN_1V8		Available in “COEX” and “WBE” or ”WBD” configuration. Signal source is WIFI module, connected to “WCI-2_SIN” signal. Pin referenced to 1.8V.	LBES5PL2xL.69
148	COEX	COEX_SOUT_1V8		Available in “COEX” and “WBE” or ”WBD” configuration. Signal source is WIFI module, connected to “WCI-2_OUT” signal, Pin referenced to 1.8V	LBES5PL2xL.70

Pin#	Assy	Pin Function	Alt#	Notes	Ball
155	RFCNTL	RF_CNTL0_1V8		Available in SOM with "RFCNTL" configuration; Signal source is WIFI module. Available in "BTPCM" configuration; Pin referenced to 1.8V	LBES5PL2xL.27
157	RFCNTL	RF_CNTL1_1V8		Available in SOM with "RFCNTL" configuration; Signal source is WIFI module. Available in "BTPCM" configuration; Pin referenced to 1.8V	LBES5PL2xL.26
154	RFCNTL	RF_CNTL3_1V8		Available in SOM with "RFCNTL" configuration; Signal source is WIFI module. Available in "BTPCM" configuration; Pin referenced to 1.8V	LBES5PL2xL.25
156	RFCNTL	RF_CNTL4_1V8		Available in SOM with "RFCNTL" configuration; Signal source is WIFI module. Available in "BTPCM" configuration; Pin referenced to 1.8V	LBES5PL2xL.24

NOTE

This assembly option was not tested yet; for further support, please contact sales@variscite.com

8.6 Multi-Media Card Secure Digital (MMCSD)

The VAR-SOM-AM62P exposes the MMCSD1/MMCSD2 controller 4-bit interface.

Key features of MMCSD:

- SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01
- SDIO Specification v3.00
- 1.8 V and 3.3 V operation
- 1-bit/4-bit SD and SDIO modes
- Up to SDR104 rate

MMCSD1 interface is used for supporting interface between the host system and the SD/SDIO/MMC cards.

MMCSD2 is used internally for the Wi-Fi SDIO interface on the SOM.
In case of SOM Module Configuration without “WBD” or “WBE” and with “MMC2” interface MMCSD2 interface is accessible externally via SOM pins

8.6.1 MMCSD1 Signals

For ***Card Detect function*** any GPIO can be used; For pinout compatibility with other SOMs of VAR-SOM pin2pin family, pin 80 GPIO1_48 is used.

Table 25: MMCSD1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
60		MMC1_CLK	0	Bank voltage set on SOM 1.8V/3.3V	J24
64		MMC1_CMD	0	Bank voltage set on SOM 1.8V/3.3V	H20
62		MMC1_DAT0	0	Bank voltage set on SOM 1.8V/3.3V	H21
63		MMC1_DAT1	0	Bank voltage set on SOM 1.8V/3.3V	H23
61		MMC1_DAT2	0	Bank voltage set on SOM 1.8V/3.3V	H22
65		MMC1_DAT3	0	Bank voltage set on SOM 1.8V/3.3V	H25
80		MMC1_SDCD	0	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D23
124		MMC1_SDWP	0		D24

8.6.2 MMCSD2 Interface Signals

Table 26: MMC2 Supply voltage input Signal

Pin#	Assy	Pin Function	Alt#	Notes	Ball
36	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	VDDSHV6		MMC2 pins group power IN “no MMC2" configuration: * Not Connected "MMC2" configuration: VDDSHV6 1.8V/3.3V voltage input. Must supply one option: 1.8 or 3.3V, Use SOM pin 49 to sequence 1.8 or 3.3V supply. The following SOM pins are referenced to this voltage: 31,33,35,47,59,76,100,102	1B10

Table 27: MMC2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
76	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_CLK	0	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K21
100	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_CMD	0	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K24
102	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_DAT0	0	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K23
35	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_DAT1	0	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K22
33	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_DAT2	0	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L20
31	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_DAT3	0	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L21
47	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_SDCD	0	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	J25
92		MMC2_SDCD	9		C24
59	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MMC2_SDWP	0	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K25
90		MMC2_SDWP	9		B24

8.6.3 MMCSD0 Signals

MMCSD controller, MMCSD0, is used internally for the eMMC interface on the SOM.

8.7 USB 2.0

The VAR-SOM-AM62P consists Two USB controllers and PHYs that support USB 2.0

The USB 2.0 subsystem supports the following USB Features:

- Operational modes:
  - Supports USB 2.0 Host mode at High-Speed (HS, 480 Mbps), Full-Speed (FS, 12 Mbps), and Low-Speed (LS, 1.5 Mbps)
  - Supports USB 2.0 Device mode at High-Speed (HS, 480 Mbps), and Full-Speed (FS, 12 Mbps). LowSpeed is not supported in Device mode.
  - Supports all modes of transfers - Control, Bulk, Interrupt, and Isochronous.
- A DRD (Dual-Role-Device - Host or Device) USB controller with the following features:
  - Compatible to the xHCI 1.0 specification in Host mode
  - Compatible with the USB 2.0 specification in Device mode
  - Supports 15 IN (Receive), 15 OUT (Transmit) endpoints (EPs), and one EP0 endpoint which is bidirectional
  - Internal DMA controller
  - Descriptor caching and data pre-fetching ensures high performance
  - Dynamic FIFO memory allocation for all endpoints
- Operation flexibility
  - Same programming model for HS, FS, and LS operation
  - Each controller instance can provide either USB Host or USB Device functionality

8.7.1 USB Port0/Port1 Interface Signals

Table 28: USB 2.0 Port0/Port1 Interface signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
114		USB0_DM		Differential Pair Negative side, USB DRD capable	AE8
116		USB0_DP		Differential Pair Positive side, USB DRD capable	AE7
94		USB0_DRVVBUS		USB PWR signal, active high control signal used to enable power to the downstream port switch.	G22
106		USB0_VBUS		USB PHY power pin; 5V tolerant	Y7
108		USB1_DM		Differential Pair Negative side, USB DRD capable	AE10
110		USB1_DP		Differential Pair Positive side, USB DRD capable	AE9
82		USB1_DRVVBUS		USB PWR signal, active high control signal used to enable power to the downstream port switch.	G21
104		USB1_VBUS		USB PHY power pin; 5V tolerant	Y10

USBx_ID

The USB PHY ID pin functionality can be implemented via any GPIO:

- "Low" means the SoC is Host role
- "High" or “Float” means the SoC is Device role.

8.8 Audio

The VAR-SOM-AM62P features the following audio interfaces:

- WM8904CGEFL Audio codec interfaces:
  - Analog outputs & inputs: stereo line-in & Stereo HP out.
  - Digital microphone input
- 3x Multichannel Audio Serial Ports (McASP)
  - Transmit and Receive Clocks up to 50 MHz
  - Up to 16/10/6 Serial Data Pins across 3 McASP with Independent TX and RX Clocks
  - Supports Time Division Multiplexing (TDM) Inter-IC Sound (I2S), and Similar Formats
  - Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 Formats)
  - FIFO Buffers for Transmit and Receive (256 Bytes)
  - Support for audio reference output clock

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only. The codec interfaces the SoC via McASP1 lines, when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

The following figure illustrates the connectivity for no large AC coupling capacitors implemented on SOM.

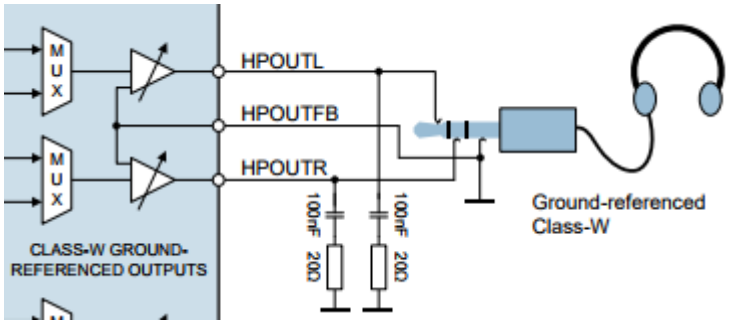


Figure 4: WM8904 Headphone connectivity

8.8.1 WM8904CGEFL Audio Codec

8.8.1.1 Audio Codec Signals

Table 29: Analog audio Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
195		AGND		Audio Ground	AGND
18	AC	DMIC_CLK		Signal source is Audio Codec Digital microphone clock output	WM8904.1
20	AC	DMIC_DATA		Signal source is Audio Codec Digital microphone data input; Divided internally by 475 Ohm resistors to match Codec input levels	WM8904.27
198	AC	HPLOUT		Signal source is Audio Codec Left headphone output (line or headphone output)	WM8904.13
196	AC	HPOUTFB		Signal source is Audio Codec Headphone output ground loop noise rejection feedback	WM8904.14
200	AC	HPROUT		Signal source is Audio Codec Right headphone output (line or headphone output)	WM8904.15
197	AC	LINEIN1_LP		Signal source is Audio Codec Left channel input	WM8904.26
199	AC	LINEIN1_RP		Signal source is Audio Codec Right channel input	WM8904.24

8.8.2 Multichannel Audio Serial Ports (McASP)

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although inter-component digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

NOTE

McASP has one or more signals which can be exported from more than one pin.
However, only specific pin combinations known as IOSETs are valid.
These are defined in TI's SysConfig-PinMux Tool.
The below tables present the valid IOSETs

The following table details the MCASP and AUDIO_EXT_REFCLK interface signals definition.

Table 30: SAI interface signals definition

Name	Function	DIR
MCASPx_AXRxx	Audio transmit/receive data – channel xx	I/O
MCASPx_ACLKX	Transmit bit clock	I/O
MCASPx_AFSX	Transmit frame synchronization	I/O
MCASPx_ACLKR	Receive bit clock	I/O
MCASPx_AFSR	Receive frame synchronization	I/O
AUDIO_EXT_REFCLKx	Transmit/ Receive high-frequency controller clock	I/O

8.8.2.1 McASP0 Signals

Table 31: McASP0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
43		MCASP0_ACLKR	0		G20
117		MCASP0_ACLKX	0		F24
39		MCASP0_AFSR	0		G23
72		MCASP0_AFSX	0		F25
69		MCASP0_AXR0	0		F23
17		MCASP0_AXR1	0		E24
41		MCASP0_AXR2	0		E25
45		MCASP0_AXR3	0		D25

8.8.2.2 McASP1 Signals

Note: McASP1 interface is used by internal Audio Codec.
McASP1interface can be used externally only in SOMs without "AC" assembly option.

Table 32: McASP1 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
47	OSPI & no MMC2 & no GPMC	MCASP1_AXR3	4	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	L23
79		MCASP1_AXR1	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N21
75		MCASP1_AXR0	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N22
70		MCASP1_ACLKX	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	P21
77		MCASP1_AFSX	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N20

Table 33: McASP1 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
79		MCASP1_AXR1	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N21
75		MCASP1_AXR0	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N22
70		MCASP1_ACLKX	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	P21
77		MCASP1_AFSX	2	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N20
47	OSPI & no MMC2 & no GPMC	MCASP1_ACLKR	3	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	L23

Table 34: McASP1 IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
59	GPMC & no MMC2 & no OSPI	MCASP1_AXR3	2	Available in SOM with "GPMC" configuration; Pin referenced to 1.8V	Y25
198	no AC	MCASP1_AXR2	2	Available in SOM without "AC" configuration	R25
36	GPMC & no MMC2 & no OSPI	MCASP1_AXR1	2	Available in SOM with "GPMC" configuration;	R24
18	no AC & no GPMC	MCASP1_AXR0	2	Available in SOM without "AC" and without "GPMC" configuration	T25
200	no AC	MCASP1_ACLKX	2	Available in SOM without "AC" configuration	U24
199	no AC	MCASP1_AFSX	2	Available in SOM without "AC" configuration	AA24
174		MCASP1_AFSR	8	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	T22
176		MCASP1_ACLKR	8	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	U25

Table 35: McASP1 IOSet_4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
176		MCASP1_AXR5	4	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	U25
174		MCASP1_AXR4	2	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	T22
59	GPMC & no MMC2 & no OSPI	MCASP1_AXR3	2	Available in SOM with "GPMC" configuration; Pin referenced to 1.8V	Y25
198	no AC	MCASP1_AXR2	2	Available in SOM without "AC" configuration	R25
36	GPMC & no MMC2 & no OSPI	MCASP1_AXR1	2	Available in SOM with "GPMC" configuration;	R24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
18	no AC & no GPMC	MCASP1_AXR0	2	Available in SOM without "AC" and without "GPMC" configuration	T25
200	no AC	MCASP1_ACLKX	2	Available in SOM without "AC" configuration	U24
199	no AC	MCASP1_AFSX	2	Available in SOM without "AC" configuration	AA24

Table 36: McASP1 IOSet_5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AXR3	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L21
33	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AXR2	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L20
35	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AXR1	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K22
102	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AXR0	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K23
47	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_ACLKX	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	J25
59	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AFSX	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K25
100	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AFSR	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K24
76	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_ACLKR	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K21

Table 37: McASP1 IOSet_6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
76	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AXR5	2	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K21
100	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AXR4	2	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K24
31	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AXR3	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L21
33	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AXR2	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L20
35	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AXR1	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K22
102	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AXR0	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K23
47	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_ACLKX	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	J25
59	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	MCASP1_AFSX	1	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K25

8.8.2.3 McASP2 Signals

Table 38: McASP2 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
102	GPMC & no MMC2 & no OSPI	MCASP2_AXR15	3	Available in SOM with "GPMC" configuration;	U23
100	GPMC & no MMC2 & no OSPI	MCASP2_AXR14	3	Available in SOM with "GPMC" configuration;	T23
35	GPMC & no MMC2 & no OSPI	MCASP2_AXR13	3	Available in SOM with "GPMC" configuration;	P25
47	GPMC & no MMC2 & no OSPI	MCASP2_AXR12	3	Available in SOM with "GPMC" configuration;	T24
40		MCASP2_AXR11	3	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W25
86		MCASP2_AXR10	3	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V24
48		MCASP2_AXR9	3	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T21
84		MCASP2_AXR8	3	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T20
173		MCASP2_AXR7	3	BOOTMODE03 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V25
76	GPMC & no MMC2 & no OSPI	MCASP2_AXR6	3	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U20
33	GPMC & no MMC2 & no OSPI	MCASP2_AXR5	3	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U21
31	GPMC & no MMC2 & no OSPI	MCASP2_AXR4	3	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U22
26		MCASP2_AXR3	3	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W24
21		MCASP2_AXR2	3	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AA25
171		MCASP2_AXR1	3	BOOTMODE09 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB25
115		MCASP2_AXR0	3	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC25
25		MCASP2_ACLKX	3	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AD25
24		MCASP2_AFSX	3	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	Y24
23		MCASP2_AFSR	3	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB24
22		MCASP2_ACLKR	3	BOOTMODE15 pin, has 100K PU on SOM for compatibly with VAR-SOM-AM62; For boot enablement, Pin is Pulled low internally on SOM during boot. Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC24

Table 39: McASP2 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
73		MCASP2_AXR6	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	B19
96		MCASP2_AXR5	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series 33R resistor;	D16
113		MCASP2_AXR4	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A20
120		MCASP2_AXR3	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	F19
122		MCASP2_AXR2	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	E19
57		MCASP2_AXR1	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	D19
71		MCASP2_AXR0	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	E17
55		MCASP2_ACLKX	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A19
56		MCASP2_AFSX	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	D17
81		MCASP2_AFSR	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	E16
177		MCASP2_ACLKR	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A21

Table 40: McASP2 IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
177		MCASP2_AXR8	5	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A21
81		MCASP2_AXR7	5	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	E16
73		MCASP2_AXR6	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	B19
96		MCASP2_AXR5	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series 33R resistor;	D16
113		MCASP2_AXR4	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A20
120		MCASP2_AXR3	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	F19
122		MCASP2_AXR2	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	E19
57		MCASP2_AXR1	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	D19
71		MCASP2_AXR0	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	E17
55		MCASP2_ACLKX	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A19
56		MCASP2_AFSX	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	D17

Table 41: McASP2 IOSet_5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
102	GPMC & no MMC2 & no OSPI	MCASP2_AXR15	3	Available in SOM with "GPMC" configuration;	U23
100	GPMC & no MMC2 & no OSPI	MCASP2_AXR14	3	Available in SOM with "GPMC" configuration;	T23
35	GPMC & no MMC2 & no OSPI	MCASP2_AXR13	3	Available in SOM with "GPMC" configuration;	P25
47	GPMC & no MMC2 & no OSPI	MCASP2_AXR12	3	Available in SOM with "GPMC" configuration;	T24
40		MCASP2_AXR11	3	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W25
86		MCASP2_AXR10	3	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V24
48		MCASP2_AXR9	3	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T21
84		MCASP2_AXR8	3	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T20
173		MCASP2_AXR7	3	BOOTMODE03 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V25
76	GPMC & no MMC2 & no OSPI	MCASP2_AXR6	3	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U20
22		MCASP2_AXR5	4	BOOTMODE15 pin, has 100K PU on SOM for compatibly with VAR-SOM-AM62; For boot enablement, Pin is Pulled low internally on SOM during boot. Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC24
23		MCASP2_AXR4	4	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB24
26		MCASP2_AXR3	3	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W24
21		MCASP2_AXR2	3	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AA25
171		MCASP2_AXR1	3	BOOTMODE09 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB25
115		MCASP2_AXR0	3	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC25
25		MCASP2_ACLKX	3	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AD25
24		MCASP2_AFSX	3	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	Y24
23		MCASP2_AFSR	3	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB24
22		MCASP2_ACLKR	3	BOOTMODE15 pin, has 100K PU on SOM for compatibly with VAR-SOM-AM62; For boot enablement, Pin is Pulled low internally on SOM during boot. Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC24
86		MCASP2_AXR10	3	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V24
48		MCASP2_AXR9	3	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T21

8.8.2.4 Audio External reference clock Signals

The VAR-SOM-AM62P exports also the AUDIO_EXT_REFCLK[0-1] signals which can be used as External clock input to McASP or output from McASP

Table 42: AUDIO_EXT_REFCLK Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
54		AUDIO_EXT_REFCLK0	2	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	C19
69		AUDIO_EXT_REFCLK0	2		F23
20	no AC & no GPMC	AUDIO_EXT_REFCLK1	1	Available in SOM without "AC" and without "GPMC" configuration	P24
72		AUDIO_EXT_REFCLK1	2		F25
197	no AC & GPMC	AUDIO_EXT_REFCLK1	1	Available in SOM without "AC" and with "GPMC" configuration	P24

8.9 Resistive Touch

The VAR-SOM-AM62P features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

The Resistive Touch is available only in SOMs with the “TP” assembly option
when not assembled, SPI0 SoC balls are exported to SOM connector instead of Resistive Touch interface pins.

8.9.1.1 Resistive Touch Signals

Table 43: Serial Resistive Touch Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
187	TP	TS_X-		Signal source is Resistive Touch controller	TSC2046.8
189	TP	TS_X+		Signal source is Resistive Touch controller	TSC2046.6
191	TP	TS_Y+		Signal source is Resistive Touch controller	TSC2046.7
193	TP	TS_Y-		Signal source is Resistive Touch controller	TSC2046.9

NOTE

Resistive touch Controller "TP” cannot be assembled if “WBE” option is selected

8.10 UART

The VAR-SOM-AM62P exposes up to nine UART interfaces. UART5 is used on SOM for Bluetooth interface and can be accessible only if the on SOM buffer is disabled or on SOM without ***"WBD" and "WBE" Configuration***.

The UART includes the following features:

- Edge-selectable RTS_B and edge-detect interrupts
- 16C750-compatible
- RS-485 external transceiver auto flow control support
- 64-byte FIFO buffer for receiver and 64-byte FIFO buffer for transmitter
- Programmable interrupt trigger levels for FIFOs
- Programmable sleep mode
- The 48 MHz functional clock is default option and allows baud rates up to 3.6 Mbps
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Optional multi-drop transmission
- Configurable time-guard feature
- Configurable data format:
    - Parity bit: Even, odd, none
    - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- False start bit detection
- Line break generation and detection
- Fully prioritized interrupt system controls
- Internal test and loopback capabilities

Table 44: UART I/O Configuration vs. mode

Module Pin Name	Device Level Signal Name	I/O	Description	Module Pin Reset Value
WKUP_UARTi				
RX	WKUP_UARTi_RXD	I	Serial data input	HiZ
TX	WKUP_UARTi_TXD	O	Serial data output	1
CTS	WKUP_UARTi_CTS	I	Clear to send	HiZ
RTS	WKUP_UARTi_RTS	O	Request to send	1
MCU_UARTi				
RX	MCU_UARTi_RXD	I	Serial data input	HiZ
TX	MCU_UARTi_TXD	O	Serial data output	1
CTS	MCU_UARTi_CTS	I	Clear to send	HiZ
RTS	MCU_UARTi_RTS	O	Request to send	1
UARTi Modem Signals				
DCD	UARTi_DCDn	I		HiZ
DSR	UARTi_DSRn	I		HiZ
DTR	UARTi_DTRn	O		1
RIN	UARTi_RIN	I		HiZ

Note: i represents a UART instance.

8.10.1 UART0 Signals

Table 45: UART0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
83		UART0_RXD	0	Used as debug UART on Variscite base board	A22
85		UART0_TXD	0	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	B22

8.10.2 UART1 Signals

Table 46: UART1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
45		UART1_CTSn	2		D25
88		UART1_DCDn	4		B25
87		UART1_DSRn	4		A24
44		UART1_DTRn	4		B23
46		UART1_RIn	4		F20
41		UART1_RTSn	2		E25
39		UART1_RXD	2		G23
92		UART1_RXD	1		C24
43		UART1_TXD	2		G20
90		UART1_TXD	1		B24

8.10.3 UART2 Signals

Table 47: UART2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
23		UART2_CTSn	8	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB24
62		UART2_CTSn	3	Bank voltage set on SOM 1.8V/3.3V	H21
22		UART2_RTSn	8	BOOTMODE15 pin, has 100K PU on SOM for compatibly with VAR-SOM-AM62; For boot enablement, Pin is Pulled low internally on SOM during boot. Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC24
63		UART2_RTSn	3	Bank voltage set on SOM 1.8V/3.3V	H23
65		UART2_RXD	3	Bank voltage set on SOM 1.8V/3.3V	H25
115		UART2_RXD	2	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC25
61		UART2_TXD	3	Bank voltage set on SOM 1.8V/3.3V	H22
171		UART2_TXD	2	BOOTMODE09 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB25

8.10.4 UART3 Signals

Table 48: UART3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
124		UART3_CTSn	3		D24
80		UART3_RTSn	3	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D23
21		UART3_RXD	2	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AA25
60		UART3_RXD	3	Bank voltage set on SOM 1.8V/3.3V	J24
26		UART3_TXD	2	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W24
64		UART3_TXD	3	Bank voltage set on SOM 1.8V/3.3V	H20

8.10.5 UART4 Signals

Table 49: UART4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
24		UART4_RXD	2	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	Y24
47	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	UART4_RXD	3	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	J25
174		UART4_RXD	3	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	T22
25		UART4_TXD	2	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AD25
59	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	UART4_TXD	3	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K25
176		UART4_TXD	3	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	U25

8.10.6 UART5 Signals

Table 50: UART5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
36	OSPI & no MMC2 & no GPMC	UART5_CTSn	5	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	P22
51		UART5_CTSn	4	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	AC21
33	OSPI & no MMC2 & no GPMC	UART5_RTSn	5	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	N23
50		UART5_RTSn	4	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	AD21
23		UART5_RXD	2	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB24
31	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	UART5_RXD	3	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L21
44		UART5_RXD	1		B23
53		UART5_RXD	4	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	AC23
22		UART5_TXD	2	BOOTMODE15 pin, has 100K PU on SOM for compatibly with VAR-SOM-AM62; For boot enablement, Pin is Pulled low internally on SOM during boot. Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC24
33	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	UART5_TXD	3	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L20
46		UART5_TXD	1		F20
47	OSPI & no MMC2 & no GPMC	UART5_TXD	5	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	L23
52		UART5_TXD	4	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	AE23

8.10.7 UART6 Signals

Table 51: UART6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
77		UART6_CTSn	3	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N20
70		UART6_RTSn	3	Pin referenced to 1.8V in SOM with "OSPI" configuration;	P21
45		UART6_RXD	3		D25
76	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	UART6_RXD	3	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K21

Pin#	Assy	Pin Function	Alt#	Notes	Ball
79		UART6_RXD	3	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N21
80		UART6_RXD	1	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D23
175		UART6_RXD	3		AD24
20	no AC & no GPMC	UART6_TXD	3	Available in SOM without "AC" and without "GPMC" configuration	P24
41		UART6_TXD	3		E25
75		UART6_TXD	3	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N22
100	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	UART6_TXD	3	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K24
124		UART6_TXD	1		D24
197	no AC & GPMC	UART6_TXD	3	Available in SOM without "AC" and with "GPMC" configuration	P24

8.10.8 MCU UART0 Signals

Table 52: MCU_UART Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
58	no BTPCM	MCU_UART0_CTSn	0		B8
93	no BTPCM	MCU_UART0_RTSn	0		B7
91	no BTPCM	MCU_UART0_RXD	0		B6
99	no BTPCM	MCU_UART0_TXD	0		C8

8.10.9 WKUP UART0 Signals

Table 53: WKUP UART Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
142	no LD0	WKUP_UART0_CTSn	0		C7
143	no LD0	WKUP_UART0_RTSn	0		C6
145	no LD0	WKUP_UART0_RXD	0		D8
147	no LD0	WKUP_UART0_TXD	0		D7

8.11 I2C

The VAR-SOM-AM62P exposes up to 5x I2C Interface connectivity peripherals which provides serial interface for external devices. Data rates of up to 400 kbps are supported.

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave.
I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices.
This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The I2C has the following key features:

- Compliant with Philips I2C-bus specification version 2.1
- Supports a standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- Supports HS mode (up to 3.4 Mbps) only for instances with true open drain buffer and in 1.8 V mode
- 7-bit and 10-bit device addressing modes
- General call
- Start/Restart/Stop
- Multicontroller transmitter/target receiver mode
- Multicontroller receiver/target transmitter mode
- Combined controller transmit/receive and receive/transmit mode
- Built-in FIFO for buffered read
- Module enable/disable capability
- Programmable multitarget channel (responds to four separate addresses)
- Programmable clock generation
- 8-bit-wide data access
- Low power consumption
- Support Auto Idle mechanism
- Support Idle Request/Idle Acknowledge handshake mechanism
- Support for asynchronous wakeup mechanism
- Wide interrupt capability

NOTE

I2C has one or more signals which can be exported from more than one pin.
However, only specific pin combinations known as IOSETs are valid.
These are defined in TI's SysConfig-PinMux Tool.
The below tables present the valid IOSETs

8.11.1 I2C0 Signals

Table 54: I2C0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
88		I2C0_SCL	0		B25
87		I2C0_SDA	0		A24

8.11.2 I2C1 Signals

Table 55: I2C1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
92		I2C1_SCL	0		C24
90		I2C1_SDA	0		B24

8.11.3 I2C2 Signals

Table 56: I2C2 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
174		I2C2_SCL	1	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	T22
176		I2C2_SDA	1	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	U25

Table 57: I2C2 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
102	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	I2C2_SCL	5	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K23
35	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	I2C2_SDA	5	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K22

Table 58: I2C2 IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
102	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	I2C2_SCL	5	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K23
33	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	I2C2_SDA	5	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L20

8.11.4 I2C3 Signals

I2C3 is used internally by on-SOM EEPROM.

8.11.5 MCU I2C0 Signals

Table 59: MCU I2C0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
146	no COEX	MCU_I2C0_SCL	0	Used for MCU_I2C function, connected also to PMIC Internal signal pulled up to SOM_PGOOD using 4.7K resistor	E11
148	no COEX	MCU_I2C0_SDA	0	Used for MCU_I2C function, connected also to PMIC Internal signal pulled up to SOM_PGOOD using 4.7K resistor	D11

8.11.6 WKUP I2C0 Signals

Table 60: WKUP I2C0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
140	no LD0	WKUP_I2C0_SCL	0	Used for WKUP_I2C function, connected also to PMIC Internal signal pulled up to SOM_PGOOD using 4.7K resistor	A13
141	no LD0	WKUP_I2C0_SDA	0	Used for WKUP_I2C function, connected also to PMIC Internal signal pulled up to SOM_PGOOD using 4.7K resistor	C11

8.12 Modular Controller Area Network (MCAN)

The Modular Controller Area Network (MCAN) module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The MCAN has the following key features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- SAE J1939 support
- AUTOSAR support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 filter elements
- Internal Loopback mode for self-test
- Maskable interrupts, two interrupt lines
- Two clock domains (CAN clock/Host clock)
- Parity/ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Local power-down and wakeup support
- Timestamp Counter

Signal Description:

- CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
- CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

NOTE

MCAN has one or more signals which can be exported from more than one pin.
However, only specific pin combinations known as IOSETs are valid.
These are defined in TI's SysConfig-PinMux Tool.
The below tables present the valid IOSETs

8.12.1 MCAN0 Signals

Table 61: MCAN0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
46		MCAN0_RX	0		F20
44		MCAN0_TX	0		B23

8.12.2 MCAN1 Signals

Table 62: MCAN1 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
61		MCAN1_RX	4	Bank voltage set on SOM 1.8V/3.3V	H22
65		MCAN1_TX	4	Bank voltage set on SOM 1.8V/3.3V	H25

Table 63: MCAN1 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
124		MCAN1_RX	4		D24
80		MCAN1_TX	4	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D23

Table 64: MCAN1 IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
176		MCAN1_RX	5	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	U25
174		MCAN1_TX	5	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with “AC” configuration pins are used for Codec I2C- Do not alter pinmux!	T22

8.12.3 MCU_MCAN0 Signals

Table 65: MCU_MCAN0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
155	no RFCNTL	MCU_MCAN0_RX	0		D6
157	no RFCNTL	MCU_MCAN0_TX	0		E8

8.12.4 MCU_MCAN1 Signals

Table 66: MCU_MCAN1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
154	no RFCNTL	MCU_MCAN1_RX	0		E7
156	no RFCNTL	MCU_MCAN1_TX	0		F8

8.13 Multichannel Serial Peripheral Interface (MCSPI)

The VAR-SOM-AM62P exposes up 5 MCSPI interfaces.

The Multichannel Serial Peripheral Interface (MCSPI) is a multichannel transmit/receive, controller/peripheral synchronous serial bus.

Key features of the MCSPI include:

- Full-duplex synchronous serial interface
- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of MCSPI word lengths, ranging from 4 to 32 bits
- Up to four controller channels, or single channel in peripheral mode
- Controller multichannel mode:
    - Full duplex/half duplex
    - Transmit-only/receive-only/transmit-and-receive modes
    - Flexible input/output (I/O) port controls per channel
    - Programmable clock granularity
    - MCSPI configuration per channel. This means, clock definition, polarity enabling and word width
- Single interrupt line for multiple interrupt source events
- Enable the addition of a programmable start-bit for MCSPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable shift operations (1-32 bits)
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel.

NOTE

MCSPI has one or more signals which can be exported from more than one pin.
However, only specific pin combinations known as IOSETs are valid.
These are defined in TI's SysConfig-PinMux Tool.
The below tables present the valid IOSETs

Note: For interfacing multiple peripherals on same SPI bus, one can define any GPIO to be used as chip select.

8.13.1 MCSPI0 Signals

Note: MCSPI0 interface is used by internal Resistive Touch Controller.
MCSPI0 interface can be used externally only in SOMs without "TP" assembly option.

Table 67: MCSPI0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
189	no TP	SPI0_CLK	0	Available in SOM without TP In "WBD" or "WBE" configuration connected also via buffer to Murata 2EL/2DL "SPI_CLK" signal.	B21, LBES5PL2XL.8 ("WBE" or "WBD")
191	no TP	SPI0_CS0	0	Available in SOM without TP In "WBD" or "WBE" configuration connected also via buffer to Murata 2EL/2DL "SPI_FRM" signal and cannot be used externally	D20, LBES5PL2XL.4 ("WBE" or "WBD")
68		SPI0_CS1	0		E20
187	no TP	SPI0_D0	0	Available in SOM without TP In "WBD" or "WBE" configuration connected also via buffer to Murata 2EL/2DL "SPI_RXD" signal.	B20, LBES5PL2XL.6 ("WBE" or "WBD")
193	no TP	SPI0_D1	0	Available in SOM without TP In "WBD" or "WBE" configuration connected also via buffer to Murata 2EL/2DL "SPI_TXD" signal.	C21, LBES5PL2XL.7 ("WBE" or "WBD")

8.13.2 MCSPI1 Signals

Table 68: MCSPI1 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
75		SPI1_CLK	1	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N22
79		SPI1_CS0	1	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N21
70		SPI1_D0	1	Pin referenced to 1.8V in SOM with "OSPI" configuration;	P21
77		SPI1_D1	1	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N20

Table 69: MCSPI1 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
80		SPI1_CS3	5	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D23
63		SPI1_CS2	5	Bank voltage set on SOM 1.8V/3.3V	H23
124		SPI1_CS1	5		D24
60		SPI1_CS0	5	Bank voltage set on SOM 1.8V/3.3V	J24
64		SPI1_CLK	5	Bank voltage set on SOM 1.8V/3.3V	H20
65		SPI1_D0	5	Bank voltage set on SOM 1.8V/3.3V	H25
61		SPI1_D1	5	Bank voltage set on SOM 1.8V/3.3V	H22

8.13.3 MCSPI2 Signals

Table 70: MCSPI2 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
61		SPI2_CS3	6	Bank voltage set on SOM 1.8V/3.3V	H22
60		SPI2_CS2	6	Bank voltage set on SOM 1.8V/3.3V	J24
65		SPI2_CS1	6	Bank voltage set on SOM 1.8V/3.3V	H25
64		SPI2_CS0	6	Bank voltage set on SOM 1.8V/3.3V	H20
80		SPI2_CLK	6	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D23
63		SPI2_D0	6	Bank voltage set on SOM 1.8V/3.3V	H23
62		SPI2_D1	6	Bank voltage set on SOM 1.8V/3.3V	H21

Table 71: MCSPI2 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
72		SPI2_CS3	1		F25
17		SPI2_CS2	1		E24
117		SPI2_CS1	1		F24
39		SPI2_CS0	1		G23
43		SPI2_CLK	1		G20
45		SPI2_D0	1		D25
41		SPI2_D1	1		E25

Table 72: MCSPI2 IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		SPI2_CS3	2		C25
87		SPI2_CS2	2		A24
92		SPI2_CS1	3		C24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
88		SPI2_CS0	9		B25
90		SPI2_CLK	3		B24
83		SPI2_D0	2	Used as debug UART on Variscite base board	A22
85		SPI2_D1	2	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	B22

8.13.4 MCU SPI0 Signals

Table 73: MCU SPI0 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
157	no RFCNTL	MCU_SPI0_CS3	2		E8
145	no LD0	MCU_SPI0_CS2	2		D8
153	no LD0	MCU_SPI0_CS1	0		E10
150	no LD0	MCU_SPI0_CLK	0		C10
151	no LD0	MCU_SPI0_D0	0		B11
152	no LD0	MCU_SPI0_D1	0		D10

Table 74: MCU SPI0 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
157	no RFCNTL	MCU_SPI0_CS3	2		E8
154	no RFCNTL	MCU_SPI0_CS2	2		E7
153	no LD0	MCU_SPI0_CS1	0		E10
150	no LD0	MCU_SPI0_CLK	0		C10
151	no LD0	MCU_SPI0_D0	0		B11
152	no LD0	MCU_SPI0_D1	0		D10

8.13.5 MCU SPI1 Signals

Table 75: MCU SPI1 IOSet_1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
155	no RFCNTL	MCU_SPI1_CS3	2		D6
154	no RFCNTL	MCU_SPI1_CS2	3		E7
156	no RFCNTL	MCU_SPI1_CS1	3		F8
142	no LD0	MCU_SPI1_CS0	3		C7
143	no LD0	MCU_SPI1_CLK	3		C6
58	no BTPCM	MCU_SPI1_D0	3		B8
93	no BTPCM	MCU_SPI1_D1	3		B7

Table 76: MCU SPI1 IOSet_2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
155	no RFCNTL	MCU_SPI1_CS3	2		D6
147	no LD0	MCU_SPI1_CS2	2		D7
156	no RFCNTL	MCU_SPI1_CS1	3		F8
142	no LD0	MCU_SPI1_CS0	3		C7
143	no LD0	MCU_SPI1_CLK	3		C6
58	no BTPCM	MCU_SPI1_D0	3		B8
93	no BTPCM	MCU_SPI1_D1	3		B7

Table 77: MCU SPI1 IOSet_3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
155	no RFCNTL	MCU_SPI1_CS3	2		D6
147	no LD0	MCU_SPI1_CS2	2		D7
156	no RFCNTL	MCU_SPI1_CS1	3		F8
142	no LD0	MCU_SPI1_CS0	3		C7
154	no RFCNTL	MCU_SPI1_CLK	4		E7
58	no BTPCM	MCU_SPI1_D0	3		B8

8.14 OSPI - Octal Serial Peripheral Interface

The VAR-SOM-AM62P exposes the OSPI module which allows single, dual, quad or octal read and write access to external flash devices.

The module contains the following features:

- Support for single, dual, quad (QSPI mode) or octal I/O bus widths.
- Memory mapped ‘direct’ mode of operation for performing flash data transfers and executing code from flash memory.
- Software triggered 'indirect' mode of operation for performing low latency and non-processor intensive flash data transfers.
- Local SRAM of configurable size to reduce advanced high-performance bus overhead and buffer flash data during indirect transfers.
- Set of software advanced peripheral bus accessible flash control registers to perform any flash command, including data transfers up to 8-bytes at a time.
- Additional addressable memory bank to accommodate more than 8-bytes at a time.
- Support for XIP, sometimes referred to as continuous mode.
- Support for DDR Mode and DTR protocol (including Octal DDR protocol with DQS for Octal-SPI devices)
- Programmable device sizes.
- Programmable write protected regions to block system writes from taking effect.
- Programmable delays between transactions.
- Legacy mode allowing software direct access to low level transmit and receive FIFOs, bypassing the higher layer processes.
- An independent reference clock to decouple bus clock from SPI clock – allows slow system clocks.
- Programmable baud rate generator to generate OSPI clocks.
- Features included to improve high speed read data capture mechanism.
- Option to use adapted clocks or DQS to further improve read data capturing.
- Programmable interrupt generation.
- Up to four external device selects - OSPI and QSPI devices can be mixed
- Programmable data decoder, enables continuous addressing mode for each of the connected devices and auto-detection of boundaries between devices.
- Supports BOOT mode.
- Bidirectional CRC on Multiple-SPI interface.
- Handling ECC errors for flash devices with embedded correction engine.
- Full integration with PHY module dedicated to more flexible and power efficient transfers.
- Supports RESET_OUT[1-0] and ECC_FAIL pins for external flash devices where ECC is checked on the flash.

Note: OSPI signals are available on SOM with “OSPI” assembly option.
OSPI signals are referenced to 1.8v.

8.14.1 OSPI Signals

Table 78: OSPI Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	OSPI & no MMC2 & no GPMC	OSPI0_CLK	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	P23
102	OSPI & no MMC2 & no GPMC	OSPI0_CSn0	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	M25
47	OSPI & no MMC2 & no GPMC	OSPI0_CSn3	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	L23
76	OSPI & no MMC2 & no GPMC	OSPI0_D0	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	L25
35	OSPI & no MMC2 & no GPMC	OSPI0_D1	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	N24
100	OSPI & no MMC2 & no GPMC	OSPI0_D2	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	N25
59	OSPI & no MMC2 & no GPMC	OSPI0_D3	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	M24
79		OSPI0_D4	0	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N21
75		OSPI0_D5	0	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N22
70		OSPI0_D6	0	Pin referenced to 1.8V in SOM with "OSPI" configuration;	P21
77		OSPI0_D7	0	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N20
36	OSPI & no MMC2 & no GPMC	OSPI0_DQS	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	P22
47	OSPI & no MMC2 & no GPMC	OSPI0_ECC_FAIL	2	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	L23
33	OSPI & no MMC2 & no GPMC	OSPI0_LBCLKO	0	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	N23
47	OSPI & no MMC2 & no GPMC	OSPI0_RESET_OUT0	1	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	L23

8.15 General-Purpose Memory Controller (GPMC)

The VAR-SOM-AM62P exposes the General-Purpose Memory Controller (GPMC) interface which can be used for interfacing with 8-bit/16-bit NAND flash devices.

Note: GPMC signals are available on SOM with “GPMC” assembly option.

8.15.1 GPMC Signals

Table 79: GPMC Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	GPMC & no MMC2 & no OSPI	GPMC0_AD0	0	Available in SOM with "GPMC” configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U22
33	GPMC & no MMC2 & no OSPI	GPMC0_AD1	0	Available in SOM with "GPMC” configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U21
21		GPMC0_AD10	0	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AA25
26		GPMC0_AD11	0	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W24
24		GPMC0_AD12	0	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	Y24
25		GPMC0_AD13	0	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AD25
23		GPMC0_AD14	0	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB24
22		GPMC0_AD15	0	BOOTMODE15 pin, has 100K PU on SOM for compatibly with VAR-SOM-AM62; For boot enablement, Pin is Pulled low internally on SOM during boot. Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC24
76	GPMC & no MMC2 & no OSPI	GPMC0_AD2	0	Available in SOM with "GPMC” configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U20
173		GPMC0_AD3	0	BOOTMODE03 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V25
84		GPMC0_AD4	0	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T20
48		GPMC0_AD5	0	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T21
86		GPMC0_AD6	0	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V24
40		GPMC0_AD7	0	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W25
115		GPMC0_AD8	0	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC25
171		GPMC0_AD9	0	BOOTMODE09 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB25
198	no AC	GPMC0_ADVn_ALE	0	Available in SOM without "AC” configuration	R25
200	no AC	GPMC0_BE0n_CLE	0	Available in SOM without "AC” configuration	U24
47	GPMC & no MMC2 & no OSPI	GPMC0_BE1n	0	Available in SOM with "GPMC” configuration;	T24
59	GPMC & no MMC2 & no OSPI	GPMC0_CLK	0	Available in SOM with "GPMC” configuration;	Y25

Pin#	Assy	Pin Function	Alt#	Notes	Ball
100	GPMC & no MMC2 & no OSPI	GPMC0_CSn0	0	Available in SOM with "GPMC" configuration;	T23
102	GPMC & no MMC2 & no OSPI	GPMC0_CSn1	0	Available in SOM with "GPMC" configuration;	U23
174		GPMC0_CSn2	0	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	T22
176		GPMC0_CSn3	0	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	U25
35	GPMC & no MMC2 & no OSPI	GPMC0_DIR	0	Available in SOM with "GPMC" configuration;	P25
59	GPMC & no MMC2 & no OSPI	GPMC0_FCLK_MUX	3	Available in SOM with "GPMC" configuration;	Y25
36	GPMC & no MMC2 & no OSPI	GPMC0_OEn_REn	0	Available in SOM with "GPMC" configuration;	R24
199	no AC	GPMC0_WAIT0	0	Available in SOM without "AC" configuration	AA24
175		GPMC0_WAIT1	0		AD24
196	no AC & GPMC	GPMC0_WEn	0	Available in SOM without "AC" and with "GPMC" configuration	T25
197	no AC & GPMC	GPMC0_WPn	0	Available in SOM without "AC" and with "GPMC" configuration	P24

8.16 eCAP

The AM62Px provides up to 3 Enhanced Pulse Width Modulation (EPWM) Modules.

The Enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The ECAP module includes the following features:

- 32-bit time base counter
- 4 × 32 bits event time-stamp capture registers (ECAP0_CAP1 through ECAP0_CAP4)
- 4-stage sequencer (Mod4 counter), synchronized to external events (ECAPx pin edges)
- Independent edge polarity (rising / falling edge) selection for all 4 sequenced time-stamp capture events
- Input capture signal pre-scaling (from 1 to 16)
- One-shot compare register (2 bits) to freeze captures after 1 to 4 time-stamp events
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Interrupt capabilities on any of the 4 capture events
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output

8.16.1 eCAP0 Signals

Table 80: eCAP0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		ECAP0_IN_APWM_OUT	8		C25
68		ECAP0_IN_APWM_OUT	3		E20

8.16.2 eCAP1 Signals

Table 81: eCAP1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
17		ECAP1_IN_APWM_OUT	2		E24
45		ECAP1_IN_APWM_OUT	5		D25
63		ECAP1_IN_APWM_OUT	4	Bank voltage set on SOM 1.8V/3.3V	H23
83		ECAP1_IN_APWM_OUT	1	Used as debug UART on Variscite base board	A22
88		ECAP1_IN_APWM_OUT	8		B25

8.16.3 eCAP2 Signals

Table 82: eCAP2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
41		ECAP2_IN_APWM_OUT	5		E25
62		ECAP2_IN_APWM_OUT	4	Bank voltage set on SOM 1.8V/3.3V	H21
85		ECAP2_IN_APWM_OUT	1	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	B22
87		ECAP2_IN_APWM_OUT	8		A24
117		ECAP2_IN_APWM_OUT	2		F24

8.17 ePWM

The AM62Px provides up to 3 Enhanced Pulse Width Modulation (EPWM) Modules.

Each EPWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Allows events to trigger both CPU interrupts and ADC start of conversions
- Programmable event prescaling minimizes CPU overhead on interrupts
- PWM chopping by a high-frequency carrier signal, useful for pulse transformer gate drives

The main signals used by the EPWM module are:

- **PWM output signals (EPWMxA and EPWMxB)**
  The PWM output signals are available external to the device through the GPIO peripheral.
- **Trip-zone signals (TZ0 to TZ5)**
  These input signals alert the EPWM module of an external fault condition. Each module on a device can be configured to either use or ignore any of the trip-zone signals. The trip-zone signal can be configured as an asynchronous input through the GPIO peripheral.
- **Time-base synchronization input (EPWMxSYNCI) and output (EPWMxSYNCO) signals**
  The synchronization signals daisy chain the EPWM modules together. Each module can be configured to either use or ignore its synchronization input. *For more information see, Daisy-Chain Connectivity between EPWM Modules (*TRM*).*
- **ADC start-of-conversion signals (EPWMxSOCA and EPWMxSOCB)**
  Each EPWM module has two ADC start of conversion signals (one for each sequencer). Any EPWM module can trigger a start of conversion for either sequencer. Which event triggers the start of conversion configured in the Event-Trigger submodule of the EPWM module.
- **Peripheral Bus**
  The peripheral bus is 32-bits wide and allows both 16-bit and 32-bit writes to the EPWM registers.

8.17.1 ePWM Signals

Table 83: ePWM Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
88		EHRPWM_SOCA	6		B25
87		EHRPWM_SOCB	6		A24
100	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM_TZn_IN0	5	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K24
193	no TP	EHRPWM_TZn_IN0	2	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_TXD” signal.	C21, LBES5PL2XL.7 (“WBE” or ”WBD”)
47	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM_TZn_IN1	5	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	J25
59	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM_TZn_IN2	5	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K25
44		EHRPWM_TZn_IN3	9		B23
46		EHRPWM_TZn_IN4	9		F20
68		EHRPWM_TZn_IN5	9		E20

8.17.2 ePWM0 Signals

Table 84: ePWM0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM0_A	4	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L21
39		EHRPWM0_A	6		G23
33	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM0_B	4	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L20
43		EHRPWM0_B	6		G20
68		EHRPWM0_B	2		E20
76	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM0_SYNCI	4	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K21
92		EHRPWM0_SYNCI	4		C24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
90		EHRPWM0_SYNCO	4		B24
100	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM0_SYNCO	4	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K24

8.17.3 ePWM1 Signals

Table 85: ePWM1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
17		EHRPWM1_A	6		E24
35	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM1_A	4	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K22
189	no TP	EHRPWM1_A	2	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_CLK” signal.	B21, LBES5PL2XL.8 (“WBE” or ”WBD”)
69		EHRPWM1_B	6		F23
102	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM1_B	4	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K23
187	no TP	EHRPWM1_B	2	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_RXD” signal.	B20, LBES5PL2XL.6 (“WBE” or ”WBD”)

8.17.4 ePWM2 Signals

Table 86: ePWM2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
47	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM2_A	4	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	J25
83		EHRPWM2_A	3	Used as debug UART on Variscite base board	A22
92		EHRPWM2_A	8		C24
59	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	EHRPWM2_B	4	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K25
85		EHRPWM2_B	3	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	B22
90		EHRPWM2_B	8		B24

8.18 eQEP

The VAR-SOM-AM62P exposes the Enhanced Quadrature Encoder Pulse (EQEP) module.
The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns, as shown in Figure 12-1800. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution).
As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

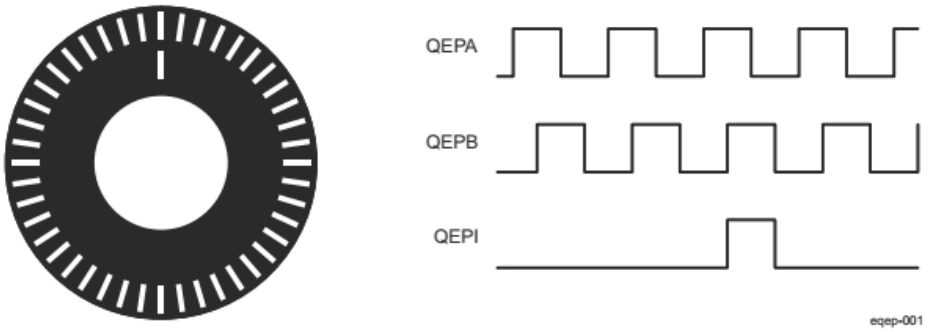


Figure 12-1800. Optical Encoder Disk

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other.
These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vise versa.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 kHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

The EQEP module includes the following features:

- Input synchronization
- Three stage/six stage digital noise filter
- Quadrature decoder unit
- Position counter and control unit for position measurement
- Quadrature edge capture unit for low-speed measurement
- Unit time base for speed and frequency measurement
- Watchdog timer for detecting stalls

- EQEP inputs (A/B/INDEX and STROBE) are available at chip level
- EQEP phase error output is also available. The status of the phase error can be observed by software through the register in the CTRL_MMR0 module.
- Counting modes:
  - Quadrature
  - Clockwise / Counter Clockwise
  - Count / Direction
- Start of Convert input for on-chip Strobe
- EQEP internal strobe (EQEP Strobe input is logically ORed with EQEP A and B inputs) may be used to:
  - Initialize the Position Counter with a non-zero value (for example, due to a limit switch input becoming active)
  - Snapshot the Position Counter into the EQEP_QPOSSLAT register
  - Gate the EQEP Index input preventing it from resetting the Position Counter

8.18.1 eQEP0 Signals

Table 87: eQEP0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
45		EQEP0_A	8		D25
41		EQEP0_B	8		E25
69		EQEP0_I	8		F23
17		EQEP0_S	8		E24

8.18.2 eQEP1 Signals

Table 88: eQEP1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
117		EQEP1_A	8		F24
72		EQEP1_B	8		F25
43		EQEP1_I	8		G20
39		EQEP1_S	8		G23

8.18.3 eQEP2 Signals

Table 89: eQEP2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
53		EQEP2_A	5	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	AC23
71		EQEP2_A	8	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	E17
88		EQEP2_A	5		B25
52		EQEP2_B	5	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	AE23
54		EQEP2_B	8	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	C19
87		EQEP2_B	5		A24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
44		EQEP2_I	5		B23
56		EQEP2_I	8	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	D17
175		EQEP2_I	8		AD24
35	GPMC & no MMC2 & no OSPI	EQEP2_S	8	Available in SOM with "GPMC" configuration;	P25

8.19 Timer

The VAR-SOM-AM62P exposes the Timer interface to its connector.

All timers include specific functions to generate accurate tick interrupts to the operating system. Each timer can be clocked from several different independent clocks. The selection of clock source is made from registers in the MCU_CTRL_MMR0/CTRL_MMR0.

Key features of the Timer controllers:

- Target interface supports:
  - 32-bit data bus width
  - 32-bit access supported
  - 10-bit address bus width
  - Write nonposted transaction mode supported
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Compare and capture modes
- Autoreload mode
- Start/stop mode
- Programmable divider clock source (2n, where n = [0-8])
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal
- On-the-fly read/write register (while counting)
- Generates a 1-ms tick clock with a 32.768 kHz functional clock sourced from the LFOSC

8.19.1.1 MAIN Timer Signals

Table 90: MAIN Timer Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
65		TIMER_IO0	2	Bank voltage set on SOM 1.8V/3.3V	H25
92		TIMER_IO0	2		C24
61		TIMER_IO1	2	Bank voltage set on SOM 1.8V/3.3V	H22
90		TIMER_IO1	2		B24
44		TIMER_IO2	2		B23
63		TIMER_IO2	2	Bank voltage set on SOM 1.8V/3.3V	H23
46		TIMER_IO3	2		F20
62		TIMER_IO3	2	Bank voltage set on SOM 1.8V/3.3V	H21
29		TIMER_IO4	4		C25
60		TIMER_IO4	2	Bank voltage set on SOM 1.8V/3.3V	J24
64		TIMER_IO5	2	Bank voltage set on SOM 1.8V/3.3V	H20
87		TIMER_IO5	3		A24
80		TIMER_IO6	2	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D23
124		TIMER_IO7	2		D24

8.19.1.2 MCU Timer Signals

Table 91: MCU Timer Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
58	no BTPCM	MCU_TIMER_IO0	1		B8
155	no RFCNTL	MCU_TIMER_IO0	1		D6
93	no BTPCM	MCU_TIMER_IO1	1		B7
153	no LD0	MCU_TIMER_IO1	4		E10
156	no RFCNTL	MCU_TIMER_IO2	1		F8
154	no RFCNTL	MCU_TIMER_IO3	1		E7

8.19.1.3 WKUP Timer Signals

Table 92: WKUP Timer Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
142	no LD0	WKUP_TIMER_IO0	1		C7
157	no RFCNTL	WKUP_TIMER_IO0	1		E8
143	no LD0	WKUP_TIMER_IO1	1		C6

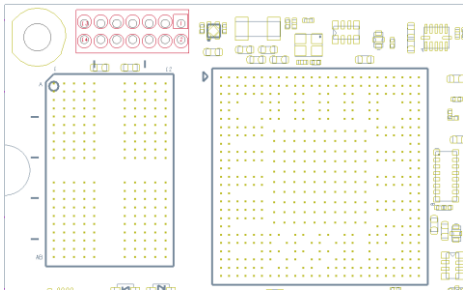
8.20 On chip Debug JTAG

AM62Px On-Chip Debug features are supported through three device interfaces:

- JTAG: IEEE 1149.1 compliant interface that provides access to Boundary Scan and acts as the primary interface for off-chip access to On-Chip debug resources.
- Trigger and Debug Boot Mode: Multi-functional interface that supports product level cross-triggering and debug-related boot modes
- Trace Port: Arm TPIU compliant Trace Port interface is used to facilitate export of trace

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support.
The following document is a good reference for guidelines: Emulation and Trace Headers.
More information can also be found here: XDS Target Connection Guide.

VAR-SOM-AM62P exposes JTAG signals on a 14-pin header (not assembled by default) on the SOM top left side.



8.20.1 JTAG Signals

Table 93: JTAG signals on 14-pin Header Connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
1		VDD_3V3		JTAG reference voltage (3.3v)	
2		TMS		Test Mode Select. Controls the transitions of the test interface state machine. Internal signal pulled up to SOM_PGOOD using 10K resistor.	E14
3		GND		Digital Ground	
4		TCK		Test Clock. Controls the timing of the test interface independently from any system clocks. TCK is pulsed by the equipment controlling the test and not by the tested device. Internal signal pulled up to SOM_PGOOD using 10K resistor.	C13
5		GND		Digital Ground	
6		TDO		Test Data Output. Used to serially output the data from the JTAG registers to the equipment controlling the test.	C14
7					
8		TDI		Test Data Input. Supplies the data to the JTAG registers. Internal signal pulled up to SOM_PGOOD using 10K resistor.	E13
9		GND		Digital Ground	
10		JTAG_EMU_RSTn		JTAG System reset	
11		TRST#		Test Reset. Initializes and disables the test interface. Internal signal pulled down to GND using 4.7K resistor.	B13
12		EMU0		Channel 0 trigger or boot mode select. Internal signal pulled up to SOM_PGOOD using 10K resistor.	B12
13					
14		EMU1		Channel 1 trigger or boot mode select. Internal signal pulled up to SOM_PGOOD using 10K resistor.	D13

8.20.2 TRACE Signals

Table 94: TRACE signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	GPMC & no MMC2 & no OSPI	TRC_CLK	6	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U22
33	GPMC & no MMC2 & no OSPI	TRC_CTL	6	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U21
76	GPMC & no MMC2 & no OSPI	TRC_DATA0	6	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U20
173		TRC_DATA1	6	BOOTMODE03 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V25
200	no AC	TRC_DATA10	6	Available in SOM without "AC" configuration	U24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
47	GPMC & no MMC2 & no OSPI	TRC_DATA11	6	Available in SOM with "GPMC" configuration;	T24
199	no AC	TRC_DATA12	6	Available in SOM without "AC" configuration	AA24
20	no AC & no GPMC	TRC_DATA13	6	Available in SOM without "AC" and without "GPMC" configuration	P24
197	no AC & GPMC	TRC_DATA13	6	Available in SOM without "AC" and with "GPMC" configuration	P24
35	GPMC & no MMC2 & no OSPI	TRC_DATA14	6	Available in SOM with "GPMC" configuration;	P25
100	GPMC & no MMC2 & no OSPI	TRC_DATA15	6	Available in SOM with "GPMC" configuration;	T23
102	GPMC & no MMC2 & no OSPI	TRC_DATA16	6	Available in SOM with "GPMC" configuration;	U23
174		TRC_DATA17	6	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	T22
176		TRC_DATA18	6	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	U25
22		TRC_DATA19	6	BOOTMODE15 pin, has 100K PU on SOM for compatibly with VAR-SOM-AM62; For boot enablement, Pin is Pulled low internally on SOM during boot. Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC24
84		TRC_DATA2	6	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T20
23		TRC_DATA20	6	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB24
25		TRC_DATA21	6	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AD25
24		TRC_DATA22	6	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	Y24
26		TRC_DATA23	6	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W24
48		TRC_DATA3	6	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T21
86		TRC_DATA4	6	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V24
40		TRC_DATA5	6	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W25
59	GPMC & no MMC2 & no OSPI	TRC_DATA6	6	Available in SOM with "GPMC" configuration;	Y25
198	no AC	TRC_DATA7	6	Available in SOM without "AC" configuration	R25
36	GPMC & no MMC2 & no OSPI	TRC_DATA8	6	Available in SOM with "GPMC" configuration;	R24
18	no AC & no GPMC	TRC_DATA9	6	Available in SOM without "AC" and without "GPMC" configuration	T25
196	no AC & GPMC	TRC_DATA9	6	Available in SOM without "AC" and with "GPMC" configuration	T25

8.21 General Purpose IO

The VAR-SOM-AM62P provides IO pins which can be used as GPIOs.

8.21.1 GPIO Signals

Table 95: GPIO Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	OSPI & no MMC2 & no GPMC	GPIO0_0	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	P23
33	OSPI & no MMC2 & no GPMC	GPIO0_1	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	N23
77		GPIO0_10	7	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N20
102	OSPI & no MMC2 & no GPMC	GPIO0_11	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	M25
47	OSPI & no MMC2 & no GPMC	GPIO0_14	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	L23
31	GPMC & no MMC2 & no OSPI	GPIO0_15	7	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U22
33	GPMC & no MMC2 & no OSPI	GPIO0_16	7	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U21
76	GPMC & no MMC2 & no OSPI	GPIO0_17	7	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U20
173		GPIO0_18	7	BOOTMODE03 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V25
84		GPIO0_19	7	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T20
36	OSPI & no MMC2 & no GPMC	GPIO0_2	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	P22
48		GPIO0_20	7	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T21
86		GPIO0_21	7	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V24
40		GPIO0_22	7	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W25
115		GPIO0_23	7	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC25
171		GPIO0_24	7	BOOTMODE09 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB25
21		GPIO0_25	7	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AA25
26		GPIO0_26	7	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W24
24		GPIO0_27	7	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	Y24
25		GPIO0_28	7	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AD25
23		GPIO0_29	7	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
76	OSPI & no MMC2 & no GPMC	GPIO0_3	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	L25
22		GPIO0_30	7	BOOTMODE15 pin, has 100K PU on SOM for compatibly with VAR-SOM-AM62; For boot enablement, Pin is Pulled low internally on SOM during boot. Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC24
59	GPMC & no MMC2 & no OSPI	GPIO0_31	7	Available in SOM with "GPMC" configuration;	Y25
198	no AC	GPIO0_32	7	Available in SOM without "AC" configuration	R25
36	GPMC & no MMC2 & no OSPI	GPIO0_33	7	Available in SOM with "GPMC" configuration;	R24
18	no AC & no GPMC	GPIO0_34	7	Available in SOM without "AC" and without "GPMC" configuration	T25
196	no AC & GPMC	GPIO0_34	7	Available in SOM without "AC" and with "GPMC" configuration	T25
200	no AC	GPIO0_35	7	Available in SOM without "AC" configuration	U24
47	GPMC & no MMC2 & no OSPI	GPIO0_36	7	Available in SOM with "GPMC" configuration;	T24
199	no AC	GPIO0_37	7	Available in SOM without "AC" configuration	AA24
175		GPIO0_38	7		AD24
20	no AC & no GPMC	GPIO0_39	7	Available in SOM without "AC" and without "GPMC" configuration	P24
197	no AC & GPMC	GPIO0_39	7	Available in SOM without "AC" and with "GPMC" configuration	P24
35	OSPI & no MMC2 & no GPMC	GPIO0_4	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	N24
35	GPMC & no MMC2 & no OSPI	GPIO0_40	7	Available in SOM with "GPMC" configuration;	P25
100	GPMC & no MMC2 & no OSPI	GPIO0_41	7	Available in SOM with "GPMC" configuration;	T23
102	GPMC & no MMC2 & no OSPI	GPIO0_42	7	Available in SOM with "GPMC" configuration;	U23
174		GPIO0_43	7	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	T22
176		GPIO0_44	7	Internal signal pulled up to SOM_PGOOD using 4.7K resistor; In SOMs with "AC" configuration pins are used for Codec I2C- Do not alter pinmux!	U25
100	OSPI & no MMC2 & no GPMC	GPIO0_5	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	N25
53		GPIO0_51	7	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	AC23
52		GPIO0_52	7	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	AE23
50		GPIO0_57	7	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	AD21

Pin#	Assy	Pin Function	Alt#	Notes	Ball
51		GPIO0_58	7	Used internally with "WBD" or "WBE", Function can be released if BT Function disabled	AC21
59	OSPI & no MMC2 & no GPMC	GPIO0_6	7	Available in SOM with "OSPI" configuration; Pin referenced to 1.8V	M24
31	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	GPIO0_65	7	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L21
33	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	GPIO0_66	7	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	L20
35	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	GPIO0_67	7	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K22
102	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	GPIO0_68	7	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K23
76	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	GPIO0_69	7	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K21
79		GPIO0_7	7	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N21
100	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	GPIO0_70	7	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K24
47	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	GPIO0_71	7	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	J25
59	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	GPIO0_72	7	Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V)	K25
1	no EC	GPIO0_73	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	B18
97	no EC	GPIO0_74	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series 33R resistor;	B17
11	no EC	GPIO0_75	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A18

Pin#	Assy	Pin Function	Alt#	Notes	Ball
9	no EC	GPIO0_76	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	C17
5	no EC	GPIO0_77	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A17
3	no EC	GPIO0_78	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	C16
15	no EC	GPIO0_79	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A15
75		GPIO0_8	7	Pin referenced to 1.8V in SOM with "OSPI" configuration;	N22
16	no EC	GPIO0_80	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series EMI filter;	A16
4	no EC	GPIO0_81	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	B15
6	no EC	GPIO0_82	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	B16
10	no EC	GPIO0_83	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A14
12	no EC	GPIO0_84	7	Available in SOM without "EC" configuration; By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	B14
30		GPIO0_85	7	Pin is referenced to 3.3V, and has an internal 1.47K Pull Up. In "RG2CM" configuration pin is routed via on SOM 1.8<->3.3V voltage translator. Do not alter pinmux with "EC" configuration	F16
74		GPIO0_86	7	Pin is referenced to 3.3V. In "RG2CM" configuration pin is routed via on SOM 1.8<->3.3V voltage translator; Do not alter pinmux with "EC" configuration	F17
113		GPIO0_87	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A20
96		GPIO0_88	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V; Includes series 33R resistor;	D16
73		GPIO0_89	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	B19
70		GPIO0_9	7	Pin referenced to 1.8V in SOM with "OSPI" configuration;	P21
177		GPIO0_90	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A21
56		GPIO0_91	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	D17
55		GPIO1_0	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	A19
120		GPIO1_1	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	F19
69		GPIO1_10	7		F23
117		GPIO1_11	7		F24

Pin#	Assy	Pin Function	Alt#	Notes	Ball
72		GPIO1_12	7		F25
39		GPIO1_13	7		G23
43		GPIO1_14	7		G20
191	no TP	GPIO1_15	7	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_FRM” signal and cannot be used externally	D20, LBES5PL2XL.4 (“WBE” or ”WBD”)
68		GPIO1_16	7		E20
189	no TP	GPIO1_17	7	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_CLK” signal.	B21, LBES5PL2XL.8 (“WBE” or ”WBD”)
187	no TP	GPIO1_18	7	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_RXD” signal.	B20, LBES5PL2XL.6 (“WBE” or ”WBD”)
193	no TP	GPIO1_19	7	Available in SOM without TP In “WBD” or ”WBE” configuration connected also via buffer to Murata 2EL/2DL “SPI_TXD” signal.	C21, LBES5PL2XL.7 (“WBE” or ”WBD”)
57		GPIO1_2	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	D19
83		GPIO1_20	7	Used as debug UART on Variscite base board	A22
85		GPIO1_21	7	Used as debug UART on Variscite base board; Internal signal pulled up to SOM_PGOOD using 4.7K resistor;	B22
44		GPIO1_24	7		B23
46		GPIO1_25	7		F20
88		GPIO1_26	7		B25
87		GPIO1_27	7		A24
92		GPIO1_28	7		C24
90		GPIO1_29	7		B24
122		GPIO1_3	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	E19
29		GPIO1_30	7		C25
81		GPIO1_4	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	E16
65		GPIO1_42	7	Bank voltage set on SOM 1.8V/3.3V	H25
61		GPIO1_43	7	Bank voltage set on SOM 1.8V/3.3V	H22
63		GPIO1_44	7	Bank voltage set on SOM 1.8V/3.3V	H23
62		GPIO1_45	7	Bank voltage set on SOM 1.8V/3.3V	H21
60		GPIO1_46	7	Bank voltage set on SOM 1.8V/3.3V	J24
64		GPIO1_47	7	Bank voltage set on SOM 1.8V/3.3V	H20
80		GPIO1_48	7	When booting from SD card, should be used as SD card detect or pulled low until after SYS_NRSTIN_3V3 rise +1ms (Read by boot ROM in boot from MMCSD1).	D23
124		GPIO1_49	7		D24
71		GPIO1_5	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	E17
94		GPIO1_50	7		G22
82		GPIO1_51	7		G21

Pin#	Assy	Pin Function	Alt#	Notes	Ball
54		GPIO1_6	7	By default, referenced to 3.3V, In "RG2CM" configuration referenced to 1.8V;	C19
45		GPIO1_7	7		D25
41		GPIO1_8	7		E25
17		GPIO1_9	7		E24

Table 96: MCU GPIO Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
153	no LD0	MCU_GPIO0_1	7		E10
147	no LD0	MCU_GPIO0_10	7		D7
142	no LD0	MCU_GPIO0_11	7		C7
143	no LD0	MCU_GPIO0_12	7		C6
157	no RFCNTL	MCU_GPIO0_13	7		E8
155	no RFCNTL	MCU_GPIO0_14	7		D6
156	no RFCNTL	MCU_GPIO0_15	7		F8
154	no RFCNTL	MCU_GPIO0_16	7		E7
146	no COEX	MCU_GPIO0_17	7	Used for MCU_I2C function, connected also to PMIC	E11
148	no COEX	MCU_GPIO0_18	7	Used for MCU_I2C function, connected also to PMIC	D11
140	no LD0	MCU_GPIO0_19	7	Used for WKUP_I2C function, connected also to PMIC	A13
150	no LD0	MCU_GPIO0_2	7		C10
141	no LD0	MCU_GPIO0_20	7	Used for WKUP_I2C function, connected also to PMIC	C11
128		MCU_GPIO0_21	7		F14
151	no LD0	MCU_GPIO0_3	7		B11
152	no LD0	MCU_GPIO0_4	7		D10
91	no BTPCM	MCU_GPIO0_5	7		B6
99	no BTPCM	MCU_GPIO0_6	7		C8
58	no BTPCM	MCU_GPIO0_7	7		B8
93	no BTPCM	MCU_GPIO0_8	7		B7
145	no LD0	MCU_GPIO0_9	7		D8

8.22 Power

8.22.1 Power

Table 97: Power

Pin#	Assy	Pin Function	Alt#	Notes	Ball
32, 34, 103, 105, 107, 109, 111		VCC_SOM		SOM Power	VCC_SOM
36	no GPMC & no OSPI & no MMC2	VCC_SOM		SOM Power	VCC_SOM
36	MMC2 & no GPMC & no OSPI & no (WBE or WBE)	VDDSHV6		Available in SOM with "MMC2"; Referenced to pin 36 supply (1.8V/3.3V) "no MMC2" configuration: * Not Connected "MMC2" configuration: VDDSHV6 1.8V/3.3V voltage input. Must supply one option: 1.8 or 3.3V, Use SOM pin 49 to sequence 1.8 or 3.3V supply. The following SOM pins are referenced to this voltage: 31,33,35,47,59,76,100,102	1B10
106		USB0_VBUS		USB PHY power pin (5V) input	Y7
104		USB1_VBUS		USB PHY power pin (5V) input	Y10
49		SOM_PGOOD		SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw allowed.	SOM_PGOOD

8.22.2 Ground

Table 98: Digital Ground Pins

Pin#	Assy	Pin Function	Alt#	Notes	Ball
2, 7, 8, 13, 14, 19, 27, 28, 37, 47, 59, 66, 67, 76, 78, 89, 95, 101, 112, 118, 126, 132, 138, 139, 144, 149, 158, 159, 169, 172, 178, 179, 185		GND		Digital ground	GND
47, 59, 76	no GPMC & no OSPI & no MMC2	GND		Digital ground	GND
195	AC	AGND		Audio ground	AGND

8.23 System Control

8.23.1 General SOM control Signals

Table 99: General SOM Control Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
49		SOM_PGOOD		SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw is allowed.	SOM_PGOOD
98		SYS_NRSTIN_3V3		SOM reset input pin. Internally pulled up. Connected via diode to internal (not exposed) 1.8V MCU_PORz ball. Once it is asserted low, CPU MCU and MAIN domains perform cold reset.	H6 (via diode)

8.23.2 Main domain System Signals

Table 100: Main System Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		EXT_REFCLK1	0	External clock input to Main Domain	C25
17		MAIN_ERRORn	5	Error signal output from MAIN Domain ESM	E24
35	GPMC & no MMC2 & no OSPI	MAIN_ERRORn	5	Error signal output from MAIN Domain ESM Available in SOM with "GPMC" configuration;	P25
68		MAIN_ERRORn	5	Error signal output from MAIN Domain ESM	E20
21		OBSCLK0	8	Main Domain Observation clock output for test and debug purposes only. BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AA25
88		OBSCLK1	3	Main Domain Observation clock output for test and debug purposes only	B25
134		RESET_REQz	0	Main Domain external warm reset request input. Internal signal pulled up to SOM_PGOOD using 10K resistor.	G24
29		SYSCLKOUT0	3	Main Domain system clock output (divided by 4) for test and debug purposes only	C25

8.23.3 MCU domain System Signals

Table 101: MCU System Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
136		MCU_ERRORn		Error signal output from MCU Domain ESM. Pin is referenced to 1.8V; Connected also to PMIC via on SOM 1.8<->3.3V voltage translator	G6
153	no LD0	MCU_EXT_REFCLK0	3	External input to MCU Domain	E10
156	no RFCNTL	MCU_EXT_REFCLK0	4	External input to MCU Domain	F8
153	no LD0	MCU_OBSCLK0	1	MCU Domain Observation clock output for test and debug purposes only	E10
98		SYS_NRSTIN_3V3	0	SOM reset input pin. Connected via diode to internal (not exposed) 1.8V MCU_PORz signal. Internally pulled up. Once it is asserted low, CPU MCU and MAIN domains perform cold reset.	H6 (via diode)
128		MCU_RESETSTATz	0	MCU Domain warm reset status output	F14
130		MCU_RESETz	0	MCU and Main Domain warm reset. Internal signal pulled up to SOM_PGOOD using 10K resistor.	F11
153	no LD0	MCU_SYSCLKOUT0	2	MCU Domain system clock output (divided by 4) for test and debug purposes only	E10

8.23.4 Boot configuration

The VAR-SOM-AM62P can be boot from the following sources:

- Internal source - eMMC Flash memory
- External source - SD Card

The AM62Px BOOTMODE [15:0] pins determine the boot source.
On SOM, logic circuitry drives the BOOTMODE3, BOOTMODE9 lines on time of boot.
The rest of BOOTMODE pins are strapped internally by PU/PD resistors.

Boot source selection is done via **pin 42** of the SOM-DIMM 200 pin connector.

Table 102: BOOT_SEL signal SOM-DIMM 200 pin connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
42		BOOT_SEL		Controls internal OR external boot source; Internal signal pulled up to SOM_PGOOD using 1K resistor; 0=EXT. BOOT 1/Float=INT. BOOT	INT. LOGIC

BOOT_MODE[15:0] are also exposed on the SOM SO-DIMM 200 in order to allow support of other boot sources.

ATTENTION

External drivers connected to BOOTMODE lines exposed to the connector should be disabled on during reset (SYS_NRSTIN_3V3 rise +1ms), otherwise they may change the boot option and the SOM will not boot.

Table 103: BOOTMODE signals on SO-DIMM 200 pin Connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	GPMC & no MMC2 & no OSPI	BOOTMODE00	10	Available in SOM with "GPMC" configuration; BOOTMODE00 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U22
33	GPMC & no MMC2 & no OSPI	BOOTMODE01	10	Available in SOM with "GPMC" configuration; BOOTMODE01 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U21
76	GPMC & no MMC2 & no OSPI	BOOTMODE02	10	Available in SOM with "GPMC" configuration; BOOTMODE02 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	U20
173		BOOTMODE03	10	BOOTMODE03 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V25
84		BOOTMODE04	10	BOOTMODE04 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T20
48		BOOTMODE05	10	BOOTMODE05 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	T21
86		BOOTMODE06	10	BOOTMODE06 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	V24
40		BOOTMODE07	10	BOOTMODE07 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W25
115		BOOTMODE08	10	BOOTMODE08 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC25
171		BOOTMODE09	10	BOOTMODE09 pin, Driven on SOM during boot; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB25
21		BOOTMODE10	10	BOOTMODE10 pin, 10K PU on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AA25
26		BOOTMODE11	10	BOOTMODE11 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	W24
24		BOOTMODE12	10	BOOTMODE12 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	Y24
25		BOOTMODE13	10	BOOTMODE13 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AD25
23		BOOTMODE14	10	BOOTMODE14 pin, 100K PD on SOM; Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AB24
22		BOOTMODE15	10	BOOTMODE15 pin, has 100K PU on SOM for compatibly with VAR-SOM-AM62; For boot enablement, Pin is Pulled low internally on SOM during boot. Do not drive until after SYS_NRSTIN_3V3 rise +1ms	AC24

9. Assembly Options

To make the solution as Flexible as possible the following assembly options were added. The assembly options help customers to order the SOM variant that includes only the needed interfaces with a lower cost.

9.1 GPMC/OSPI/MMC2

The SOM can be ordered with the GPMC/OSPI/MMC2 related pins exposed.

Table 104: GPMC/OSPI/MMC2 assembly option

	Default SOM option (no GPMC & no OSPI & no MMC2)		Special SOM option (GPMC)		Special SOM option (OSPI)		Special SOM option (MMC2)	
Pin #	Pin Function	Ball	Pin Function	Ball	Pin Function	Ball	Pin Function	Ball
31	NC	NC	GPMC0_AD0	U22	OSPI0_CLK	P23	MMC2_DAT3	L21
33	NC	NC	GPMC0_AD1	U21	OSPI0_LBCLKO	N23	MMC2_DAT2	L20
35	NC	NC	GPMC0_DIR	P25	OSPI0_D1	N24	MMC2_DAT1	K22
36	VCC_SOM	VCC_SOM	GPMC0_OEN_REN	R24	OSPI0_DQS	P22	VDDSHV6	1B10
47	GND	GND	GPMC0_BE1N	T24	OSPI0_CSN3	L23	MMC2_SDCD	C24
59	GND	GND	GPMC0_CLK	Y25	OSPI0_D3	M24	MMC2_SDWP	K25
76	GND	GND	GPMC0_AD2	U20	OSPI0_D0	L25	MMC2_CLK	K21
100	NC	NC	GPMC0_CSN0	T23	OSPI0_D2	N25	MMC2_CMD	K24
102	NC	NC	GPMC0_CSN1	U23	OSPI0_CSN0	M25	MMC2_DAT0	K23

9.2 Analog Audio Codec

The SOM can be ordered without Audio Codec chip assembled. This allows reducing the overall cost of the product in case the Analog Audio Codec is not used.
when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

Note: For layout reasons, in case of SOM without Audio Codec assembled, the export of CPU balls T25, P24 depends on GPMC assembly option as follows:

Table 105: (no AC & no GPMC/ no AC & GPMC) assembly option

	SOM option (no AC & no GPMC)		SOM option (no AC & GPMC)	
Pin #	Pin Function	Ball	Pin Function	Ball
18	GPMC0_WEN	T24	NC	NC
20	GPMC0_WPN	P24	NC	NC
196	NC	NC	GPMC0_WEN	T25
197	NC	NC	GPMC0_WPN	P24

9.3 DSI, LD0

The SOM can be ordered with the DSI Interface signals exposed instead of LVDS0 signals. In “DSI” configuration, optional configuration “LD0” can be ordered, enabling to export both DSI and LVDS0. In “LD0” configuration signal are exported to SOM connector pins instead of MCU/WKUP interface signals.

Table 106: (no DSI & no LD0, DSI, DSI & LD0) assembly option

	Default SOM option (no DSI & no LD0)		Special SOM option (DSI)		Special SOM option (DSI & LD0)	
Pin #	Pin Function	Ball	Pin Function	Ball	Pin Function	Ball
140	WKUP_I2C0_SCL	A13	WKUP_I2C0_SCL	A13	OLDI0_A0N	AE20
141	WKUP_I2C0_SDA	C11	WKUP_I2C0_SDA	C11	OLDI0_A1N	AC19
142	WKUP_UART0_CTSN	C7	WKUP_UART0_CTSN	C7	OLDI0_A0P	AD20
143	WKUP_UART0_RTSN	C6	WKUP_UART0_RTSN	C6	OLDI0_A1P	AD19
145	WKUP_UART0_RXD	D8	WKUP_UART0_RXD	D8	OLDI0_A2N	AA19
147	WKUP_UART0_TXD	D7	WKUP_UART0_TXD	D7	OLDI0_A2P	AB19
150	MCU_SPI0_CLK	C10	MCU_SPI0_CLK	C10	OLDI0_CLK0N	AE18
151	MCU_SPI0_D0	B11	MCU_SPI0_D0	B11	OLDI0_A3N	AD18
152	MCU_SPI0_D1	D10	MCU_SPI0_D1	D10	OLDI0_CLK0P	AE17
153	MCU_SPI0_CS1	E10	MCU_SPI0_CS1	E10	OLDI0_A3P	AE19
160	OLDI0_A1N	AC19	DSI0_TXN1	AB13	DSI0_TXN1	AB13
161	OLDI0_A0N	AE20	DSI0_TXN0	AD11	DSI0_TXN0	AD11
162	OLDI0_A1P	AD19	DSI0_TXP1	AB14	DSI0_TXP1	AB14
163	OLDI0_A0P	AD20	DSI0_TXP0	AD12	DSI0_TXP0	AD12
164	OLDI0_A2N	AA19	DSI0_TXN2	AC12	DSI0_TXN2	AC12
165	OLDI0_A3N	AD18	DSI0_TXN3	AE14	DSI0_TXN3	AE14
166	OLDI0_A2P	AB19	DSI0_TXP2	AC13	DSI0_TXP2	AC13
167	OLDI0_A3P	AE19	DSI0_TXP3	AE15	DSI0_TXP3	AE15
168	OLDI0_CLK0N	AE18	DSI0_TXCLKN	AA12	DSI0_TXCLKN	AA12
170	OLDI0_CLK0P	AE17	DSI0_TXCLKP	AA13	DSI0_TXCLKP	AA13

9.4 Dual band Wi-Fi and BT/BLE combo

The SOM can be ordered with Dual band Wi-Fi and BT/BLE combo chip assembled.
In case ordered, additional assembly options related to Wi-Fi and BT/BLE chip are available.

NOTE

These assembly options were not tested yet; for further support, please contact sales@variscite.com

9.4.1 BTPCM

Table 107: (no BTPCM/ BTPCM) assembly option

	SOM option (no AC & no GPMC)		SOM option (no AC & GPMC)	
Pin #	**Pin Function**	**Ball**	**Pin Function**	**Ball**
58	MCU_UART0_CTSN	B8	BT_PCM_IN_1V8	LBES5PL2xL.93
91	MCU_UART0_RXD	B6	BT_PCM_CLK_1V8	LBES5PL2xL.57
93	MCU_UART0_RTSN	B7	BT_PCM_OUT_1V8	LBES5PL2xL.59
99	MCU_UART0_TXD	C8	BT_PCM_SYNC_1V8	LBES5PL2xL.61

9.4.2 RFCNTL

Table 108: (no RFCNTL/RFCNTL) assembly option

	SOM option (no AC & no GPMC)		SOM option (no AC & GPMC)	
Pin #	**Pin Function**	**Ball**	**Pin Function**	**Ball**
154	MCU_MCAN1_RX	E7	RF_CNTL3_1V8	LBES5PL2xL.25
155	MCU_MCAN0_RX	D6	RF_CNTL0_1V8	LBES5PL2xL.27
156	MCU_MCAN1_TX	F8	RF_CNTL4_1V8	LBES5PL2xL.24
157	MCU_MCAN0_TX	E8	RF_CNTL1_1V8	LBES5PL2xL.26

9.4.3 COEX

Table 109: (no COEX/COEX) assembly option

	SOM option (no AC & no GPMC)		SOM option (no AC & GPMC)	
Pin #	**Pin Function**	**Ball**	**Pin Function**	**Ball**
146	MCU_I2C0_SCL	E11	COEX_SIN_1V8	LBES5PL2xL.69
148	MCU_I2C0_SDA	D11	COEX_SOUT_1V8	LBES5PL2xL.70

9.4.4 ANT2

Two antennas assembled with Wi-Fi and BT/BLE combo chip: ANT1 for Wi-Fi, ANT2 for BT and 802.15.4

9.5 Resistive Touch

The SOM can be ordered without Resistive Touch controller assembled. This allows reducing the overall cost of the product in case the Resistive Touch is not used.
when not assembled, SoC balls are exported to SOM connector instead of Resistive Touch interface pins.

NOTE

[1] The utilization of the same SPI channel by WBE and TP assembly choices makes it unfeasible to assemble them simultaneously.

9.6 Ethernet PHY

The SOM can be ordered without Ethernet PHY chip assembled; it allows reducing the overall cost of the product in case the Ethernet Interfaces are not used.
when not assembled, SoC balls are exported to SOM connector instead of Ethernet interface pins.

9.7 LPDDR4

The SOM can be ordered with different RAM size capacities, it allows reducing the overall cost of the product in case lower RAM size is sufficient.

9.8 eMMC

The SOM can be ordered with different eMMC size capacities, it allows reducing the overall cost of the product in case lower eMMC size is sufficient.

9.9 RG2CM

The SOM can be ordered with RGMII2/RMII2 signals referenced to 1.8V, for compatibility with other VAR-SOM family modules in which RGMII2 operates at 1.8V.
Note that with RG2CM configuration, in case of “no EC”, RGMII1/RMII1 signals exported via SOM connectors will also run at 1.8V.

The voltage is set according to resistor assembly which provides power to VDDSHV2 domain of CPU.
In “no RG2CM” configuration voltage will be set to 3.3V.
In “RGCM” configuration voltage will be set to 1.8V.

10. Electrical Specifications

10.1 Absolute Maximum Ratings

Table 110: Absolute Maximum Ratings

Pin #	Min	Max	Units	Comments
VCC_SOM	-0.3	3.6	V	
USB0_VBUS, USB1_VBUS	-0.3	5.25	V	
VDDSHV6	-0.3	3.63	V	
ESD damage immunity Human Body Model (HBM)	--	+/-1000	V	Per ANSI/ESDA/JEDEC JS-001
ESD damage immunity Charge Device Model (CDM)	--	+/-250	V	Per ANSI/ESDA/JEDEC JS-002

10.2 Operating Conditions

Table 111: Operating Ranges

Parameter		Min.	Typ.	Max.	Unit
VCC_SOM		3.25	3.3	3.45	V
USB0_VBUS, USB1_VBUS		4.75	5	5.25	V
VDDSHV6	1.8	1.71	1.8	1.89	V
	3.3	3.135	3.3	3.465	

10.3 Peripheral Voltage Levels

Most of the peripheral interface lines used as inputs or output to the VAR-SOM-AM62P use 3.3V levels, with the below exceptions for the following interfaces:

USB/MIPI-CSI/DSI/LVDS: Interfaces follow a different standard since they are high-speed signals.

MMC1: (SDIO lines) interface IOs will change voltage between 3.3V and 1.8V depending on the SD card capabilities. With other alternative functions, the user can determine the voltage MMC1 IOs bank will be 1.8V or 3.3V.

MMC2: interface available in case SOM is ordered with "MMC2." interface IOs will run at voltage 1.8V or 3.3V levels depending on the power fed to VDDSHV6 (pin 36) (1.8V/3.3V)

RGMII1/RMI1, RGMII2/RMII2:
In “no RG2CM” configuration – pins will be referenced to 3.3V
In “RG2CM” configuration – pins will be referenced to 1.8V

OSPI: interface available in case SOM is ordered with "OSPI." interface IOs will run at 1.8V levels.

BTPCM, RFCNTL, COEX: Signal source is Signal source is WIFI module. Interfaces’ IOs will run at 1.8V levels.

MCU_ERRORN: Signal is refenced to 1.8V level

10.4 Power Consumption

Table 112: VAR-SOM-AM62P Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.35V	TBD	TBD	Linux up, Wi-Fi connected and Iperf is running 802.11 ax 5GHz
Run	3.35V	TBD	TBD	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	3.35V	TBD	TBD	Linux up. Ethernet0 & Ethernet1 running benchmark
Run	3.35V	TBD	TBD	Linux up. Ethernet0, Ethernet1, Wi-Fi module up
FHD video playback	3.35V	TBD	TBD	On 800x400 LCD
Standby	3.35V	TBD	TBD	Memory retention mode
Off	3.35V	TBD	TBD	All power rails are Off

NOTE

HW Setup:
VAR-SOM-AM62P_1400C_2048R_16G_AC_EC_TP_WBD_IT V1.0

Note: *The Wi-Fi module needs a power source that can provide a peak current of ~1000mA@3.3V during DPD calibration when the firmware is downloaded, even though its max continuous supply current during transmission/reception is less.*
Module calibration occurs:

- *When the Module is initially powered up.*
- *The module is reset.*
- *When the radio is initialized.*
- *Every two minutes after the radio is initialized.*

DISCLAIMER:

The power consumption measurements apply only to limited operation scenarios. Actual power consumption may vary depending on the interfacing peripherals and user application modes; Users must conduct testing per their specific operation scenarios.

Depending on the specific use cases and end product system design, an appropriate thermal solution should be applied.

11. Environmental Specifications

Table 113: Environmental Specifications

Parameter	Min	Max
Extended Operating Temperature Range	0°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Prediction Method Model: Telcordia Technologies Special Report SR-332, Issue 4 50°C, GB	> TBD Khrs	

Note: Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

12. Mechanical

12.1 Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-3.0-M2-B**

12.2 Thermal Management

Certain operation scenarios may prompt the use of an external heat dissipation solution.
To handle intensive applications where thermal management is required, Variscite offers a heat sink designed for the VAR-SOM-AM62P family:

Variscite PN: TBD

DISCLAIMER:
Implemented solution may vary depending on the device operation scenario as well as its mechanical design. Thermal solution must be evaluated.

12.3 SOM Dimensions

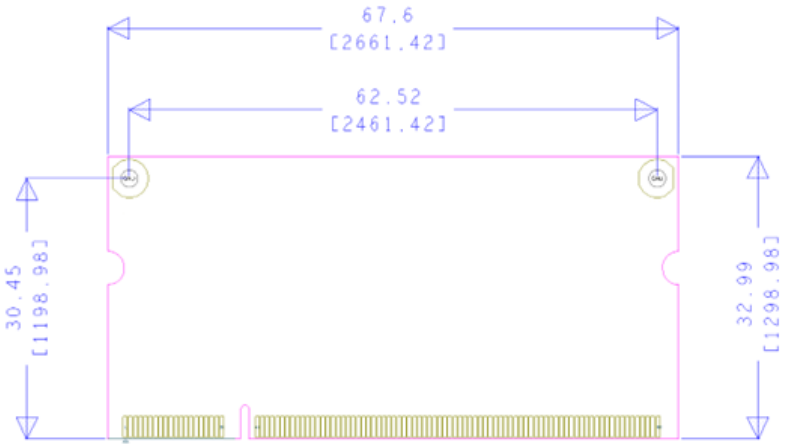


Figure 5: VAR-SOM-AM62P Mechanics in millimeters [mils]

12.3.1 CAD Files

CAD files are available for download at http://www.variscite.com/

13. Legal Notice

Variscite Ltd. (“Variscite”) products and services are sold subject to Variscite terms and conditions of sale, delivery and payment supplied at the time of order acknowledgement.

Variscite warrants performance of its products to the specifications in effect at the date of shipment. Variscite reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant product information from Variscite to verify that their reference is current.

Testing and other quality control techniques are utilized to the extent that Variscite deems necessary to support its warranty.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

In order to minimize risks associated with customer applications, the customer must use adequate design and operating safeguards to minimize inherent or procedural hazards. Variscite is not liable for applications assistance or customer product design. The customer is solely responsible for its selection and use of Variscite products. Variscite is not liable for such selection or use or for use of any circuitry other than circuitry entirely embodied in a Variscite product.

Variscite products are not intended for use in life support systems, appliances, nuclear systems or systems where malfunction can reasonably be expected to result in personal injury, death or severe property or environmental damage. Any use of products by the customer for such purposes is at the customer’s own risk.

Variscite does not grant any license (express or implied) under any patent right, copyright, mask work right or other intellectual property right of Variscite covering or relating to any combination, machine, or process in which its products or services might be or are used. Any provision or publication of any third party’s products or services does not constitute Variscite’s approval, license, warranty or endorsement thereof. Any third-party trademarks contained in this document belong to the respective third-party owner.

Reproduction of information from Variscite datasheets is permissible only if reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices (including this notice) and conditions. Variscite is not liable for any un-authorized alteration of such information or for any reliance placed thereon.

Any representations made, warranties given, and/or liabilities accepted by any person which differ from those contained in this datasheet or in Variscite’s standard terms and conditions of sale, delivery and payment are made, given and/or accepted at that person’s own risk. Variscite is not liable for any such representations, warranties or liabilities or for any reliance placed thereon by any person.

14. Warranty Terms

Variscite guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Variscite's sole liability shall be for Variscite, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Disclaimer of Warranty

THIS WARRANTY IS MADE IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL VARISCITE BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL VARISCITE BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT. BY ORDERING THE SOM, THE CUSTOMER APPROVES THAT THE VARISCITE SOM, HARDWARE AND SOFTWARE, WAS THOROUGHLY TESTED AND HAS MET THE CUSTOMER'S REQUIREMETS AND SPECIFICATIONS.

15. Contact Information

Headquarters:
Variscite Ltd.

9, Hamelacha Street
Lod
P.O.B 1121
Airport City, 70100
ISRAEL

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

Sales: sales@variscite.com

Technical Support: support@variscite.com

Corporate Website: www.variscite.com