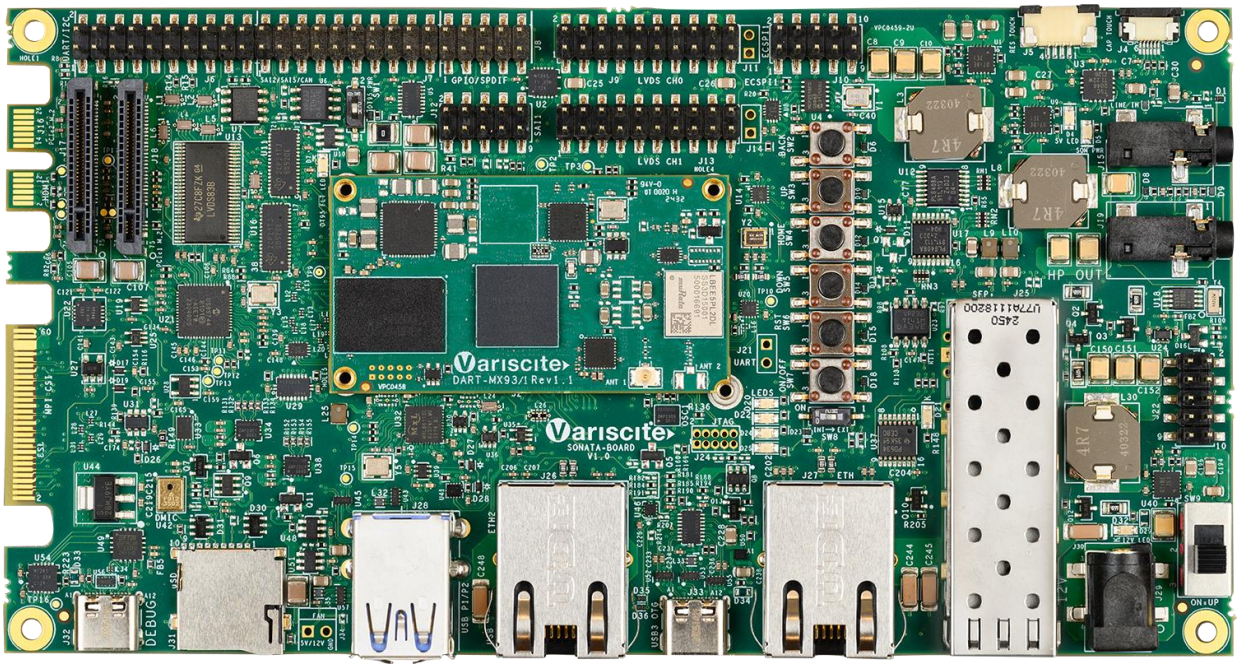
VARISCITE LTD

Sonata Board V1.1 Datasheet

Carrier-board for:

DART-MX8M
DART-MX8M-MINI
DART-MX8M-PLUS
DART-MX91
DART-MX93
DART-MX95



VARISCITE LTD.

Sonata-Board Datasheet

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1 Revision History

Revision	Date	Notes
1.0	Oct, 2024	Initial – Preliminary
1.1	Apr, 2025	Sonata Rev 1.1 changes

2 Table of Contents

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4 Overview

This chapter provides an overview of the Sonata-Board.

4.1 General Information

Sonata-Board is a complete development board, utilizing all of the DART-MX8M, DART-MX8M-MINI, DART-MX8M-PLUS, DART-MX91, DART-93 and DART-MX95 System-on-Modules features. It is assembled with large variety of user and debug interfaces enabling it to serve as both a complete development kit or a stand-alone end-product.

4.1.1 Supported Variscite products

- DART-MX8M
- DART-MX8M-MINI
- DART-MX8M-PLUS
- DART-MX91
- DART-MX93
- DART-MX95

- VAR-EXT-HDMI
- VAR-EXT-CB8-B
- VCAM-5640S

- 7” Capacitive touch LCD

4.1.2 Supporting O.S

- Linux
- Android

4.1.3 Additional information

Board schematics as well as mechanical CAD database is available for download at Variscite Web Site: www.variscite.com.

Valuable information including board schematics in Orcad format, Allegro layout files, pre-built software images, and more can be located on the Variscite FTP: ftp://ftp.variscite.com/ site Please contact Variscite support for access details.

Additional SW support information can be found: http://variwiki.com/

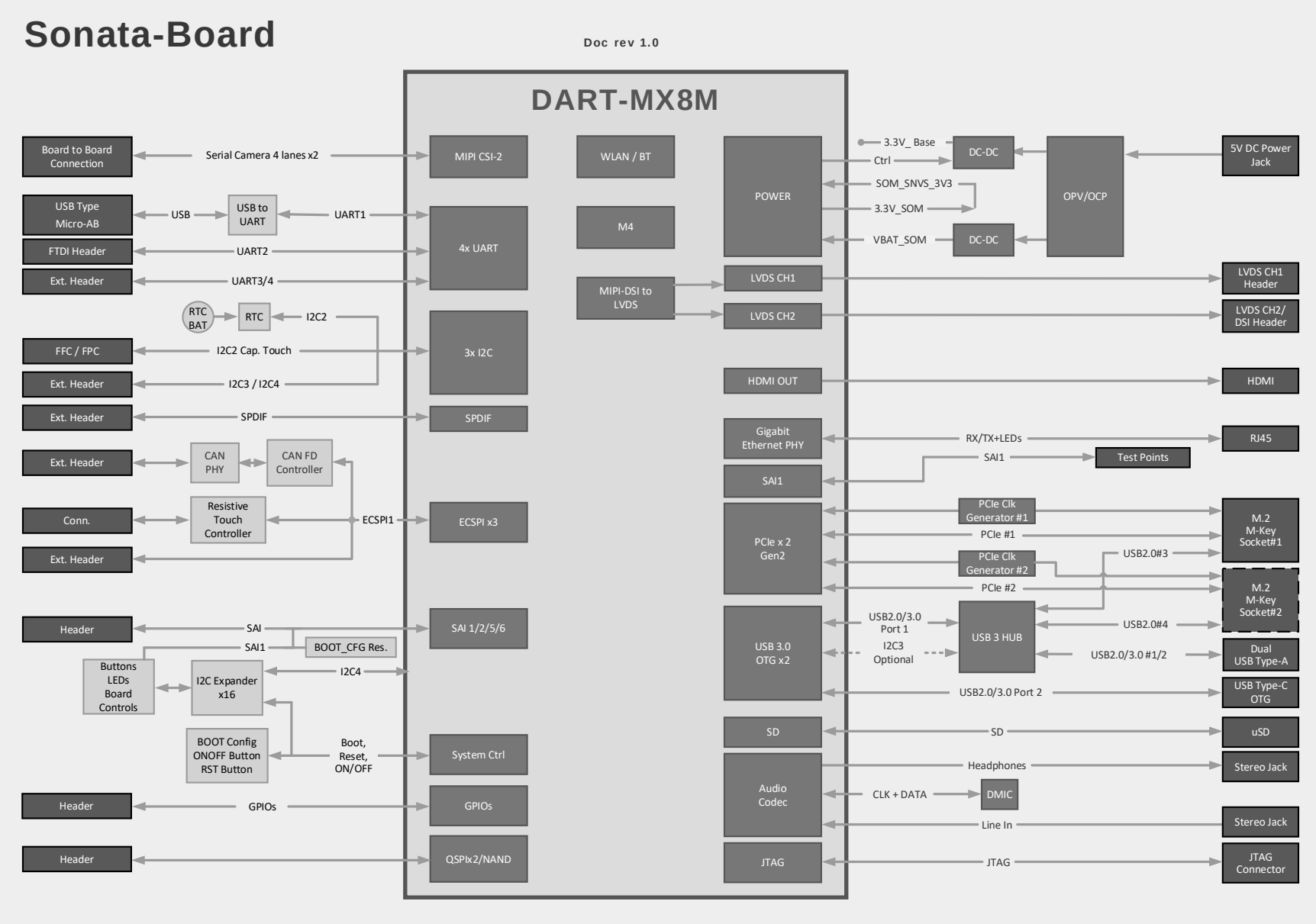
For more information contact Variscite support at mailto:support@variscite.com.

5 Sonata-Board features summary

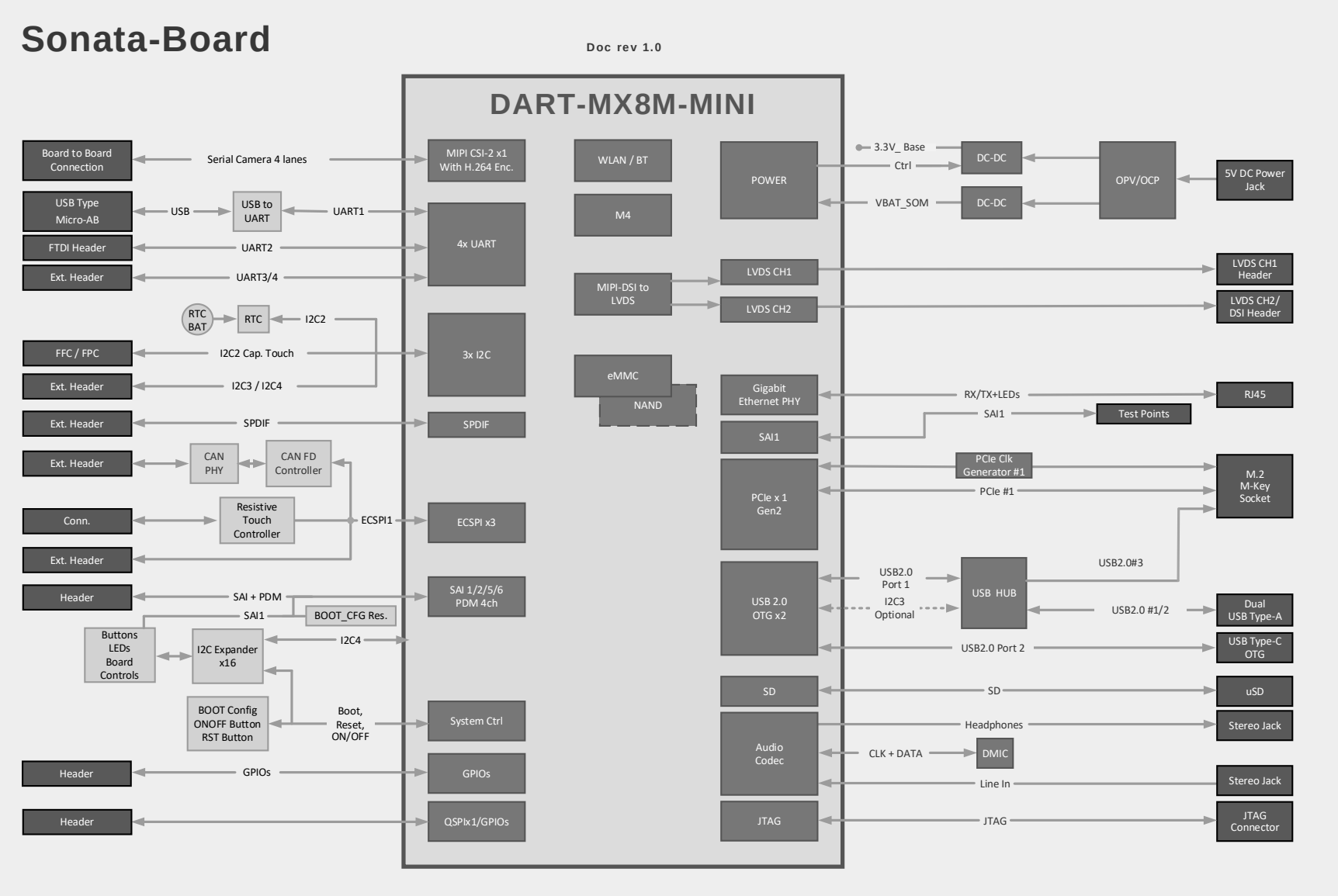
- 3 x 90 pin high density connectors, compatible with:
  - DART-MX8M
  - DART-MX8M-MINI
  - DART-MX8M-PLUS
  - DART-MX91
  - DART-MX93
  - DART-MX95
- Display
  - 2x18 bit LVDS Interface supporting Variscite's 7" TFT capacitive touch LCD
  - 18bit Parallel RGB. DT91, DT93 only
  - HDMI 2.0a (Via Extension Card). DT8M& and DT8MP
  - DSI
- Touch panel interface
  - Capacitive - I2C based
  - Resistive – SPI based
- Ethernet
  - 2 x 10/100/1000BaseT – RJ45
  - 10GbE – SFP+ (Copper/Fiber). DT95 only
- PCIe
  - 2xM.2 M-Key PCIe interfaces
- USB
  - USB3.0 OTG Type C
  - USB3.0 Host Type A x 2
- AUDIO
  - 3.5mm Headphones jack
  - 3.5mm Line in jack
  - Digital Microphone
- µSD-Card slot
- Camera
  - Serial interface – Dual MIPI CSI x4 lanes each.
- Debug
  - USB debug (UART1) – USBC type.
  - JTAG – Header
- RTC
  - DS1337U+ Chip

- Security Flash-memory-based trusted platform module (TPM)
  - ST33KTPM2I Chip
  - I2C interface
- Additional
  - SAI (Serial Audio Interface) – Headers, Test Points
  - UART, QSPI, ECSPI, I2C, GPIO's – Headers
  - CAN Bus - SPI based controller with 5Mb/s or 12Mb/s CAN PHY – Header
    DT8M-PLUS only – 2nd 5Mb/s or 12Mb/s CAN PHY - Header
  - General purpose LEDs, Buttons
- Power
  - 12V DC Input. - 2.0mm DC jack / 2 pin Terminal Block
  - 5V/12V DC Out – 2 pin Header FAN Power
  - RTC Backup battery (Not Assembled) - CR1225 Battery Holder

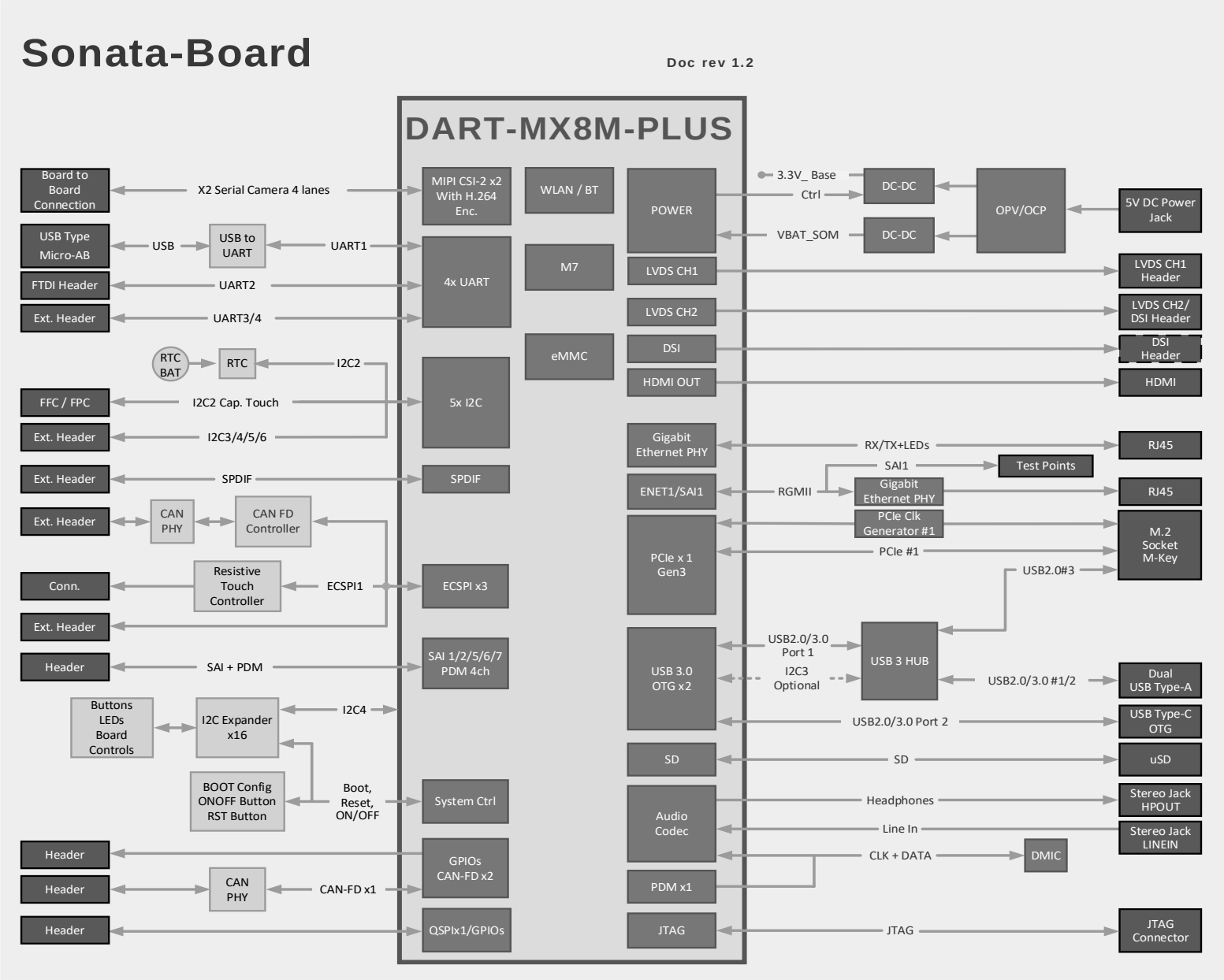
5.1 Block Diagram with DART-MX8M



5.2 Block Diagram with DART-MX8M-MINI

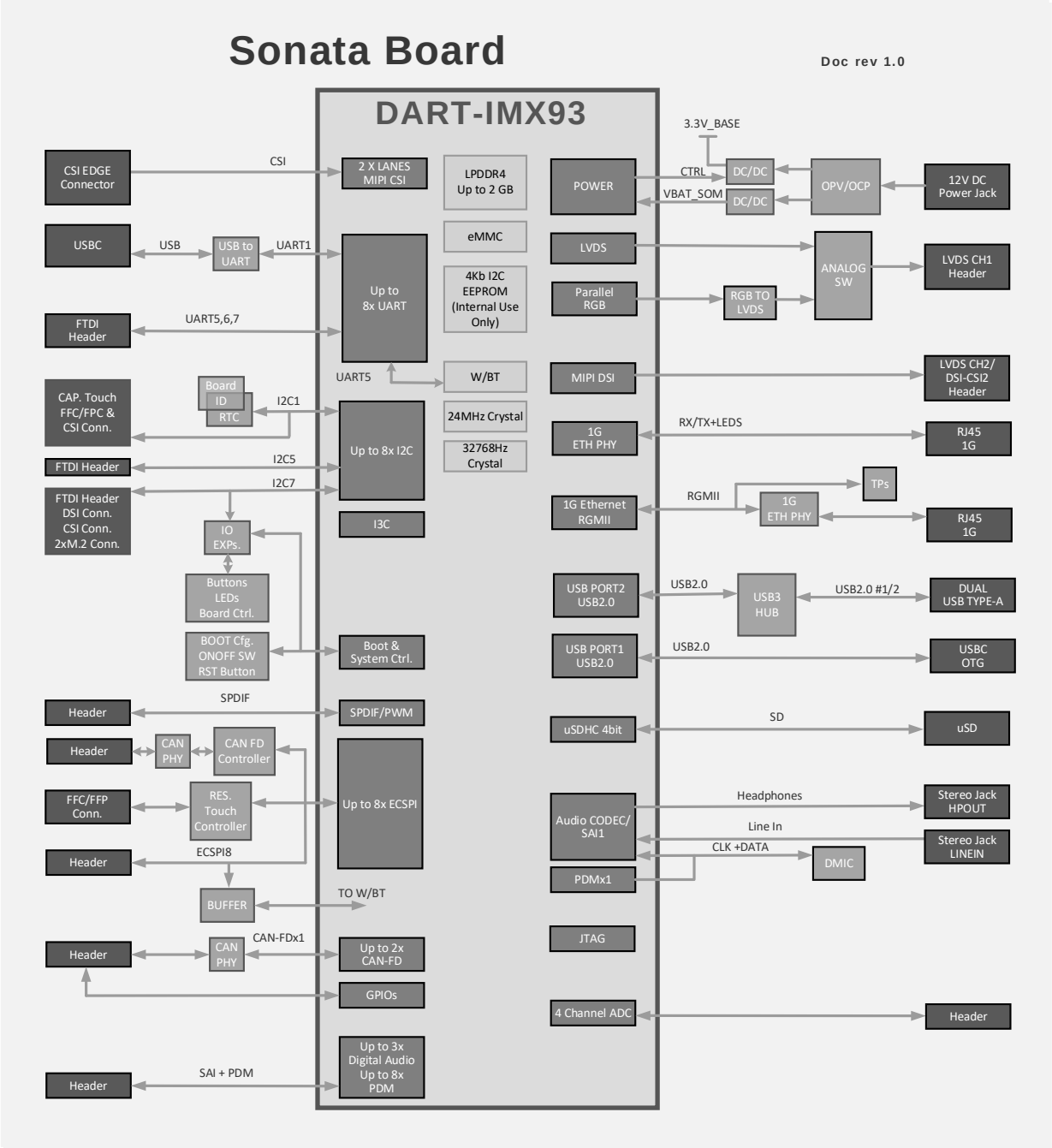


5.3 Block Diagram with DART-MX8M-PLUS

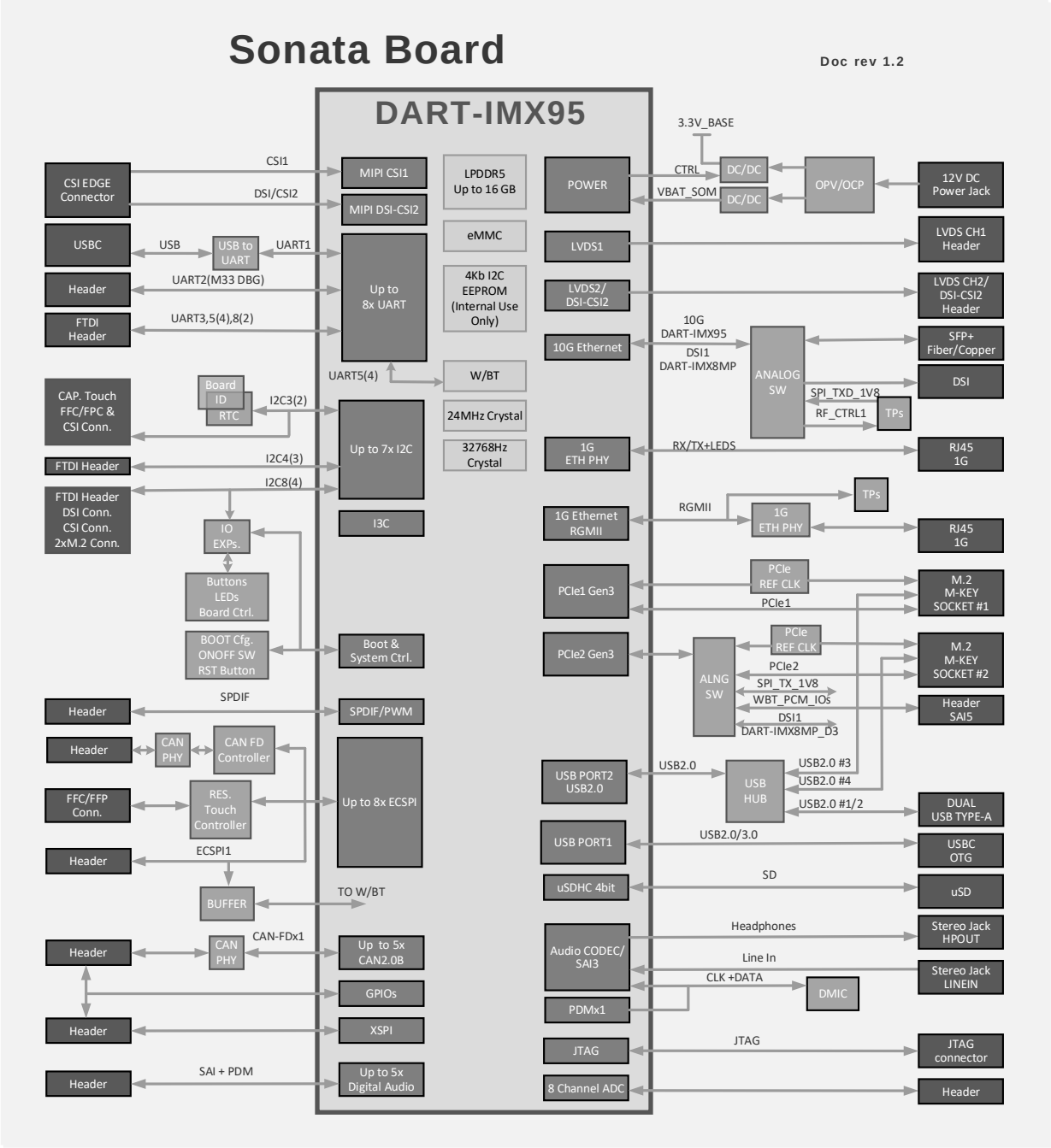


5.4 Block Diagram with DART-MX91

5.5 Block Diagram with DART-MX93

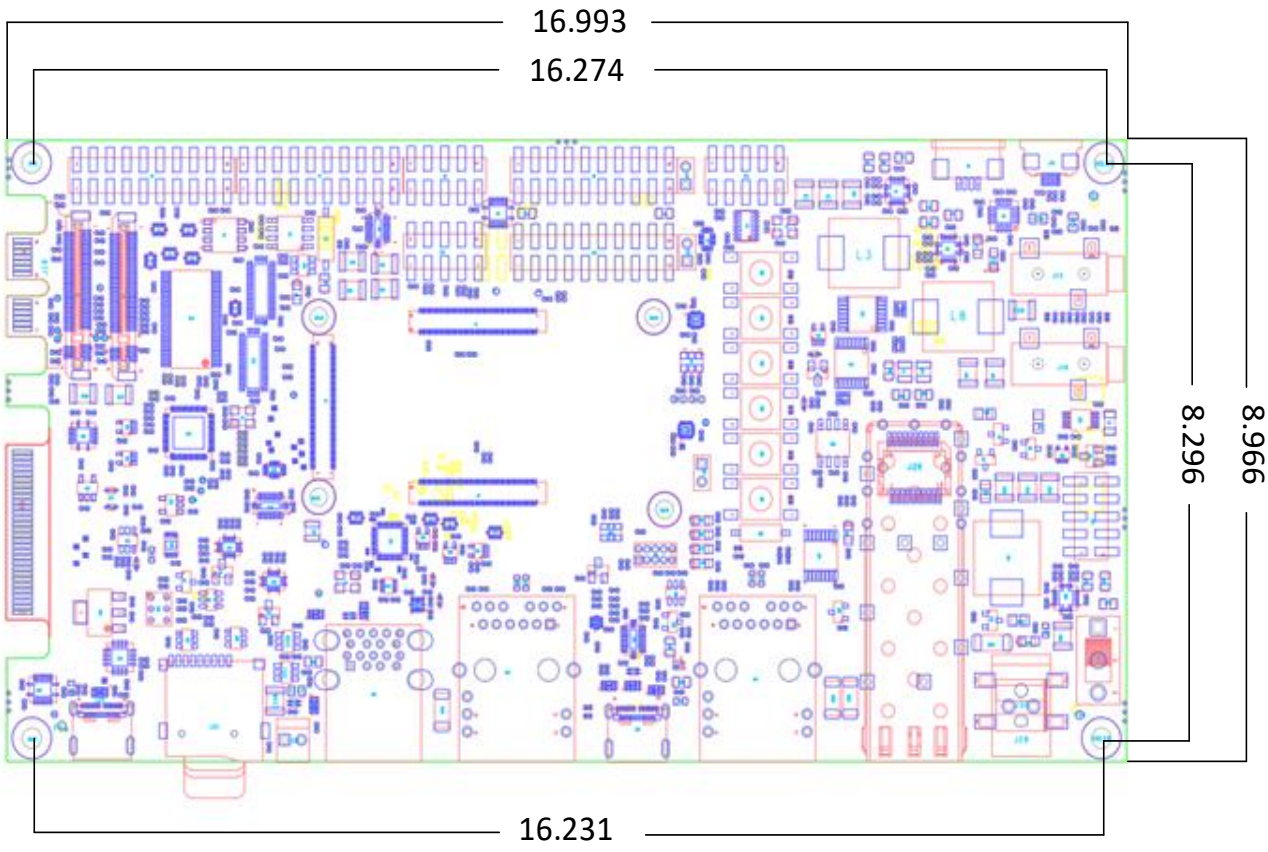


5.6 Block Diagram with DART-MX95



5.7 Board Layout

The Sonata-Board's physical dimensions are 169.9 x 89.6 mm.



Detailed CAD files are available for download at www.variscite.com.

5.8 Sonata-Board connectors

The below table lists all available connectors on Sonata-Board,
Refer to chapter 2 for a more detailed description and Pin-out of each connector.

Table 5-1 Sonata-Board connectors

Reference	Function	Type
J1	DART J1	Board to board, 90 pos., 0.4mm
J2	DART J2	Board to board, 90 pos., 0.4mm
J3	DART J3	Board to board, 90 pos., 0.4mm
J4	Capacitive Touch Panel I/F	FFC/FPC 6-pin
J5	Resistive Touch I/F	FFC/FPC 4-pin
J6	UART, I2C	Header SMT, 10x2, 2.54mm
J7	SAI2, SAI5	Header SMT, 10x2, 2.54mm
J8	GPIO, SPDIF	Header SMT, 5x2, 2.54mm
J9	LVDS#1 (Clock & Data pairs 0-2)	Header SMT, 10x2, 2.54mm
J10	ECSPI, BT/WIFI Host wake	Header SMT, 5x2, 2.54mm
J11	LVDS#1 (Data pair 3)	Header TH, 2x1, 2.54mm
J12	QSPIA	Header SMT, 5x2, 2.54mm
J13	LVDS#2 (Clock & Data pairs 0-2)	Header SMT, 5x2, 2.54mm
J14	LVDS#2 (Data pair 3)	Header TH, 2x1, 2.54mm
J15	Line In	Audio Jack 3.5 mm
J16	HDMI	HDMI Type A Rcpt. SMT, R/A
J17	PCIe#2	M.2 M-KEY, Vertical Connector
J18	PCIe#1	M.2 M-KEY, Vertical Connector
J19	Headphones	Audio Jack 3.5 mm
J20	10Gb ETH Port	SFP+ Receptacle SMT, 2x10
J21	M33 UART	Header TH, 2x1, 2.54mm
J22	SAI1	Header SMT, 5x2, 2.54mm
J23	MIPI-CSI (4 lanes x 2 Cameras)	Edge Connector mates to HSEC8-130-01-SM-DV-A
J24	JTAG	Header TH, 5x2, 1.27mm
J25	10Gb ETH Port	SFP+ Cage TH Connector
J26	10/100/1000Mbps ETH2 Port	RJ-45
J27	10/100/1000Mbps ETH1 Port	RJ-45
J28	USB 3.0 Host x2	USB 3.0 Type A Stacked
J29	Power In	2 Pin Terminal Block
J30	Power In	DC In Jack 2.0 mm
J31	SD-MMC	uSD Connector
J32	USB Debug	USB Type C
J33	USB 3.0/2.0 OTG	USB Type C
J34	FAN 5V	Header TH, 2x1, 2.54mm

J35	DSI/QSPIB	Header SMT, 10x2, 2.54mm
J36	RGB 666 LCD	FPC/FFC Connector - optional
JBT1	RTC Battery Holder	CR1225 Battery Holder - optional

6 Detailed Description

6.1 Overview

This chapter details the Sonata-Board features and external interfaces, some of which are driven directly by the following SOMs:

- DART-MX8M
- DART-MX8M-MINI
- DART-MX8M-PLUS
- DART-MX91
- DART-MX93
- DART-MX95

Please refer to the applicable DART data sheet for more information.

Table 6-1 describes this chapter table headers and acronyms used.

Table 6-1: Acronyms used on tables column header

Heading	Options	Meaning
Pin#	x	**Pin number on a connector**
Type		**Pin type & direction**
	I	INPUT
	O	OUTPUT
	DS	Differential Signal
	A	Analog
	P	Power
Signal		**Sonata-Board schematic signal name**
Description		**Short Pin functionality description**

6.2 Functionality of Sonata-Board Connectors

Various products can use the same connector pins to expose different interfaces, resulting in incompatibility or loss of intended functionality.

The reason is that not all products are compatible with the same set of interfaces.
We are making every effort to make as many interfaces available on each SOC as possible and utilize any available free pins to do so.

Please refer to the specific SOM datasheet for exact pin information.

6.3 Sonata-Board Interfaces

6.3.1 SOM

The Sonata-Board features x3 90 pin mating connectors that allows it to connect with all the pin-compatible SOMs listed above.
Please refer to the applicable SOM module data sheet for a complete signal description and pin-out on J1, J2 and J3 connectors.

6.4 Standard External Interfaces

6.4.1 USB HOST & OTG

SOMs USB capability is as follows:

- DART-MX8M & DART-MX8M-PLUS features two USB3.0/2.0 ports
- DART-MX8M-MINI, DART-MX91 & DART-MX93 features two USB2.0 ports
- DART-MX95 features one USB3.0 port and one USB2.0 port

Custom board implements the following:

- First port connected to a USB3.0/2.0 Type C OTG connector
- Second port connected to a USB3.0/2.0 four port hub which connects as follows:
    - Two hub ports connect to a USB3.0/2.0 Type A stacked Host Connector
    - Two hub ports connect to the USB2.0 interface of two M.2 PCIe connectors.

6.4.1.1 USB3.0/2.0 Type-C OTG Connector Pin-out (J33)

Table 6-2 USB Type-C OTG Connector Pin-out (J33)

Pin #	Sonata-Board Signal	Type	Description
A1	GND	P	Ground return
A2	SS_TX1_P	DSO	SuperSpeed diff. pair #1, TX, positive
A3	SS_TX1_N	DSO	SuperSpeed diff. pair #1, TX, negative
A4	USB_SS3_VBUS	P	Bus power
A5	USB_SS3_CC1	IO	Configuration channel
A6	USB_C_OTG_DP	DSIO	Non-SuperSpeed diff. pair, pos. 1, positive
A7	USB_C_OTG_DN	DSIO	Non-SuperSpeed diff. pair, pos. 1, negative
A8	SBU1	IO	Sideband use (SBU)
A9	USB_SS3_VBUS	P	Bus power
A10	SS_RX2_N	DSI	SuperSpeed diff. pair #4, RX, negative
A11	SS_RX2_P	DSI	SuperSpeed diff. pair #4, RX, positive
A12	GND	P	Digital Ground

Pin #	Sonata-Board Signal	Type	Description
B1	GND	P	Digital Ground
B2	SS_TX2_P	DSO	SuperSpeed diff. pair #3, TX, positive
B3	SS_TX2_N	DSO	SuperSpeed diff. pair #3, TX, negative
B4	USB_SS3_VBUS	P	Bus power
B5	USB_SS3_CC2	IO	Configuration channel
B6	USB_C_OTG_DP	DSIO	Non-SuperSpeed diff. pair, pos. 2, positive
B7	USB_C_OTG_DN	DSIO	Non-SuperSpeed diff. pair, pos. 2, negative
B8	SBU2	IO	Sideband use (SBU)
B9	USB_SS3_VBUS	P	Bus power
B10	SS_RX1_N	DSI	SuperSpeed diff. pair #2, RX, negative
B11	SS_RX1_P	DSI	SuperSpeed diff. pair #2, RX, positive
B12	GND	P	Digital Ground
SH1	GND	P	SHIELD pin reference
SH2	GND	P	SHIELD pin reference
SH3	GND	P	SHIELD pin reference
SH4	GND	P	SHIELD pin reference

6.4.1.2 USB3.0/2.0 HOST Connector Pin-out (J28)

Table 6-3 USB3.0/2.0 Host Connector Pin-out (J28)

Pin #	Sonata-Board Signal	Type	Description
1	USB3_PRT2_PWR	P	Port2 Bus power
2	USB2_P2_C_DN	DSIO	Port2 SuperSpeed diff. pair, negative
3	USB2_P2_C_DP	DSIO	Port2 Non-SuperSpeed diff. pair, positive
4	GND	P	Digital Ground
5	USB2_P2_R_RXN	DSI	Port2 SuperSpeed diff. pair RX, negative
6	USB2_P2_R_RXP	DSI	Port2 SuperSpeed diff. pair RX, positive
7	GND	P	Digital Ground
8	USB2_P2_C_TXN	DSO	Port2 SuperSpeed diff. pair TX, negative
9	USB2_P2_C_TXP	DSO	Port2 SuperSpeed diff. pair TX, positive
10	USB3_PRT1_PWR	P	Bus power
11	USB2_P1_C_DN	DSIO	Port1 Non-SuperSpeed diff. pair, negative
12	USB2_P1_C_DP	DSIO	Port1 Non-SuperSpeed diff. pair, positive
13	GND	P	Digital Ground
14	USB2_P1_RXN	DSI	Port1 SuperSpeed diff. pair RX, negative
15	USB2_P1_RXP	DSI	Port1 SuperSpeed diff. pair RX, positive
16	GND	P	Digital Ground
17	USB2_P1_C_TXN	DSO	Port1 SuperSpeed diff. pair TX, negative
18	USB2_P1_C_TXP	DSO	Port1 SuperSpeed diff. pair TX, positive

Pin #	Sonata-Board Signal	Type	Description
SH1	GND	P	SHIELD pin reference
SH2	GND	P	SHIELD pin reference
SH3	GND	P	SHIELD pin reference
SH4	GND	P	SHIELD pin reference

6.4.2 uSD Card

uSD Card interface is driven by SD/MMC2 interface of all SOMs.

6.4.2.1 uSD card slot Connector Pin-out (J31)

Table 6-4 uSD Card Slot Connector Pin-out (J31)

Pin #	Sonata-Board Signal	Type	Description
1	CONN_SD2_DATA2	IO	MMC Parallel Data2
2	CONN_SD2_DATA3	IO	MMC Parallel Data3
3	CONN_SD2_CMD	IO	MMC Command
4	SW_3P3_SD2	P	3.3V supply from SOM; Supply is switchable
5	CONN_SD2_CLK_R	I	MMC Clock
6	GND	P	Digital Ground
7	CONN_SD2_DATA0	IO	MMC Parallel Data0
8	CONN_SD2_DATA1	IO	MMC Parallel Data1
9	CONN_SD2_CD_B	O	MMC Card Detect
10	GND	P	SHIELD pin reference
11	GND	P	SHIELD pin reference
12	GND	P	SHIELD pin reference
13	GND	P	SHIELD pin reference

6.4.3 M.2 PCIe Slots

The Sonata-Board exports two PCIe ports through standard M.2 M-Key slots, supporting variety of M.2 cards.

6.4.3.1 M.2 PCIe Connector Pin-out (J17 & J18)

SOMs PCIe capability is as follows:

- DART-MX8M & DART-MX95 have two PCIe ports
- DART-MX8M-MINI & DART-MX8M-PLUS have one PCIe port
- DART-MX91 & DART-MX93 have none

Note:

It is important to be aware that PCIe port2 signals are multiplexed with other signals. Default interface is set to support PCIe. Mux select signal is connected to I/O Expander #3, please refer to Sonata-Board schematics. For other supported interfaces, please refer to specific SOM datasheet.

Table 6-5 PCIe1 Connector Pinout (J18)

Pin #	Sonata-Board Signal	Type	Description
1	GND	P	Digital Ground
2	BASE_PER_3V3	P	Base board 3.3V
3	GND	P	Digital Ground
4	BASE_PER_3V3	P	Base board 3.3V
5			
6			
7			
8			
9	GND	P	Digital Ground
10			
11			
12	BASE_PER_3V3	P	Base board 3.3V
13			
14	BASE_PER_3V3		Base board 3.3V
15	GND	P	Digital Ground
16	BASE_PER_3V3	P	Base board 3.3V
17			
18	BASE_PER_3V3	P	Base board 3.3V
19			

Pin #	Sonata-Board Signal	Type	Description
20			
21	GND	P	Digital Ground
22			
23			
24			
25			
26			
27	GND	P	Digital Ground
28			
29			
30			
31			
32			
33	GND	P	Digital Ground
34	USB_mPCIE1_DP	DSIO	USB2.0 Diff. Positive; USB Hub port 3 or 4
35			
36	USB_mPCIE1_DM	DSIO	USB2.0 Diff. Negative; USB Hub port 3 or 4
37			
38	PCIE1_DEVSLP#	I	Device Sleep. Connected to Test Point
39	GND	P	Digital Ground
40	I2C4_SCL_1V8	I	I2C #4 Clock, 1V8 I/O
41	PCIE1_RXN	DSO	PCIe Transmit Lane Diff. Negative
42	I2C4_SDA_1V8	IO	I2C #4 Data, 1V8 I/O
43	PCIE1_RXP	DSO	PCIe Transmit Lane Diff. Positive
44			
45	GND	P	Digital Ground
46			
47	PCIE1_TXN	DSI	PCIe Receive Lane Diff. Negative
48			
49	PCIE1_TXP	DSI	PCIe Receive Lane Diff. Positive
50	EXP_mPCIe1_RST_B	I	PCIe Port n Reset signal. From GPIO Expander #2
51	GND	P	Digital Ground
52	PCIE1_CLKREQ_B	O	M.2 Clock request. Connected to PCIe reference clock generator.
53	PCIE1_REFCLK100M_N	DSI	PCIe Clock Diff. Negative; 100MHz HCSL
54	PCIE1_WAKE_B	O	PCIe wake. Connected to Test Point
55	PCIE1_REFCLK100M_P	DSI	PCIe Clock Diff. Positive; 100MHz HCSL
56			
57	GND	P	Digital Ground

Pin #	Sonata-Board Signal	Type	Description
58			
59-66 M-Key			
67			
68	PCIE1_32K	I	32.768 kHz clock supply input. Connected to Test Point
69	PCIE1_PEDET	I	
70	BASE_PER_3V3	P	Base board 3.3V
71	GND	P	Digital Ground
72	BASE_PER_3V3	P	Base board 3.3V
73	GND	P	Digital Ground
74	BASE_PER_3V3	P	Base board 3.3V
75	GND	P	Digital Ground
S1	GND	P	Digital Ground
S2	GND	P	Digital Ground

Table 6-6 PCIe2 Connector Pinout (J19)

Pin #	Sonata-Board Signal	Type	Description
1	GND	P	Digital Ground
2	BASE_PER_3V3	P	Base board 3.3V
3	GND	P	Digital Ground
4	BASE_PER_3V3	P	Base board 3.3V
5			
6			
7			
8			
9	GND	P	Digital Ground
10			
11			
12	BASE_PER_3V3	P	Base board 3.3V
13			
14	BASE_PER_3V3		Base board 3.3V
15	GND	P	Digital Ground
16	BASE_PER_3V3	P	Base board 3.3V
17			
18	BASE_PER_3V3	P	Base board 3.3V
19			
20			
21	GND	P	Digital Ground
22			

Pin #	Sonata-Board Signal	Type	Description
23			
24			
25			
26			
27	GND	P	Digital Ground
28			
29			
30			
31			
32			
33	GND	P	Digital Ground
34	USB_mPCIE2_DP	DSIO	USB2.0 Diff. Positive; USB Hub port 3 or 4
35			
36	USB_mPCIE2_DM	DSIO	USB2.0 Diff. Negative; USB Hub port 3 or 4
37			
38	PCIE2_DEVSLP#	I	Device Sleep. Connected to Test Point
39	GND	P	Digital Ground
40	I2C4_SCL_1V8	I	I2C #4 Clock, 1V8 I/O
41	PCIE2_SW_RXN	DSO	PCIe Transmit Lane Diff. Negative
42	I2C4_SDA_1V8	IO	I2C #4 Data, 1V8 I/O
43	PCIE2_SW_RXP	DSO	PCIe Transmit Lane Diff. Positive
44			
45	GND	P	Digital Ground
46			
47	PCIE2_SW_TXN	DSI	PCIe Receive Lane Diff. Negative
48			
49	PCIE2_SW_TXN	DSI	PCIe Receive Lane Diff. Positive
50	EXP_mPCIe2_RST_B	I	PCIe Port n Reset signal. From GPIO Expander #2
51	GND	P	Digital Ground
52	PCIE2_CLKREQ_B	O	M.2 Clock request. Connected to PCIe reference clock generator.
53	PCIE2_REFCLK100M_N	DSI	PCIe Clock Diff. Negative; 100MHz HCSL
54	PCIE2_WAKE_B	O	PCIe wake. Connected to Test Point
55	PCIE2_REFCLK100M_P	DSI	PCIe Clock Diff. Positive; 100MHz HCSL
56			
57	GND	P	Digital Ground
58			
59-66 M-Key			
67			

Pin #	Sonata-Board Signal	Type	Description
68	PCIE2_32K	I	32.768 kHz clock supply input. Connected to Test Point
69	PCIE2_PEDET	I	
70	BASE_PER_3V3	P	Base board 3.3V
71	GND	P	Digital Ground
72	BASE_PER_3V3	P	Base board 3.3V
73	GND	P	Digital Ground
74	BASE_PER_3V3	P	Base board 3.3V
75	GND	P	Digital Ground
S1	GND	P	Digital Ground
S2	GND	P	Digital Ground

6.4.4 Ethernet

The Sonata-Board supports 3 different Ethernet interfaces as follows:

1. 1Gb Ethernet. SOMs' internal Gigabit Ethernet PHY is routed to a standard RJ45 Ethernet jack connector (J27) with integrated magnetics.

2. 1Gb Ethernet. The Sonata-Board's external Gigabit Ethernet PHY is routed to 2nd RJ45 Ethernet jack connector (J26) with integrated magnetics. Supported SOMs:

   - DART-MX8M-PLUS
   - DART-MX91
   - DART-MX93
   - DART-MX95

Note:

Instead of the 2nd *1Gb Ethernet port,* DART-MX8M & DART-MX8M-MINI *support SAI1 interface. Thus, these signals are routed to Test Points for optional use. See also Audio section.*

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3. 10Gb Ethernet. DART-MX95 10Gb signals are routed to a standard SFP+ connector (J20 & J25). It can be connected to fiber or copper SFP+ module.

Note:

It is important to be aware that 10Gb signals are multiplexed with MIPI-DSI signals on other SOMs. Default interface is set to support MIPI-DSI. Mux select signal is connected to I/O Expander #3, please refer to Sonata-Board schematics and to a specific SOM datasheet.

6.4.4.1 10/100/1000BaseT RJ45 Connector Pin-out (J27) – Internal PHY

Table 6-7 10/100/100BaseT Internal PHY RJ45 Connector Pin-out (J27)

Pin #	Sonata-Board Signal	Type	Description
L1	LED_ACT	O	Activity LED Anode;
L2	GND	P	Digital Ground
L4	LED_LINK10_100	IO	Link 10/100 LED Anode;
			Link 1000 LED Cathode;
L5	LED_LINK1000	IO	Link 1000 LED Anode;
			Link 10/100 LED Cathode;
R1	TCT3	O	Primary transformer common pin
R2	ETH_TRX2_N	DSIO	Bi-directional diff. pair C negative
R3	ETH_TRX2_P	DSIO	Bi-directional diff. pair C positive
R4	ETH_TRX1_P	DSIO	Bi-directional diff. pair B positive
R5	ETH_TRX1_N	DSIO	Bi-directional diff. pair B negative
R6	TCT2	O	Primary transformer common pin
R7	TCT4	O	Primary transformer common pin
R8	ETH_TRX3_P	DSIO	Bi-directional diff. pair D positive
R9	ETH_TRX3_N	DSIO	Bi-directional diff. pair D negative
R10	ETH_TRX0_N	DSIO	Bi-directional diff. pair A negative
R11	ETH_TRX0_P	DSIO	Bi-directional diff. pair A positive
R12	TCT1	O	Primary transformer common pin
SH1	GND_EARTH	P	EARTH
SH2	GND_EARTH	P	EARTH

Note:

For detailed LED behavior see LED status table in SOM data sheet.

6.4.4.2 10/100/1000BaseT RJ45 Connector Pin-out (J26) – External PHY

Table 6-8 10/100/1000BaseT External PHY RJ45 Connector Pin-out (J26)

Pin #	Sonata-Board Signal	Type	Description
L1	ETH1_LED_ACT	O	Activity LED Anode;
L2	GND	P	Digital Ground
L4	GND	P	Digital Ground
L5	ETH1_LED_LINK	IO	Link 1000 LED Anode;
R1	TCT3	O	Primary transformer common pin
R2	ETH1_MDI_C_N	DSIO	Bi-directional diff. pair C negative
R3	ETH1_MDI_C_P	DSIO	Bi-directional diff. pair C positive

R4	ETH1_MDI_B_P	DSIO	Bi-directional diff. pair B positive
R5	ETH1_MDI_B_N	DSIO	Bi-directional diff. pair B negative
R6	TCT2	O	Primary transformer common pin
R7	TCT4	O	Primary transformer common pin
R8	ETH1_MDI_D_P	DSIO	Bi-directional diff. pair D positive
R9	ETH1_MDI_D_N	DSIO	Bi-directional diff. pair D negative
R10	ETH1_MDI_A_N	DSIO	Bi-directional diff. pair A negative
R11	ETH1_MDI_A_P	DSIO	Bi-directional diff. pair A positive
R12	TCT1	O	Primary transformer common pin
SH1	GND_EARTH	P	EARTH
SH2	GND_EARTH	P	EARTH

Table 6-9 Ethernet PHY LED Behavior

STATUS / LED	10M Link	10M Active	100M Link	100M Active	1000M Link	1000M Active
LED_LINK	ON	ON	ON	ON	ON	ON
ETH1_LED0	ON	BLINK	ON	BLINK	ON	BLINK

6.4.4.3 10Gb Ethernet SFP+ connector Pin-out (J25)

Table 6-10 10Gb Ethernet SFP+ connector Pin-out (J25)

Pin #	Sonata-Board Signal	Type	Description
1	VEET	P	Transmitter Ground
2	TX_FLT	O	Transmit fault. Active low open drain
3	TX_DIS	I	Transmit disable. Active high
4	I2C2_SDA	IO	I2C #2 data. Interface module internal EEPROM
5	I2C2_SCL	I	I2C #2 clock. Interface module internal EEPROM
6	MOD_PRSNT#	O	Indicating module plugged in. Connected to LED (D21)
7	RS0	I	Connected to GND
8	SFP_RX_LOS	O	LOS of receive signal. Active low open drain
9	RS1	I	Connected to GND
10	VEER	P	Receiver Ground
11	VEER	P	Receiver Ground
12	DT95_ETH10G_TX0_P	DSI	Differential transmitter input, positive
13	DT95_ETH10G_TX0_N	DSI	Differential transmitter input, negative
14	VEER	P	Receiver Ground

15	VCCR	P	Receiver power
16	VCCT	P	Transmitter power
17	VEET	P	Transmitter Ground
18	DT95_ETH10G_RX0_P	DSO	Differential receiver input, positive
19	DT95_ETH10G_RX0_N	DSO	Differential receiver input, negative
20	VEET	P	Transmitter Ground

6.4.5 AUDIO

The Sonata-Board features two 3.5mm jacks for analog audio interfaces.

- Headphone (J19)
- Line in (J15)

The analog audio I/F signals are driven by the SOMs Audio Codec. Please refer to the applicable SOM module data sheet for complete audio codec information.

Also, a digital microphone is implemented on the Sonata-Board, see schematics for U42.

6.4.5.1 Line In Jack Connector Pin-out (J15)

Table 6-11 Line in Jack Connector Pin-out (J15)

Pin #	Sonata-Board Signal	Type	Description
1	AGND	AP	Analog ground return for audio.
2	LLINEIN_C	AI	Line-in Left input
3	RLINEIN_C	AI	Line-in Right input

6.4.5.2 Headphone jack Connector Pin-out (J19)

Table 6-12 Headphone out Jack Connector Pin-out (J19)

Pin #	Sonata-Board Signal	Type	Description
1	AGND	AP	Analog ground return for audio.
2	HPLOUT_C	AO	Headphone out Left
3	HPROUT_C	AO	Headphone out Right

6.4.6 Serial Camera

The Sonata-Board supports two MIPI CSI camera sensor inputs using an extension camera board connected to an edge connector (J23). Extension board for utilizing this interface can be purchased on Variscite's website.

The Camera Board Mating connector: SAMTEC 60POS 0.8mm pitch, **HSEC8-130-01-SM-DV-A**

SOMs MIPI CSI capability is as follows:

- DART-MX8M, DART-MX8M-PLUS & DART-MX95 support 2x 4 lanes MIPI CSI
- DART-MX8M-MINI supports 1x 4 lanes MIP CSI
- DART-MX93 supports 1x 2 lanes MIPI CSI
- DART-MX91 supports none

Note:

It is important to be aware that on System on Modules (SOMs) that do not have support for the MIPI CSI camera interfaces, this connector may be used for other interfaces. For specific pin information, refer to the SOM datasheets.

6.4.6.1 Serial Camera Connector Pin-out (J23)

Table 6-13 Serial Camera Connector Pin-out (J23)

Pin #	Sonata-Board Signal	Type	Description
1	BASE_PER_3V3	P	Base board 3.3V
2	GND	P	Digital Ground
3	BASE_PER_3V3	P	Base board 3.3V
4	I2C4_SDA_1V8	IO	I2C #4 Data
5	BASE_PER_1V8	P	Base board 1.8V
6	I2C4_SCL_1V8	IO	I2C #4 Clock
7	BASE_PER_1V8	P	Base board 1.8V
8	GND	P	Digital Ground
9	GND	P	Digital Ground
10	EXP_CSI_P2_PWREN_1V8	O	Power down control; Active Low; GPIO Expander #1 port 2
11	CSI_P1_DP0	DSI	CSI Port1 Lane0; Positive
12	EXP_CSI_P2_RST_B_1V8	O	Reset control; Active Low; GPIO Expander #1 port 0
13	CSI_P1_DN0	DSI	CSI Port1 Lane0; Negative
14	CSI_P2_OPT_1V8	O	Optional discrete
15	GND	P	Digital Ground

Pin #	Sonata-Board Signal	Type	Description
16	CSI_P2_SYNC_1V8	O	Sync signal
17	CSI_P1_CKP	DSI	CSI Port1 Clock; Positive
18	GND	P	Digital Ground
19	CSI_P1_CKN	DSI	CSI Port1 Clock; Negative
20	CSI_P2_TRIG_1V8	I	Trigger
21	GND	P	Digital Ground
22	GND	P	Digital Ground
23	CSI_P1_DP1	DSI	CSI Port1 Lane1; Positive
24	CSI_P2_DN3	DSI	CSI Port2 Lane3; Negative
25	CSI_P1_DN1	DSI	CSI Port1 Lane1; Negative
26	CSI_P2_DP3	DSI	CSI Port2 Lane3; Positive
27	GND	P	Digital Ground
28	GND	P	Digital Ground
29	CSI_P1_DP2	DSI	CSI Port1 Lane2; Positive
30	CSI_P2_DN2	DSI	CSI Port2 Lane2; Negative
31	CSI_P1_DN2	DSI	CSI Port1 Lane2; Negative
32	CSI_P2_DP2	DSI	CSI Port2 Lane2; Positive
33	GND	P	Digital Ground
34	GND	P	Digital Ground
35	CSI_P1_DP3	DSI	CSI Port1 Lane3; Positive
36	CSI_P2_DN1	DSI	CSI Port2 Lane1; Negative
37	CSI_P1_DN3	DSI	CSI Port1 Lane3; Negative
38	CSI_P2_DP1	DSI	CSI Port2 Lane1; Positive
39	GND	P	Digital Ground
40	GND	P	Digital Ground
41	CSI_P1_TRIG_1V8	I	Trigger
42	CSI_P2_CKN	DSI	CSI Port2 Clock; Negative
43	GND	P	Digital Ground
44	CSI_P2_CKP	DSI	CSI Port2 Clock; Positive
45	CSI_P1_SYNC_1V8	O	Sync signal
46	GND	P	Digital Ground
47	CSI_P1_OPT_1V8	O	Optional discrete
48	CSI_P2_DN0	DSI	CSI Port2 Lane0; Negative
49	EXP_CSI_P1_RST_B_1V8	O	Reset control; Active Low; GPIO Expander #1 port 1
50	CSI_P2_DP0	DSI	CSI Port2 Lane0; Positive
51	EXP_CSI_P1_PWREN_1V8	O	Power down control; Active Low; GPIO Expander #1 port 3
52	GND	P	Digital Ground
53	GND	P	Digital Ground
54	BASE_PER_1V8	P	Base board 1.8V

Pin #	Sonata-Board Signal	Type	Description
55	I2C2_SCL_1V8	IO	I2C #2 Clock
56	BASE_PER_1V8	P	Base board 1.8V
57	I2C2_SDA_1V8	IO	I2C #2 Data
58	BASE_PER_3V3	P	Base board 3.3V
59	GND	P	Digital Ground
60	BASE_PER_3V3	P	Base board 3.3V

Note

Camera control (reset, power down, sync, trigger, optional) and I2C interfaces runs at 1.8V levels.

6.4.7 Display

The Sonata-Board supports 4 different display interfaces as follows:

1. LVDS
2. MIPI-DSI
3. HDMI
4. Parallel RGB to LVDS
5. RGB 666 LCD, Sonata-Board Rev1.1 only

Note:

Sonata-Board doesn't support eDP interface.

6.4.7.1 LVDS

SOMs LVDS capability is as follows:

- Dual-Link LVDS interface supported by these SOMs
    - DART-MX8M
    - DART-MX8M-MINI
    - DART-MX8M-PLUSE
    - DART-MX95
- Single-Link LVDS interface supported by DART-MX93
- DART-MX91 supports none

Note:

Please note that:

DART-MX8M & DART-MX8M-MINI expose Dual-Link LVDS interface via MIPI-DSI to FlatLink™ bridge assembled on the SOM.

DART-MX8M-PLUSE, DART-MX93 & DART-MX95 LVDS interfaces are directly connected to the SOC.

LVDS#1 interface is muxed with Parallel RGB to LVDS bridge (DART-MX91 &DART-MX93). Mux select signal is connected to I/O Expander #3 (default is set to support LVDS).

For more information, please refer to Sonata-Board schematics and to a specific SOM datasheet.

The interface is exposed using two Variscite's standard 20 pin Headers (J9, J13). Fourth data bit of each interface is extended using additional 2 pin connectors (J11, J14)

J9 is used for connecting Variscite's standard 7" LVDS LCD screen.

6.4.7.2 LVDS#1 Connector Pin-out (J9)

Table 6-14 LVDS Channel 0 Connector Pin-out (J9)

Pin #	Sonata-Board Signal	Type	Description
1	BASE_PER_3V3	P	Base power 3.3V
2	BASE_PER_3V3	P	Base power 3.3V
3	GND	P	Digital Ground
4	GND	P	Digital Ground
5	LVDS1_CON_TX0_N	DSO	LVDS Data0 Diff. Negative
6	LVDS1_CON_TX0_P	DSO	LVDS Data0 Diff. Positive
7	GND	P	Digital Ground
8	LVDS1_CON_TX1_N	DSO	LVDS Data1 Diff. Negative
9	LVDS1_CON_TX1_P	DSO	LVDS Data1 Diff. Positive
10	GND	P	Digital Ground
11	LVDS1_CON_TX2_N	DSO	LVDS Data2 Diff. Negative
12	LVDS1_CON_TX2_P	DSO	LVDS Data2 Diff. Positive
13	GND	P	Digital Ground
14	LVDS1_CON_CLK_N	DSO	LVDS Clock Diff. Negative
15	LVDS1_CON_CLK_P	DSO	LVDS Clock Diff. Positive
16	GND	P	Digital Ground
17	VCC_5V	P	Backlight LED 5V power
18	VCC_5V	P	Backlight LED 5V power
19	GPIO1_IO01(PWM1_OUT)	IO	Backlight Brightness Control; GPIO1_IO01
20	GND	P	Digital Ground

6.4.7.3 LVDS#1 Data3 Extension Connector Pin-out (J11)

Table 6-15 LVDS Channel 0 Data3 Connector Pin-out (J11)

Pin #	Sonata-Board Signal	Type	Description
1	LVDS1_TX3_CM_P	DSO	LVDS Data3 Diff. Positive
2	LVDS1_TX3_CM_N	DSO	LVDS Data3 Diff. Negative

6.4.7.4 LVDS#2 Connector Pin-out (J13)

Table 6-16 LVDS Channel 1 Connector Pin-out (J13)

Pin #	Sonata-Board Signal	Type	Description
1	BASE_PER_3V3	P	Base power 3.3V
2	BASE_PER_3V3	P	Base power 3.3V

Pin #	Sonata-Board Signal	Type	Description
3	GND	P	Digital Ground
4	GND	P	Digital Ground
5	LVDS2_DSI_TX0_CM_N	DSO	LVDS Data0 Diff. Negative
6	LVDS2_DSI_TX0_CM_P	DSO	LVDS Data0 Diff. Positive
7	GND	P	Digital Ground
8	LVDS2_DSI_TX1_CM_N	DSO	LVDS Data1 Diff. Negative
9	LVDS2_DSI_TX1_CM_P	DSO	LVDS Data1 Diff. Positive
10	GND	P	Digital Ground
11	LVDS2_TX2_DSI_CLK_CM_N	DSO	LVDS Data2 Diff. Negative
12	LVDS2_TX2_DSI_CLK_CM_P	DSO	LVDS Data2 Diff. Positive
13	GND	P	Digital Ground
14	LVDS2_CLK_DSI_TX2_CM_N	DSO	LVDS Clock Diff. Negative
15	LVDS2_CLK_DSI_TX2_CM_P	DSO	LVDS Clock Diff. Positive
16	GND	P	Digital Ground
17	VCC_5V	P	Backlight LED 5V power
18	VCC_5V	P	Backlight LED 5V power
19	GPIO1_IO01(PWM1_OUT)	IO	Backlight Brightness Control; GPIO1_IO01
20	GND	P	Digital Ground

6.4.7.5 LVDS#2 Data3 Extension Connector Pin-out (J14)

Table 6-17 LVDS Channel 2 Data3 Connector Pin-out (J14)

Pin #	Sonata-Board Signal	Type	Description
1	LVDS2_DSI_TX3_CM_P	DSO	LVDS Data3 Diff. Positive
2	LVDS2_DSI_TX3_CM_N	DSO	LVDS Data3 Diff. Negative

Note:

Please note that some SOMs assemblies expose native 4 lanes MIPI-DSI instead of LVDS#2 interface. Please refer to the next section for further details

6.4.7.6 MIPI-DSI

SOMs MIPI-DSI capability is as follows:

- DART-MX8M & DART-MX8MM ***without*** ***"LD"*** assembly option, expose it to J13, J14 (instead of LVDS#2)
- DART-MX8M-PLUSE:
  - ***With*** "**DSCM"** assembly option, expose it to J13, J14 (instead of LVDS#2)
  - ***Without*** **"DSCM**" assembly option, expose it to J35
- DART-MX93 has only single LVDS interface, thus MIPI-DSI is exposed to J13, J14.

- DART-MX95
  - ***With*** **"DSCM"** assembly option, expose it to J13, J14 (instead of LVDS#2)
  - ***Without*** **"DSCM"** assembly option, MIPI-DSI is exposed to J23 (MIP-CSI connector)
- DART-MX91 doesn't support MIPI-DSI

6.4.7.7 MIPI-DSI Pin-out for DART-MX8M-PLUSE (J35)

Table 6-18 MIPI-DSI Pin-out connector for DART-MX8M-PLUSE (J35)

Pin #	Sonata-Board Signal	Type	Description
1	I2C4_SDA_SW	IO	I2C #4 Data
2	I2C4_SCL_SW	IO	I2C #4 Clock
3	BASE_PER_3V3	P	Base power 3.3V
4	BASE_PER_3V3	P	Base power 3.3V
5	GND	P	Digital Ground
6	GND	P	Digital Ground
7	DT8MP-DSI1_D0_N	DSO	DSI Data0 Diff. Negative
8	DT8MP-DSI1_D0_P	DSO	DSI Data0 Diff. Positive
9	GND	P	Digital Ground
10	DT8MP-DSI1_D1_N	DSO	DSI Data1 Diff. Negative
11	DT8MP-DSI1_D1_P	DSO	DSI Data1 Diff. Positive
12	GND	P	Digital Ground
13	DT8MP-DSI1_D2_N	DSO	DSI Data2 Diff. Negative
14	DT8MP-DSI1_D2_P	DSO	DSI Data2 Diff. Positive
15	GND	P	Digital Ground
16	DT8MP-DSI1_CLK_N	DSO	DSI Clock Diff. Negative
17	DT8MP-DSI1_CLK_P	DSO	DSI Clock Diff. Positive
18	GND	P	Digital Ground
19	VCC_5V	P	Backlight LED 5V power
20	VCC_5V	P	Backlight LED 5V power
21	PWM1_OUT	O	Backlight Brightness Control
22	GND	P	Digital Ground
23	DT8MP-DSI1_D3_N	DSO	DSI Data3 Diff. Negative
24	DT8MP-DSI1_D3_P	DSO	DSI Data3 Diff. Positive

Note:

Please note that:

DART-MX8M-PLUS DSI interface is MUX with DART-MX95 10Gb Ethernet interface. Default is set to support DART-MX8M-PLUS DSI interface. Mux select signal is connected to IO Expander #3.

J35 is located on the PS side and is unassembled.

For more information, please refer to Sonata-Board schematics and to a specific SOM datasheet.

6.4.7.8 HDMI

SOMs HDMI capability is as follows:

- DART-MX8M & DART-MX8M-PLUS support HDMI 2.0
- All the other SOMs don't support HDMI interface.

HDMI interface is routed through an edge connector - J16. Extension boards for utilizing this interface can be purchased on Variscite's website.

The HDMI extension board Mating connector: SAMTEC 26POS 0.8mm pitch, HSEC8-113-01-L-RA.

HDMI path coupling and level termination:

MX8M, according to NXP, requires AC coupling and level termination on HDMI path.
On the other hand, MX8MP, requires DC coupling with no level termination.
Sonata-Board supports MX8MP requirements only.
This option has been tested on the DART-MX8M with resolution up to 4K.
Testing was done with limited number of monitors and was found to be functioning properly.
Despite that, Variscite recommends using the dedicated lane coupling and termination per NXP requirements.

Refer to the DART-MX8M & DART-MX8M-PLUS data sheets and NXP references for detailed description of these interfaces and HDMI level termination.

6.4.7.9 HDMI Connector Pin-out (J16)

Table 6-19 HDMI Connector Pin-out (J16)

Pin #	Sonata-Board Signal	Type	Description
1			
2	BASE_PER_3V3	P	Base Board 3.3V
3			
4	BASE_PER_3V3	P	Base board 3.3V
5			
6	VCC_5V	P	Base board 5V
7	HDMI_CN_Utility/HEAC+_R	DSI	HDMI Ethernet and ARC. Positive
8	HDMI_CN_SCL	O	I2C Clock for HDMI DDC
9	HDMI_CN_HPD/HEAC-	AI/DSI	HDMI Hot Plug Detect/ HDMI Ethernet and ARC. Negative
10	HDMI_CN_SDA	IO	Data for HDMI DDC
11	HDMI_CN_CEC	IO	HDMI Consumer Electronics Control; 1 Wire Serial; Bidirectional
12	HDMI_DP_SEL	I	See Pin 7,8 description
13	GND	P	Digital Ground
14	GND	P	Digital Ground

Pin #	Sonata-Board Signal	Type	Description
15	HDMI_CN_CLK_P	DSO	HDMI TMDS Diff. Clock; Positive
16	HDMI_CN_D0_P	DSO	HDMI TMDS Diff. Data 0; Positive
17	HDMI_CN_CLK_N	DSO	HDMI TMDS Diff. Clock; Negative
18	HDMI_CN_D0_N	DSO	HDMI TMDS Diff. Data 0; Negative
19	GND	P	Digital Ground
20	GND	P	Digital Ground
21	HDMI_CN_D2_P	DSO	HDMI TMDS Diff. Data 2; Positive
22	HDMI_CN_D1_P	DSO	HDMI TMDS Diff. Data 1; Positive
23	HDMI_CN_D2_N	DSO	HDMI TMDS Diff. Data 2; Negative
24	HDMI_CN_D1_N	DSO	HDMI TMDS Diff. Data 1; Negative
25	GND	P	Digital Ground
26	GND	P	Digital Ground

6.4.7.10 Parallel RGB to LVDS

SOMs parallel RGB capability is as follows:

- DART-MX91 supports parallel RGB
- All the other SOMs don't support this interface.

RGB interface is routed to *FlatLink™ Transmitter,* LVDS serializer, that converts it to LVDS interface. This interface is muxed to LVDS#1 interface. Mux select signal is connected to I/O Expander #3 (default is set to support LVDS).
For more information, please refer to Sonata-Board schematics and to specific SOM datasheet.

6.4.7.11 RGB 666 LCD Connector (J36) – optional

SOMs RGB 666 LCD capability is as follows:

- DART-MX91 & DART-MX93 support RGB 666 LCD
- All the other SOMs don't support this interface.

Table 6-20 RGB 666 LCD connector

DART Pin#	RGB Signals	Type	Description
J36.1	GND	P	Digital GND
J36.2	GND	P	Digital GND
J36.3	PWM1_OUT	O	Backlight Brightness Control
J36.4	VCC_5V	P	5V supply for backlight LEDs
J36.5	VCC_5V	P	5V supply for backlight LEDs
J36.6	VCC_5V	P	5V supply for backlight LEDs

DART Pin#	RGB Signals	Type	Description
J36.7	BASE_PER_3V3	P	Base board 3.3V
J36.8	BASE_PER_3V3	P	Base board 3.3V
J36.9	RGB_DE	O	Data enable
J36.10	GND	P	Digital GND
J36.11	GND	P	Digital GND
J36.12	GND	P	Digital GND
J36.13	RGB_DATA7	O	Data bit
J36.14	RGB_DATA6	O	Data bit
J36.15	RGB_DATA5	O	Data bit
J36.16	GND	P	Digital GND
J36.17	RGB_DATA4	O	Data bit
J36.18	RGB_DATA3	O	Data bit
J36.19	RGB_DATA2	O	Data bit
J36.20	GND	P	Digital GND
J36.21	RGB_DATA15	O	Data bit
J36.22	RGB_DATA14	O	
J36.23	RGB_DATA13	O	Data bit
J36.24	GND	P	Digital GND
J36.25	RGB_DATA12	O	Data bit
J36.26	RGB_DARA11	O	Data bit
J36.27	RGB_DATA10	O	Data bit
J36.28	GND	P	Digital GND
J36.29	RGB_DATA23	O	Data bit
J36.30	RGB_DATA22	O	Data bit
J36.31	RGB_DATA21	O	Data bit
J36.32	GND	P	Digital GND
J36.33	RGB_DATA20	O	Data bit
J36.34	RGB_DATA19	O	Data bit
J36.35	RGB_DATA18	O	Data bit
J36.36	GND	P	Digital GND
J36.37	GND	P	Digital GND
J36.38	PCLK	O	Pixel clock
J36.39	GND	P	Digital GND
J36.40	GND	P	Digital GND

Note:

It is important to be aware that on SOMs that do not support the above interface, these signals are used for other interfaces. For more information, refer to specific SOM datasheet.

6.4.8 DSI/QSPIB Connector Pin-out (J35)

J35 connector function is as follows:

- DART-MX8M exports the QSPIB interface or other alternate functions available
- DART-MX8M-PLUS exports MIPI-DSI lanes when hardware configuration is ***without*** "DSCM"
- DART-MX8M-MINI exports GPIOs
- All other SOMs don't use this connector

Table 6-21 QSPIB Connector Pin-out (J35)

Pin #	SOM Signal	Type	Description
1	I2C4_SDA	IO	I2C #4 Data
2	I2C4_SCL	O	I2C #4 Clock
3	BASE_PER_3V3	P	Base power 3.3V
4	BASE_PER_3V3	P	Base power 3.3V
5	GND	P	Digital Ground
6	GND	P	Digital Ground
7	NAND_DATA04 DT8MP-DSI1_D0_N	IO DSO	DART-MX8M - QSPI B Data 0 DART-MX8M-PLUS - DSI Data0 Diff. Negative
8	NAND_RE_B GPIO1_IO07 DT8MP-DSI1_D0_P	IO IO DSO	DART-MX8M - QSPI B Strobe DART-MX8M-MINI - GPIO DART-MX8M-PLUS - DSI Data0 Diff. Positive
9	GND	P	Digital Ground
10	NAND_DATA05 DT8MP-DSI1_D1_N	IO DSO	DART-MX8M - QSPI B Data 1 DART-MX8M-PLUS - DSI Data1 Diff. Negative
11	NAND_CLE CLKOUT1_1V8 DT8MP-DSI1_D1_P	IO O DSO	DART-MX8M - QSPI B Serial Clock DART-MX8M-MINI - CLKOUT1; 1.8V Level only DART-MX8M-PLUS - DSI Data1 Diff. Positive
12	GND	P	Digital Ground
13	NAND_WP_B DT8MP-DSI1_D2_N	IO DSO	DART-MX8M - GPIO3_IO18 DART-MX8M-PLUS - DSI Data2 Diff. Negative
14	NAND_WE_B DT8MP-DSI1_D2_P	IO DSO	DART-MX8M - GPIO3_IO17 DART-MX8M-PLUS - DSI Data2 Diff. Positive
15	GND	P	Digital Ground
16	NAND_DATA07 CLKIN1_1V8 DT8MP-DSI1_CLK_N	IO I DSO	DART-MX8M - QSPI B Data 3 DART-MX8M-MINI - CLKIN1 1.8V Level only DART-MX8M-PLUS - DSI Clock diff. Negative
17	NAND_DATA06 CLKIN2_1V8 DT8MP-DSI1_CLK_P	IO I DSO	DART-MX8M - QSPI B Data 2 DART-MX8M-MINI - CLKIN2; 1.8V Level only DART-MX8M-PLUS - DSI Clock Diff. Positive
18	GND	P	Digital Ground
19	VCC_5V	P	Backlight LED 5V power
20	VCC_5V	P	Backlight LED 5V power
21	GPIO1_IO01(PWM1_OUT)	IO	DART-MX8M-PLUS - Backlight Brightness Control
22	GND	P	Digital Ground
23	DT8MP-DSI1_D3_N	DSO	DART-MX8M-PLUS - DSI Data3 Diff. Negative

Pin #	SOM Signal	Type	Description
24	DT8MP-DSI1_D3_P	DSO	DART-MX8M-PLUS - DSI Data3 Diff. Positive

Note:

J35 is located on print side and not assembled.

DART-MX95 SOM uses some of these signals as Ethernet 10Gb interface. Thus, these signals are passed via mux. Mux select signal is connected to IO Expander #3; default is set to support DART-MX8M-PLUS DSI interface.

For further information refer to Sonata-Board schematics and SOMs datasheets.

6.4.9 Capacitive Touch

Sonata-Board provides a capacitive Touch interface exposed to an FFC/FPC connector for connecting to Variscite's standard 7" Capacitive touch LCD screen.

6.4.9.1 Capacitive Touch Panel Connector Pin-out (J4)

Table 6-22 Capacitive Touch Panel Connector Pin-out (J4)

Pin #	Sonata-Board Signal	Type	Description
1	EXP_CAPTOUCH_RST_B	O	Capacitive Touch Reset, Active Low GPIO Expander #2 port 4
2	I2C2_SDA	IO	I2C #2 Data
3	I2C2_SCL	O	I2C #2 Clock
4	CAP_TOUCH_INTn	IO	Capacitive Touch Interrupt; Active Low; GPIO1_IO14
5	BASE_PER_3V3	P	Base board 3.3V
6	GND	P	Digital Ground
7	GND	P	Digital Ground
8	GND	P	Digital Ground

Note:

Capacitive Touch Interrupt pin is connected differently in each SOM.

In DART-MX8M, DART-MX8M-MINI & DART-MX8M-PLUS it is connected to GPIO1_IO14.

In DART-MX93 it is connected to GPIO3_IO27.

In DART-MX95 it is connected to GPIO1_IO07.

Please refer to Sonata-Board schematics and specific SOM datasheet.

6.4.10 Resistive Touch

Sonata-Board provides a resistive interface exposed to FFC/FPC connector for connecting to a resistive touch LCD screen.

6.4.10.1 Resistive Touch Connector Pin-out (J5)

Table 6-23 Resistive Touch Connector Pin-out (J5)

Pin #	Sonata-Board Signal	Type	Description
1	TS_X-	AI	X negative side plate connection
2	TS_Y+	AI	Y positive side plate connection
3	TS_X+	AI	X positive side plate connection
4	TS_Y-	AI	Y negative side plate connection
5	GND	P	Digital Ground
6	GND	P	Digital Ground

Note:

Resistive touch controller interrupt pin is connected differently in each SOM.
In DART-MX8M-PLUS it is connected to GPIO1_IO07.
In DART-MX8M and DART-MX8M-MINI it is connected to GPIO1_IO03.
In DART-MX95 it is connected to GPIO2_IO24.
Please refer to Sonata-Board schematics and specific SOM datasheet.

6.4.11 USB - Debug

The Sonata-Board exposes the debug UART1 interface. The signals are driven by an on-board UART-to-USB Bridge and exposed to a USB-C connector.

6.4.11.1 USB Debug Connector Pin-out (J32)

Table 6-24 USB Debug Connector Pin-out (J32)

Pin #	Sonata-Board Signal	Type	Description
A1	GND	P	Ground return
A2			
A3			
A4	DEBUG_VBUS_C	P	Bus power
A5	DBG_CC1	IO	Pulled down to GND
A6	USB_DEBUG_DP	DSIO	Non-SuperSpeed diff. pair, pos. 1, positive
A7	USB_DEBUG_DN	DSIO	Non-SuperSpeed diff. pair, pos. 1, negative
A9	DEBUG_VBUS_C	P	Bus power
A10			
A11			
A12	GND	P	Digital Ground
B1	GND	P	Digital Ground
B2			
B3			
B4	DEBUG_VBUS_C	P	Bus power
B5	DBG_CC2	IO	Pulled down to GND
B6	USB_DEBUG_DP	DSIO	Non-SuperSpeed diff. pair, pos. 2, positive
B7	USB_DEBUG_DM	DSIO	Non-SuperSpeed diff. pair, pos. 2, negative
B8			
B9	DEBUG_VBUS_C	P	Bus power
B10			
B11			
B12	GND	P	Digital Ground
SH1	GND	P	SHIELD pin reference
SH2	GND	P	SHIELD pin reference
SH3	GND	P	SHIELD pin reference
SH4	GND	P	SHIELD pin reference

6.4.12 I2C & UART & ENET MDIO

The Sonata-Board exposes I2C, UART and ENET MDIO interfaces. Signals are exported to a standard 20 pin Header. Some of these interfaces are used or shared by other functions.
Please see note below this table for more details.

6.4.12.1 I2C and UART Connector Pin- out (J6)

Table 6-25 I2C, UART and ENET MDIO Connector Pin-out (J6)

Pin #	Sonata-Board Signal	Type	Description
1	BT_UART4_TX	IO	UART4 Transmit
2	FTDI_RTSN	O	FTDI Header Ready To Send; Active Low
3	BT_UART4_CTS_B	IO	UART4 Clear To Send
4	FTDI_RXI	IO	UART2 Transmit
5	BT_UART4_RX	IO	UART4 Receive
6	FTDI_TXO	IO	UART2 Receive
7	BT_UART4_RTS_B	IO	UART4 Ready To Send
8			
9	BASE_PER_3V3	P	Base board 3.3V;
10	FTDI_CTSN	IO	FTDI Header Clear To Send; Active Low
11	UART3_RXD	IO	UART3 Receive
12	GND	P	Digital Ground
13	UART3_TXD	IO	UART3 Transmit
14	ENET_MDIO	IO	ENET Management Data;
15	GND	P	Digital Ground
16	ENET_MDC	O	ENET Management Clock;
17	I2C4_SCL	IO	I2C #4 Clock
18	I2C3_SCL	IO	I2C #3 Clock
19	I2C4_SDA	IO	I2C #4 Data
20	I2C3_SDA	IO	I2C #3 Data

Note:
UART4 is used on SOMs with "WBD" or "WBE" assemblies.
MDIO interface is shared with SOMs with "EC" assembly. It is running on 2.5V levels in this case.
UART2 implements FTDI adapter connector layout for simple USB conversion with external module.
I2C3 is pulled up with 10K resistors on SOMs.
Please refer to Sonata-Board schematics and specific SOM datasheet for more details.

6.4.13 GPIO & Digital Audio (SPDIF)

The Sonata-Board exports alternate GPIO's and SPDIF through a standard 10 pin Header.

6.4.13.1 GPIO & SPDIF Pin-out (J8)

Table 6-26 GPIOs and SPDIF Connector Pin-out (J8)

Pin #	Sonata-Board Signal	Type	Description
1	BASE_PER_3V3	P	Base power 3.3V
2	GPIO1_IO11	IO	GPIO1_IO11
3	SPDIF_RX	IO	SPDIF Receive Data. Refer to note below
4	GPIO1_IO12	IO	GPIO1_IO12
5	SPDIF_EXT_CLK	IO	SPDIF External Clock
6	GPIO1_IO08	IO	GPIO1_IO08
7	SPDIF_TX	IO	SPDIF Transmit Data. Refer to note below
8	GPIO1_IO15	IO	GPIO1_IO15. Refer to note below
9	GND	P	Digital Ground
10	GPIO1_IO06	IO	GPIO1_IO06

Note:

Some of the above signals are connected differently in each SOM.
SPDIF_RX & SPDIF_TX are connected by serial resistors to CAN-FD interface.
GPIO1_IO15 is connected to RTC interface as RTC_IRQn.
Please refer to Sonata-Board schematics and specific SOM datasheet for more details.

6.4.14 Digital Audio (SAI1 & SAI2 & SAI5)

Sonata-Board exports SAI2 and SAI5 signals through standard 20 pin Header (J7).
SAI1 signals are exported via a 10 Pin Header (J22) and via Test Points connected in parallel to Ethernet PHY's RGMII signals.

Note:

For interfacing SAI1 pins via Test Points, EXP_ENET1_IO_LEVEL (GPIO Expander #2 port 0) line should be set to low.

SAI1 TXD[7..0] and RXD[7..0] pins are used by DART-MX8M and DART-MX8M-MINI for boot config. Care should be given not to drive them before rise of POR_B signal + 1ms; See "Boot Configuration" in data sheet.
DART-MX8M-PLUS boot configuration set by 4 BOOT_MODE[0..3] pins; Critical one is BOOT_MODE[0] connected internally to SAI1_TXD2 – previous module BOOT_CONFIG10.
DART-MX8M-MINI has PDM interface available on SAI1 & SAI5.
For more details, please refer to Sonata-Board schematics and specific SOM datasheet.

6.4.14.1 SAI2 & SAI5 & CAN-FD Header Pin-out (J7)

Table 6-27 SAI2 & SAI5 Header Pin-out (J7)

Pin #	Sonata-Board Signal	Type	Description
1	CAN_H	IO	CAN Bus High side;
2	CAN_L	IO	CAN Bus Low side
3	BASE_PER_1V8	P	Base board 1.8V
4	GND	P	Digital Ground
5	SAI2_RXC	IO	SAI2 Receive Bit Clock. Refer to note below
6	PMIC_STBY_REQ	O	SOM PMIC standby request; If used, isolate with high impedance input
7	SAI2_RXFS	IO	SAI2 Receive Frame Sync
8	SAI5_RXC	IO	SAI2 Receive Bit Clock. Refer to note below
9	SAI2_RXD0	IO	SAI2 Receive Data 0
10	SAI5_RXFS	IO	SAI5 Receive Frame Sync
11	SAI2_TXC	IO	SAI2 Transmit Bit Clock
12	SAI5_RXD0	IO	SAI5 Receive Data 0
13	SAI2_TXFS	IO	SAI2 Transmit Frame Sync
14	SAI5_RXD1	IO	SAI5 Receive Data 1
15	SAI2_TXD0	IO	SAI2 Transmit Data 0
16	SAI5_RXD2	IO	SAI5 Receive Data 2
17	SAI2_MCLK	IO	SAI2 Master Clock
18	SAI5_RXD3	IO	SAI2 Receive Data 0
19	SOM_VDD_PHY_1V8	P	programmable PMIC LDO. Refer to note below
20	SAI5_MCLK	IO	SAI5 Master Clock

Note:

Some of the above signals are connected differently in each SOM.
SAI2_RXC & SAI2_TXC are connected by serial resistors to DART-MX8M-PLUS CAN-FD interface.
SOM_VDD_PHY_1V8 is internal DART-MX8M HDMI PHY power.
SOM_VDD_PHY_1V8 is NVCC_SAI1_SAI5 output from DART-MX8M-PLUS.
For more details, please refer to Sonata-Board schematics and specific SOM datasheet.

6.4.14.2 SAI1 Header Pin-out (J22)

Table 6-28 SAI1 Header Pin-out (J22)

Pin #	Sonata-Board Signal	Type	Description
1	HDMI_DDC_SCL	O	I2C Serial Clock for DDC (Data Display Channel) (SoC side)
2	SAI1_RXFS	IO	SAI1 Receive Frame Sync
3	HDMI_DDC_SDA	IO	I2C Serial Data for DDC (Data Display Channel) (SoC side)
4	SAI1_RXC	IO	SAI1 Receive Bit Clock
5	HDMI_CEC	IO	Consumer Electronics Control; 1 Wire Serial; Bidirectional (SoC side)
6	SAI1_RXD0(GPIO4_IO02)	IO	SAI1 Receive Data 0 Note: Used by SOM for boot config @ power up
7	HDMI_HPD	O	HDMI Hot Plug Detect (SoC side)
8	SAI1_MCLK(GPIO4_IO20)	IO	SAI1 Master Clock
9	GPIO1_IO00	IO	GPIO. Refer to note below
10	GND	P	Digital Ground

Note

SAI1 alternate function for DART-MX8M-MINI is PDM.
In DART-MX8M GPIO1_IO00 is used as 32.768Khz reference clock for "WBD" assembly.
In DART-MX8M-MINI & DART-MX8M-PLUS it is used as GPIO
In DART-MX93 & DART-MX95 it is used as PIMIC interrupt.
For more details, please refer to Sonata-Board schematics and specific SOM datasheet.

6.4.14.3 SAI1 Test Points.

Table 6-29 SAI1 Test Points

Pin #	Sonata-Board Signal	Type	Description
TP24	ENET1_RGMII_RD0	IO	SAI1_RXD4(GPIO4_IO06)
TP29	ENET1_RGMII_TD0	IO	SAI1_TXD0(GPIO4_IO12)
TP28	ENET1_RGMII_RD1	IO	SAI1_RXD5(GPIO4_IO07)
TP22	ENET1_RGMII_TD1	IO	SAI1_TXD1(GPIO4_IO13)
TP32	ENET1_RGMII_RD3	IO	SAI1_RXD7(GPIO4_IO09)
TP25	ENET1_RGMII_TXC	IO	SAI1_TXD5(GPIO4_IO17)
TP27	ENET1_RGMII_RD2	IO	SAI1_RXD6(GPIO4_IO08)
TP30	ENET1_RGMII_TD2	IO	SAI1_TXD2(GPIO4_IO14)
TP31	ENET1_RGMII_TD3	IO	SAI1_TXD3(GPIO4_IO15)
TP23	ENET1_RGMII_RXC	IO	SAI1_TXC(GPIO4_IO11)
TP26	ENET1_RGMII_RX_CTL	IO	SAI1_TXFS(GPIO4_IO10)
TP34	ENET1_RGMII_TX_CTL	IO	SAI1_TXD4(GPIO4_IO16)
TP21	ENET1_MDC	IO	SAI1_RXD2(GPIO4_IO04). Refer to note below
TP33	ENET1_MDIO	IO	SAI1_RXD3(GPIO4_IO05). Refer to note below

Note:

These Test Points are used to access DART-MX8M & DART-MX8M-MINI SAI1 signals
MDIO interface is supported by DART-MX8M-PLUS & DART-MX95 only.
For more details, please refer to Sonata-Board schematics and specific SOM datasheet.

6.4.15 ECSPI & BT/WIFI Host Wake

This connector export 3 functions as follows:

- All SOMs supports the following functions:
  - ECSPI1 interface
  - BT and WIFI Host wake signals (in case of WBD/WBE assemblies)
- DART-MX8M-PLUS exports CAN-FD bus signals
- SD2_WP(GPIO2_IO20) GPIO line is connected differently in each SOM.

6.4.15.1 ECSPI1 & BT/WIFI Host Wake Header Pin-out (J10)

Table 6-30 ECSPI1 & BT/WIFI Host Wake Header Pin-out (J10)

Pin #	Sonata-Board Signal	Type	Description
1	BT_HOST_WAKE	O	SOM WIFI module Bluetooth host wake
2	ECSPI1_SCLK	IO	SPI Serial Clock
3	SD2_WP(GPIO2_IO20) SD1_DATA7(GPIO2_IO09) SD1_RESET_B(GPIO2_IO10) ADC_IN0	IO IO IO A	DART-MX8M; 1.8V/3.3V levels depends on SD2 interface DART-MX8M-MINI; 1.8V level supported only! DART-MX8M-PLUS; WBD - 1.8V level WB - 3.3V level DART-MX95; ADC input #0
4	ECSPI1_SS0	IO	SPI Slave Select; Active Low
5	WIFI_HOST_WAKE	O	SOM WIFI module WIFI host wake
6	ECSPI1_MOSI	IO	SPI Master Out Slave In
7	CAN-MX8MP_H	DSIO	DART-MX8M-PLUS CAN-FD Bus High side
8	ECSPI1_MISO	IO	SPI Master In Slave Out
9	CAN-MX8MP_H	DSIO	DART-MX8M-PLUS CAN-FD Bus Low side
10	GND	P	Digital Ground

Note:

ECSPI1 interface is used for the resistive touch controller assembled on the Sonata-Board. Thus, to use this interface via J10 header, ECSPI1_MISO needs to be disconnected from the resistive controller or use a different GPIO as slave select.
DART-MX95 can use ECSPI1 for the BT and WIFI module in WBE assembly.
BT HOST wake and/or WIFI HOST wake signals can be connected to J10.3 to use these functions; Logic is required to use both.
J10.3 is not connected in DART-MX93
For more details, please refer to Sonata-Board schematics and specific SOM datasheet.

6.4.16 QSPIA & QSPIB

The Sonata-Board exports QSPI and NAND signals through J12, J35 Headers.
Both interfaces share the same pins on the SOM.
SOMs capability is as follows:

- DART-MX8M, DART-MX8M-PLUS & DART-MX95 supports QSPIA
- DART-MX8M-MINI supports QSPIA when eMMC is assembled. In his case signals levels are 1.8V only.
- DART-MX93 supports none

For NAND and other functions of these pins refer to the SOMs data sheet.

6.4.16.1 QSPIA Header Pin-out (J12)

Table 6-31 QSPIA Header Pin-out (J12)

Pin #	Sonata-Board Signal	Type	Description
1	NAND_DQS	IO	QSPI A Strobe
2	NAND_READY_B	IO	GPIO3_IO16
3	NAND_DATA03	IO	QSPI A Data 3
4	NAND_CE2_B	IO	QSPI B Slave Select 0; Active Low
5	NAND_DATA02	IO	QSPI A Data 2
6	EN_SOM_VBAT_3V3	I	EN_SOM_VBAT_3V3
7	NAND_DATA01	IO	QSPI A Data 1
8	NAND_ALE	IO	QSPI A Serial Clock
9	NAND_DATA00	IO	QSPI A Data 0
10	NAND_CE0_B	IO	QSPI A Slave Select 0; Active Low

Note:
Only 1.8V level only is supported by DART-MX8M-MINI, DART-MX8M-PLUS & DART-MX95 for QSPIA interface.
Some of the above signals connected differently in each SOM.
Please refer to Sonata-Board schematics and specific SOM datasheet.
For NAND and other functions of these pins refer to the SOMs data sheet.

6.4.16.2 DSI/QSPIB Header Pin-out (J35)

Please refer to DSI/QSPIB Connector Pin-out (J35) section.

6.4.17 JTAG

The Sonata-Board exports the JTAG signals through a standard 1.27" 10 pin Header.

6.4.17.1 JTAG Header Pin-out (J24)

Table 6-32 JTAG Header Pin-out (J24)

Pin #	Sonata-Board Signal	Type	Description
1	JTAG_VREF	O	JTAG IO reference voltage. Connects to SOM_NVCC_3V3;
2	JTAG_TMS	I	JTAG Mode Select signal
3	GND	P	Digital Ground
4	JTAG_TCK	I	JTAG Clock signal; Requires 10K pull down.
5	GND	P	Digital Ground
6	JTAG_TDO	O	JTAG Data Out signal
7	NC		Not connected
8	JTAG_TDI	I	JTAG Data In signal
9	JTAG_NTRST_C	I	JTAG Reset signal
9	JTAG_MODE	I	DART-MX8M-PLUS only. Refer to note below
10	POR_B_D	IO	Programmer Reset; Open Drain; Used to put the SOC in reset state.

Note:
J24 is not assembled.
JTAG_MODE is required to set DART-MX8M-PLUS in JTAG mode. This is done via Sonata-Board assembly option. Refer to Sonata-Board schematics.
All SOMs JTAG interface is routed through this connector, except DART-MX93 which export it with UART4 signals. Refer for specific SOM datasheet.

6.4.18 Security - TBD

6.5 User Interfaces

6.5.1 Control Buttons

6.5.1.1 Power Switch (SW9)

The Power Switch SW9 Connect/Isolate the DC Power input to the Sonata-Board.

6.5.1.2 Power select Switch (SW1)

The Power select Switch SW1 Connects the J3.15, 27, 34 & 63 SOM pins to SOM power rail in case of DART-MX95. On the other hand, these pins are isolated in case of other SOMs.
This switch defaults to OFF set to ON when using DT95 SOM.

Table 5-33 Power Select Switch (SW1)

Pin #	SOM	Description
ON	DART-MX95 only	J3.15, 27, 34 & 63 connected to SOM power
OFF	All other SOMs	J3.15, 27, 34 & 63 isolated from SOM power

6.5.1.3 Boot Select (SW8)

The Boot select switch SW8 sets the SOM boot source & sequence. Refer to the specific SOM data sheet for detailed Boot description.

Table 5-34 Boot Select (SW8)

Pin #	Logic Level	Description
ON	High	External boot SD Card
OFF	Low	Internal boot Nand or eMMC

Note:
DART-MX8M-MINI NAND configuration currently not available.

6.5.1.4 User Buttons (SW2, SW3, SW4, SW5)

SW1, SW2, SW3 and SW4 are User Buttons connected to GPIO Expander #1 ports 4-7 for general purpose usage. In Linux release they can be configured, e.g., as Left, Enter, and Right Buttons in the DTS file.

6.5.1.5 Reset Button (SW6)

A press on SW6 will perform a system hardware-reset resulting in a complete power cycle of the SOMs.

6.5.1.6 ON/OFF Button (SW7)

The ON/OFF is Button supports the following:

1. **In OFF mode:** A short button press causes the internal power management state machine to change state to ON.
2. **In ON mode:** A short button press generates an interrupt (intended to initiate a software-controllable power-down).
   An approximate 5 second or more button press causes a forced OFF.
3. **In Suspend mode:** A short button press will the system to exit suspend mode.

6.5.1.7 Workaround for NXP DART-MX95 bring up bug (SW10) – Sonata-Board Rev1.1 only

Switch defaults to OFF set to ON when using DT95 SOM.

6.5.2 LED Indications

6.5.2.1 Power-On LEDs (D4, D5, D32)

Two LED indicators used:

- **D4** indicates that the Symphony-Board Carrier VCC_5V power is ON
- **D5** indicates that the Sonata-Board Carrier SOM_VBAT power is ON
- **D32** indicates that the Symphony-Board VCC_12V DC IN is ON.

6.5.2.2 SOM Power pins J3.15, 27, 34 & 63 LED (D7)

This led indicates that SOM power is supplied to these pins.

Note:
It is important to be sure that this power is supplied only in case of DART-MX95.

6.5.2.3 SFP+ module present indication LED (D21)

This LED indicates SFP+ presence.

6.5.2.4 GP LEDs (D20, D22, D24, D25)

- LEDs **D20**, **D22**, **D24** are General Purpose functionality LED controlled by GPIO Expander #2 ports 5-7.
- LED **D25** is a General-Purpose functionality LED controlled by a GPIO.

Note:
GP-LED D25 is controlled by GPIO which is part of the boot configuration pins in DART-MX8M/DART-MX8M-MINI.
Care should be given not to drive it before rise of POR_B signal + 1ms.

6.5.3 Power

The Sonata-Board is powered by a +12V power supply, connected either through a 2.0 mm power plug (J30) or alternatively through a 2 pin Terminal block (J29).

A 5V fan power output is available via shrouded 2 pin header (J34). Mating Housing Molex 22-01-3027; Connector Terminal Female Molex 08-50-0114;

6.5.3.1 DC-in Jack Pin-out (J30)

Table 6-35 DC-in Jack Pin-out (J30)

Pin #	Sonata-Board Signal	Type	Description
1	GND	P	Power supply return
2	GND	P	Power supply return
3	VCC_12V_PJ	P	Power supply 12V
4	VCC_12V_PJ	P	Power supply 12V

6.5.3.2 DC-in Terminal Block Pin-out (J29)

Table 6-36 DC-in 2 pins Terminal Block Pin-out (J29)

Pin #	Sonata-Board Signal	Type	Description
1	GND	P	Power supply return
2	VCC_PJ	P	Power supply 12V

6.5.3.3 DC-out FAN 5V Pin-out (J34)

Table 6-37 DC-out 5V FAN Header Pin-out (J34)

Pin #	Sonata-Board Signal	Type	Description
1	FAN_PWR	P	Power supply 5V out ***Note: Power via Ferrite Bead***
2	GND	P	Ground Return

Note:
J29, J34 are not assembled.
Sonata-Board has an assembly option to connect 12V fan to J34 instead of 5V.

6.5.3.4 RTC

The Sonata-Board features 12V input LDO, powering the on board DS1337U+ RTC Module.

Thus, to check RTC feature 12V input must be connected. Sonata-Board has an assembly option to add battery for those who wants to check it without power input.

7 Electrical Environmental Specifications

7.1 Absolute maximum electrical specifications

Table 7-1 DC Power Input absolute maximum electrical specifications

	Min	Max
Main Power Supply, DC-IN	-0.3V	20V

7.2 Operational electrical specifications

Table 7-2 DC Power Input Operational electrical specifications

	Min	Max
Main Power Supply, DC-IN	8V	18V

8 Environmental specifications

Table 8-1 Environmental specifications

	Min	Max
Commercial operating temperature range	0^0C	+70^0C
MTBF	>10kHRS	
Relative humidity, Operational	10%	90%
Relative humidity, Storage	5%	95%

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