Sonata Board 1.1

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11	BOOT CONFIG & MODE
12	CAN FD INTERFACE
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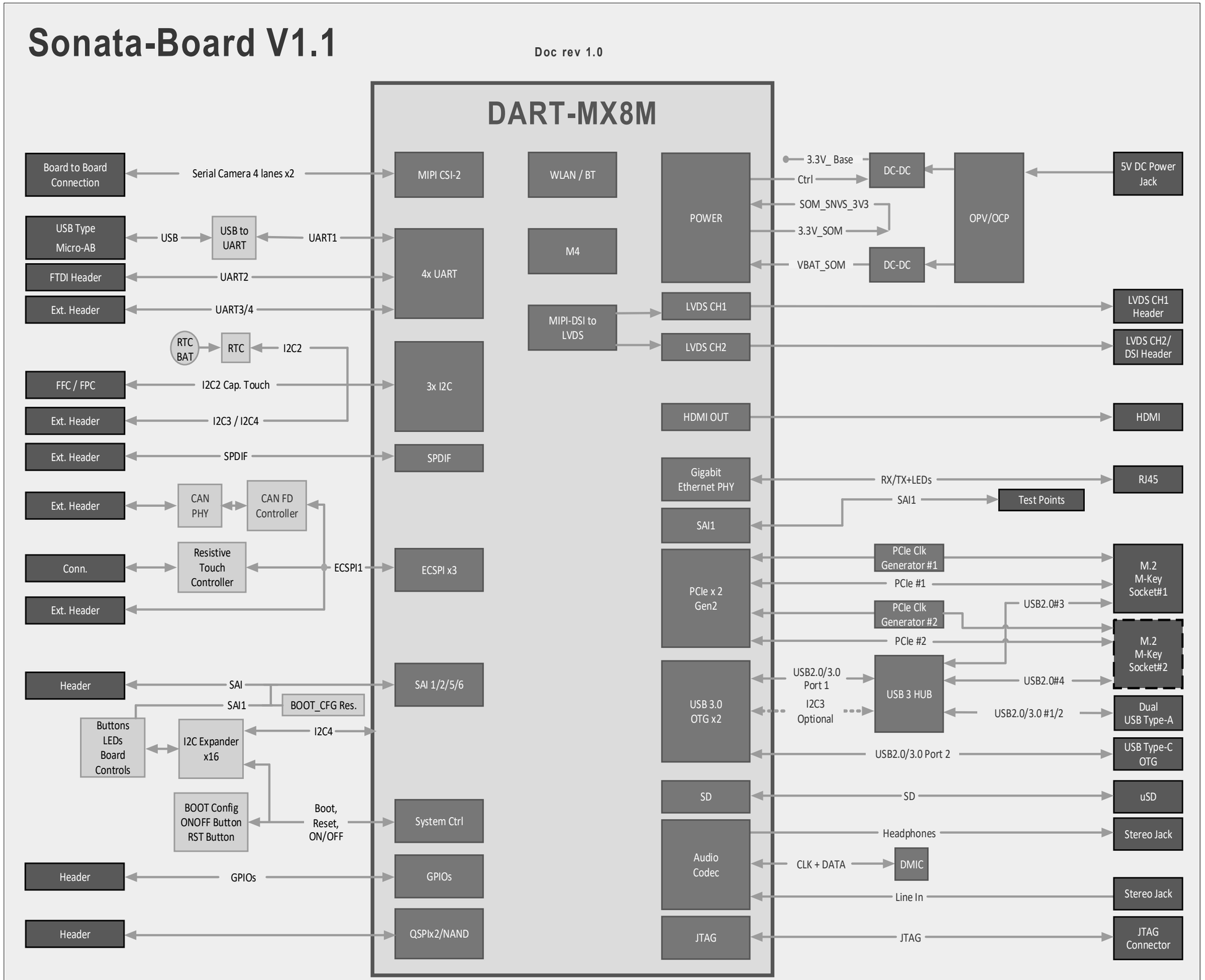
Revision History

Document	Carrier	Description
1.0	1.0	New layout to support DART-MX95, DART-MX93 & DART-MX91
1.1	1.1	1. Adding DT91 & DT93 block diagrams and symbols 2. DART-MX95 V1.1 J3.48 and J3.50 GPIO swap 3. Change IO EXP. #3 (U37) address to 0x22 4. SPI contention issue - U8.16 connect to U8.1 5. Remove R172 6. Combine R1 and R2. R1 removed, R2 changed to 174K and R3 changed to 31.6K 7. Connect 3.8 LED to regulator PGOOD pin 8. Buffer enable when RGB mode is off - Connect U26.7 to U37.2 9. Put RGMII filters on clock signals only. 10. Enable SOM_SNVS power by DIP SW when DT95 11. R28 changed to 1K 12. C205 changed to 1nF - solve DT95 boot always from eMMC 13. Remove SFP CLK EMI filtre L16 14. SFP RX p/n swap 15. Replace DT95 symbols 16. Add RGB 666 LCD connector - J36 17. Solve LDO RTC issue - Replace R102 and R106 with diode - Adding 1K resistr between 12V and U24 - Replace C136 to 10uF - Add voltage divider to Q10 to protect it fom burning 18. Trusted Platform Module (TPM) U60

For complete alternate function per pin
and specific SOM please refer to:
"DART_Compatibility_and_Pinout.XLS" located at:
ftp://ftp.variscite.com/DART_Compatibility

Title: 01. Cover			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 16, 2025		Sheet 1 of 23	

02A. Block Diagram – DART-MX8M



I2C BUS ADDRESS:

```
I2C1:   Internal to SOM

I2C2:   PU - 10K on U8
             10K on custom
        0x54 BOARD ID EEPROM Page0
        0x55 BOARD ID EEPROM Page1
        0x68 RTC
        0x38 CAPACITIVE TOUCH CTRLR
        0x3D USB-C CC Logic PTN5150AHXMP
        0x3C CSI P1 Camera (1V8) OV5640

I2C3:   PU - 5K on SOM
        0x60 SOM - Int. power ctrl.
        0x2D USB3 HUB
        0xXX Header J12

I2C4:   PU - 10K on U8
             10K on custom
        0x3C CSI P2 Camera (1V8) OV5640
        0xXX Header J12
        0xXX mPCIe J23 & J32
```

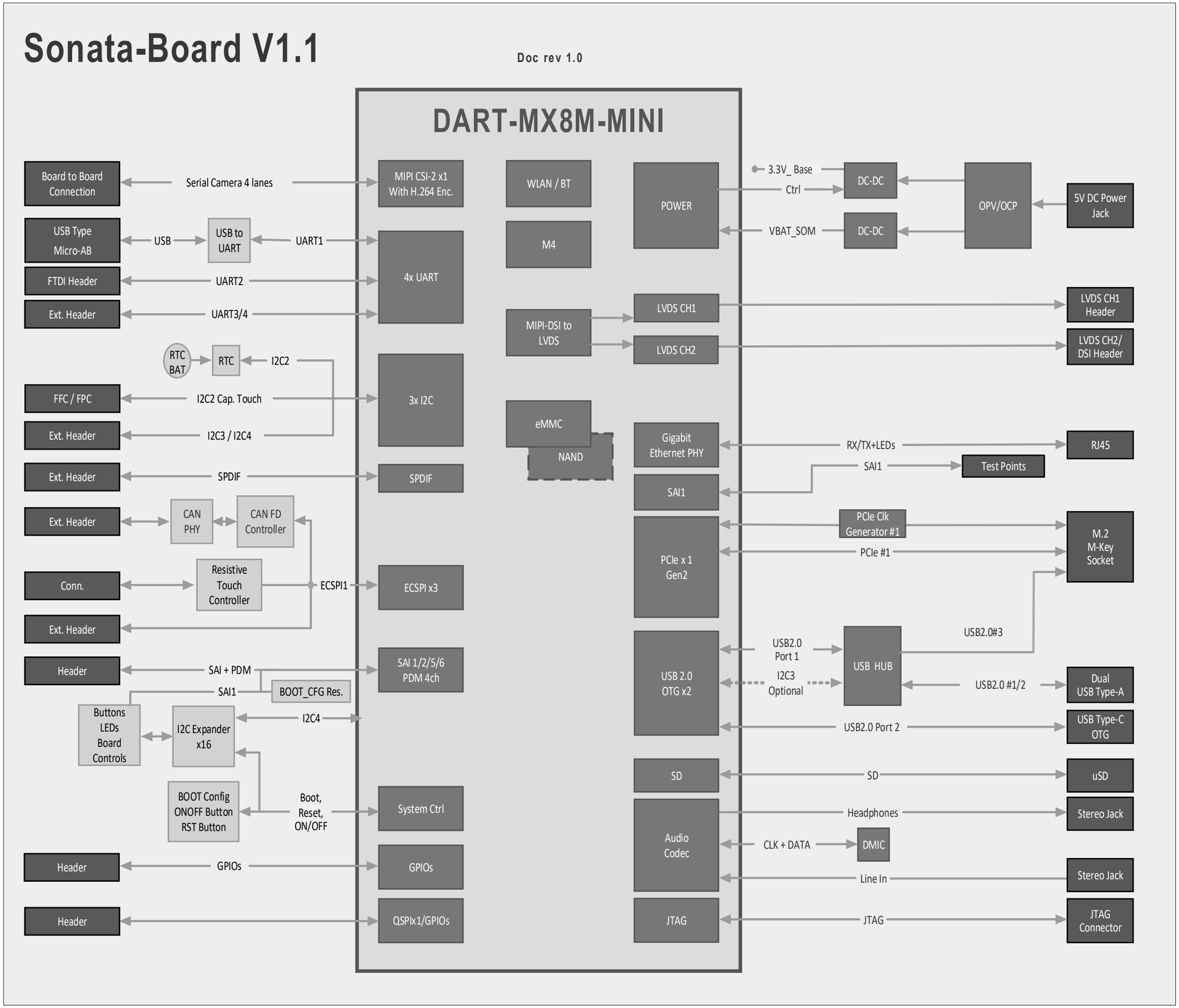
Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

Variscite

Title: 02A. Block Diagram with DART-MX8M			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 2 of 23	

02B. Block Diagram - DART-MX8M-MINI



I2C BUS ADDRESS:

```
I2C1:   Internal to SOM

I2C2:   PU - 10K on U8
            10K on custom
        0x54 BOARD ID EEPROM Page0
        0x55 BOARD ID EEPROM Page1
        0x68 RTC
        0x38 CAPACITIVE TOUCH CTRLR
        0x3D USB-C CC Logic PTN5150AHXMP
        0x3C CSI P1 Camera (1V8) OV5640

I2C3:   PU - 5K on SOM
        0x1A SOM - Int. CODEC
        0x2D USB3 HUB
        0xXX Header J12

I2C4:   PU - 10K on U8
            10K on custom
        0x3C CSI P1 Camera (1V8) OV5640
        0xXX Header J12
        0xXX mPCIe J23 & J32
```

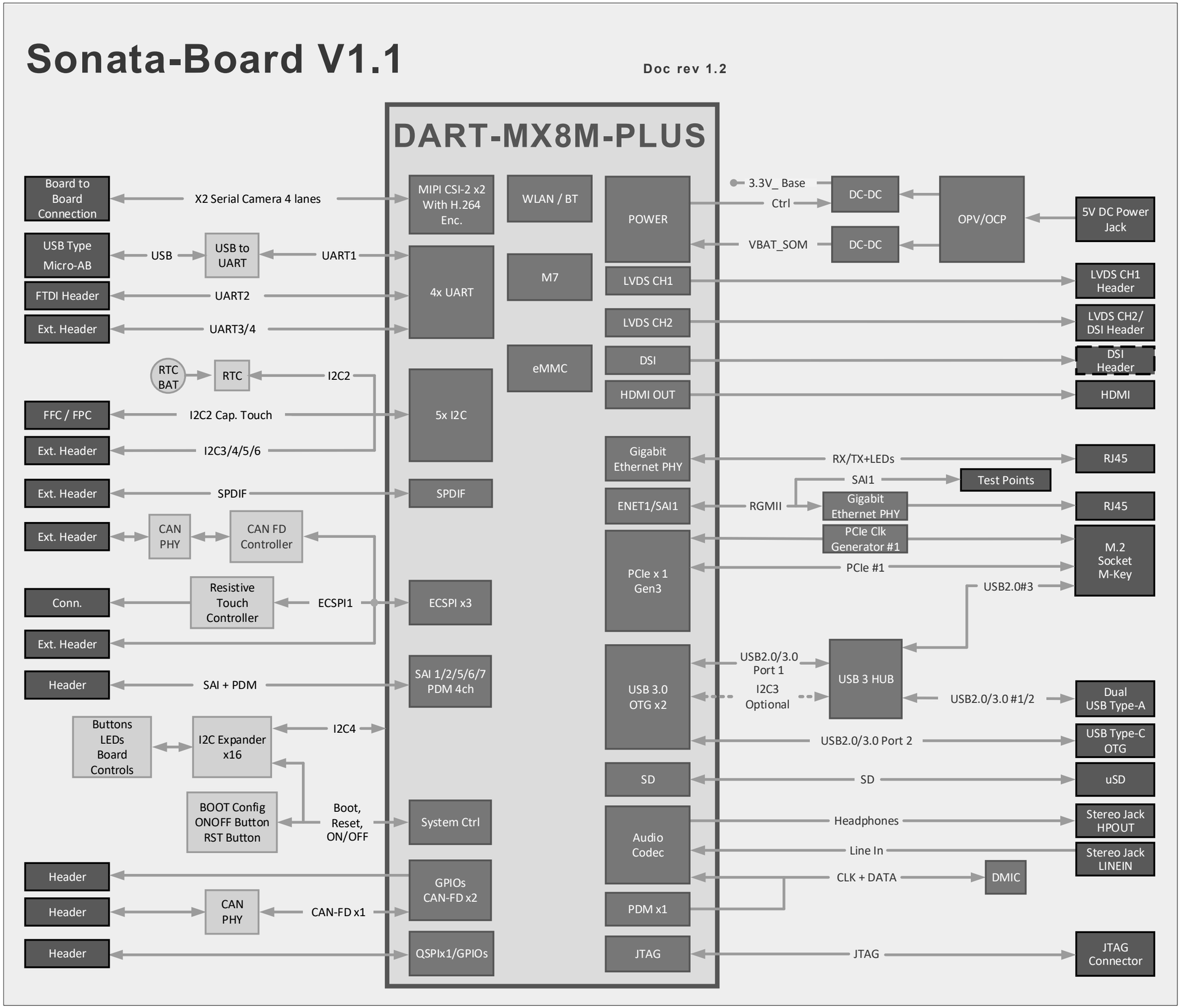
Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

Variscite

Title: 02B. Block Diagram with DART-MX8M-MINI			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 3 of 23	

02C. Block Diagram - DART-MX8M-PLUS



I2C BUS ADDRESS:

I2C1: Internal to SOM

I2C2: PU - 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM

0x2D USB3 HUB
0xXX Header J12

I2C4: PU - 10K on U8
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

Variscite

Title: 02B. Block Diagram with DART-MX8M-MINI			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 4 of 23	

02D. Block Diagram - DART-MX95

Sonata Board V1.1

Doc rev 1.2

DART-IMX95

CSI EDGE Connector
CSI1
DSI/CSI2
MIPI CSI1
MIPI DSI-CSI2
USBC
USB
USB to UART
UART1
Header
UART2(M33 DBG)
FTDI Header
UART3,5(4),8(2)
Up to 8x UART
UART5(4)
CAP. Touch FFC/FPC & CSI Conn.
Board ID
RTC
I2C3(2)
Up to 7x I2C
FTDI Header
I2C4(3)
FTDI Header DSI Conn. CSI Conn. 2xM.2 Conn.
I2C8(4)
I3C
IO EXPs.
Buttons LEDs Board Ctrl.
BOOT Cfg. ONOFF SW RST Button
Boot & System Ctrl.
Header
SPDIF
SPDIF/PWM
Header
CAN PHY
CAN FD Controller
FFC/FFP Conn.
RES. Touch Controller
Up to 8x ECSPI
Header
ECSPI1
BUFFER
TO W/BT
Header
CAN PHY
CAN-FDx1
Up to 5x CAN2.0B
GPIOs
Header
XSPI
Header
SAI + PDM
Up to 5x Digital Audio

LPDDR5 Up to 16 GB
eMMC
4Kb I2C EEPROM (Internal Use Only)
W/BT
24MHz Crystal
32768Hz Crystal

POWER
LVDS1
LVDS2/ DSI-CSI2
10G Ethernet
1G ETH PHY
1G Ethernet RGMII
PCIe1 Gen3
PCIe2 Gen3
USB PORT2 USB2.0
USB PORT1
uSDHC 4bit
Audio CODEC/ SAI3
PDMx1
JTAG
8 Channel ADC

3.3V_BASE
CTRL
VBAT_SOM
DC/DC
DC/DC
OPV/OCP
12V DC Power Jack
LVDS CH1 Header
LVDS CH2/ DSI-CSI2 Header
10G DART-IMX95
DSI1 DART-IMX8MP
ANALOG SW
SFP+ Fiber/Copper
DSI
SPI_TXD_1V8
RF_CTRL1
TPs
RX/TX+LEDS
RJ45 1G
RGMII
TPs
1G ETH PHY
RJ45 1G
PCIe REF CLK
PCIe1
M.2 M-KEY SOCKET #1
PCIe REF CLK
PCIe2
SPI_TX_1V8
WBT_PCM_IOs
DSI1 DART-IMX8MP_D3
ALNG SW
M.2 M-KEY SOCKET #2
Header SAI5
USB2.0
USB HUB
USB2.0 #3
USB2.0 #4
USB2.0 #1/2
DUAL USB TYPE-A
USB2.0/3.0
USBC OTG
SD
uSD
Headphones
Stereo Jack HPOUT
Line In
CLK +DATA
Stereo Jack LINEIN
DMIC
JTAG
JTAG connector
Header

Variscite

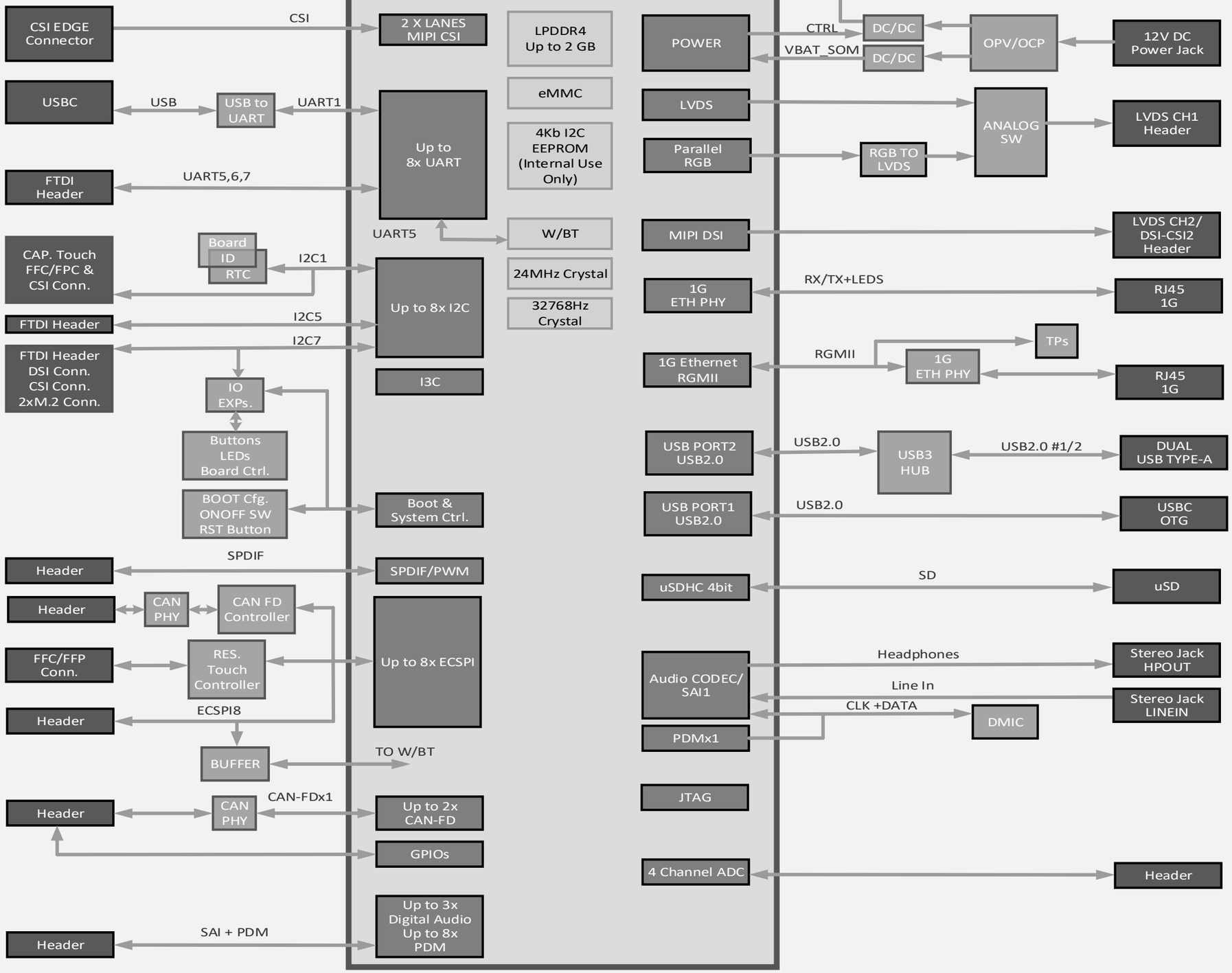
Title: 02D. Block Diagram with DART-MX95			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 5 of 23	

02E. Block Diagram - DART-MX93

Sonata Board V1.1

Doc rev 1.0

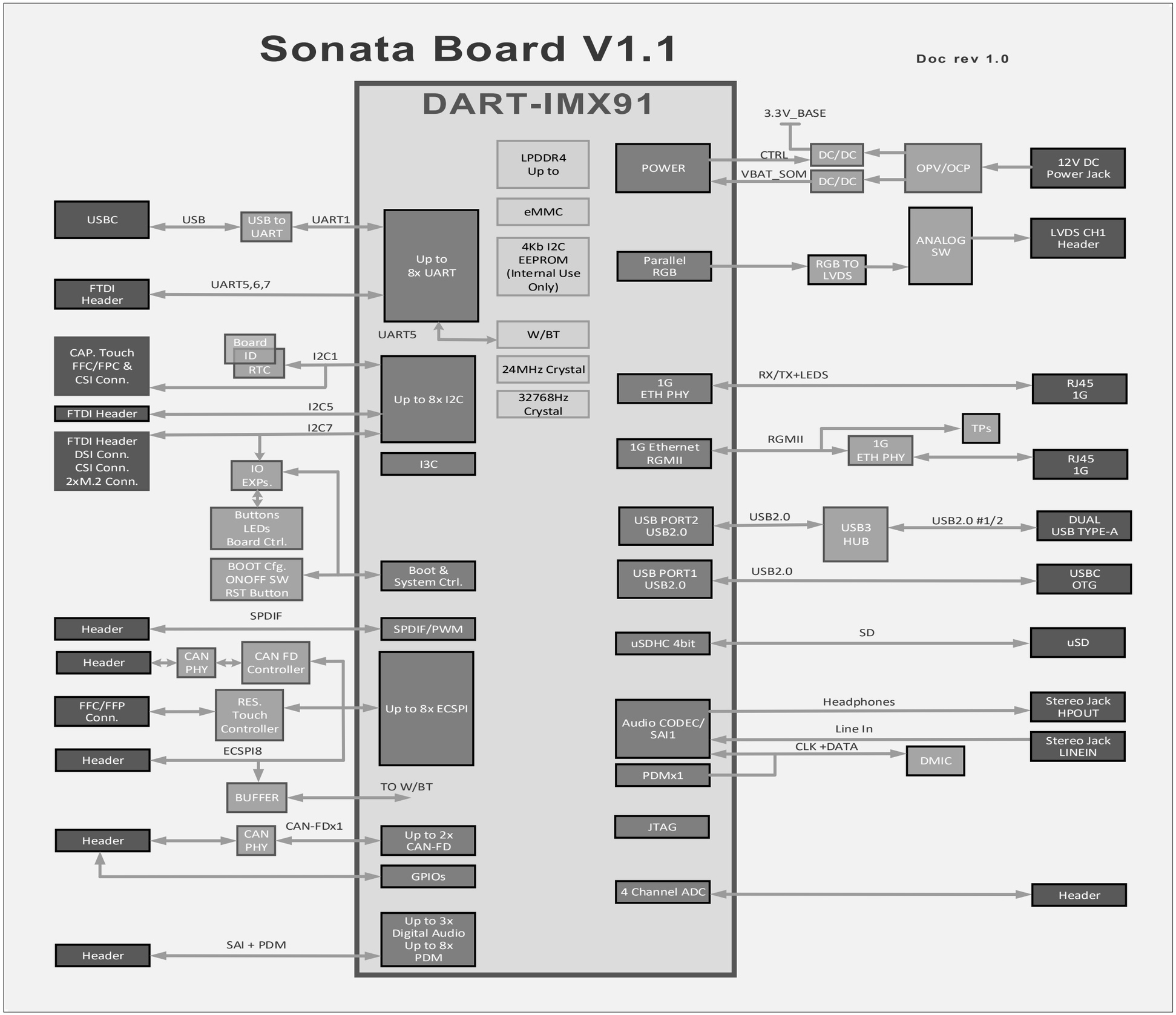
DART-IMX93



Variscite

Title: 02E. Block Diagram with DART-MX93			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 6 of 23	

02F. Block Diagram - DART-MX91



Variscite

Title: 02D. Block Diagram with DART-MX93			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 7 of 23	

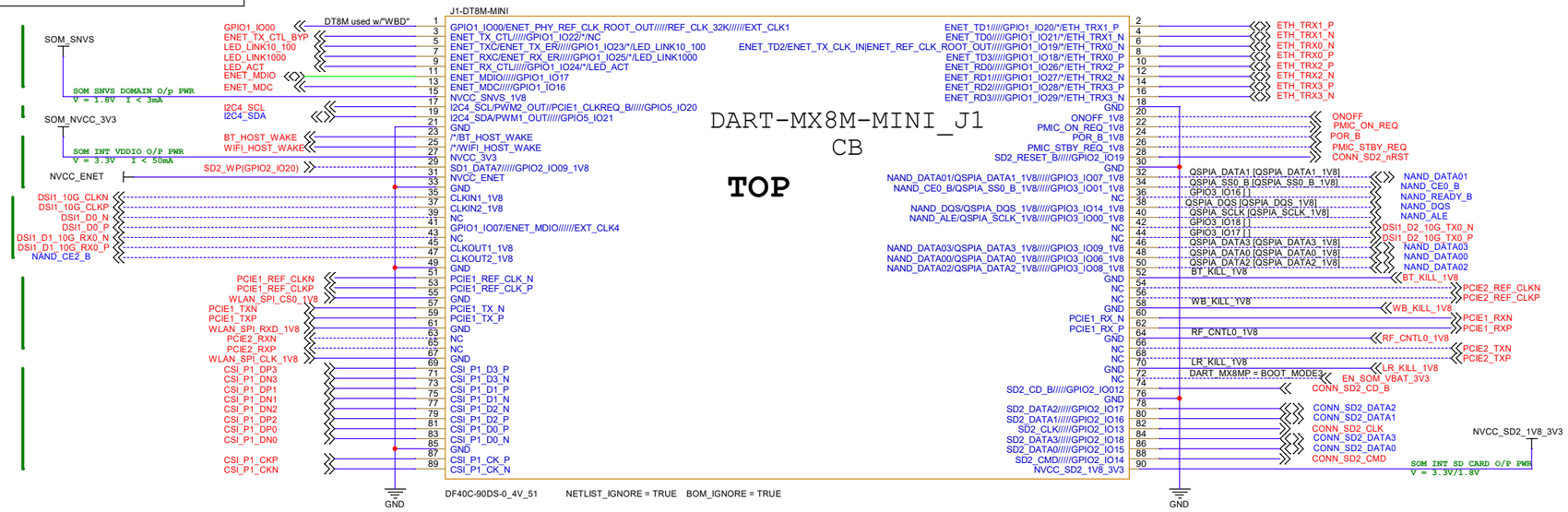
03A - DART-MX8M Connectors

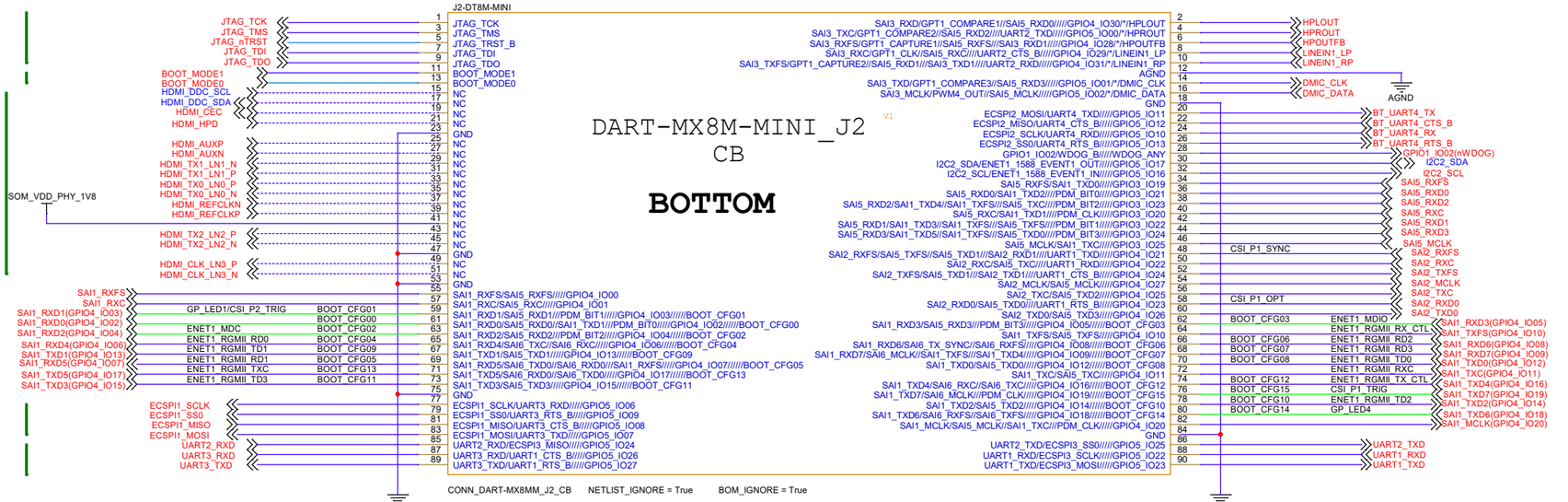
Note: Pinname with /*/ prefix denotes a HW assy option.

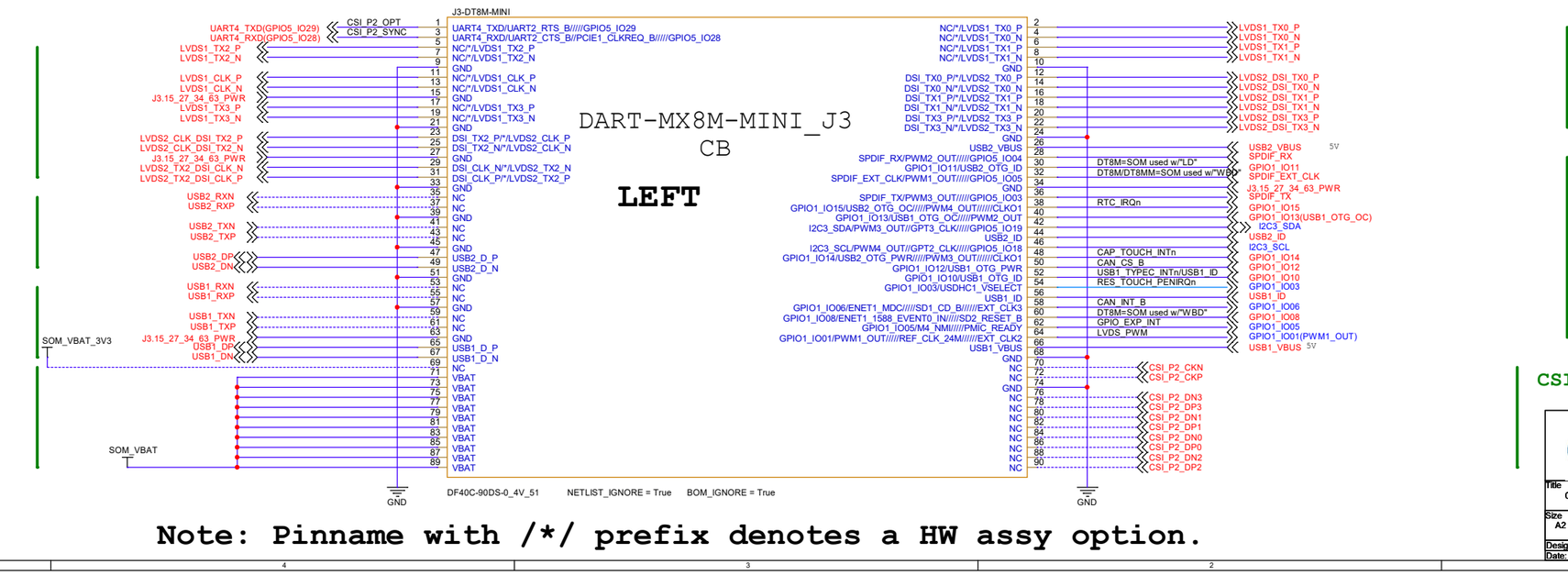
Title: 03. DART-MX8M Connectors			
Size: A2	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 8 of 23	

03B - DART-MX8M-MINI Connectors

***** Dotted nets - Functionality differ from DART-MX8M. *****







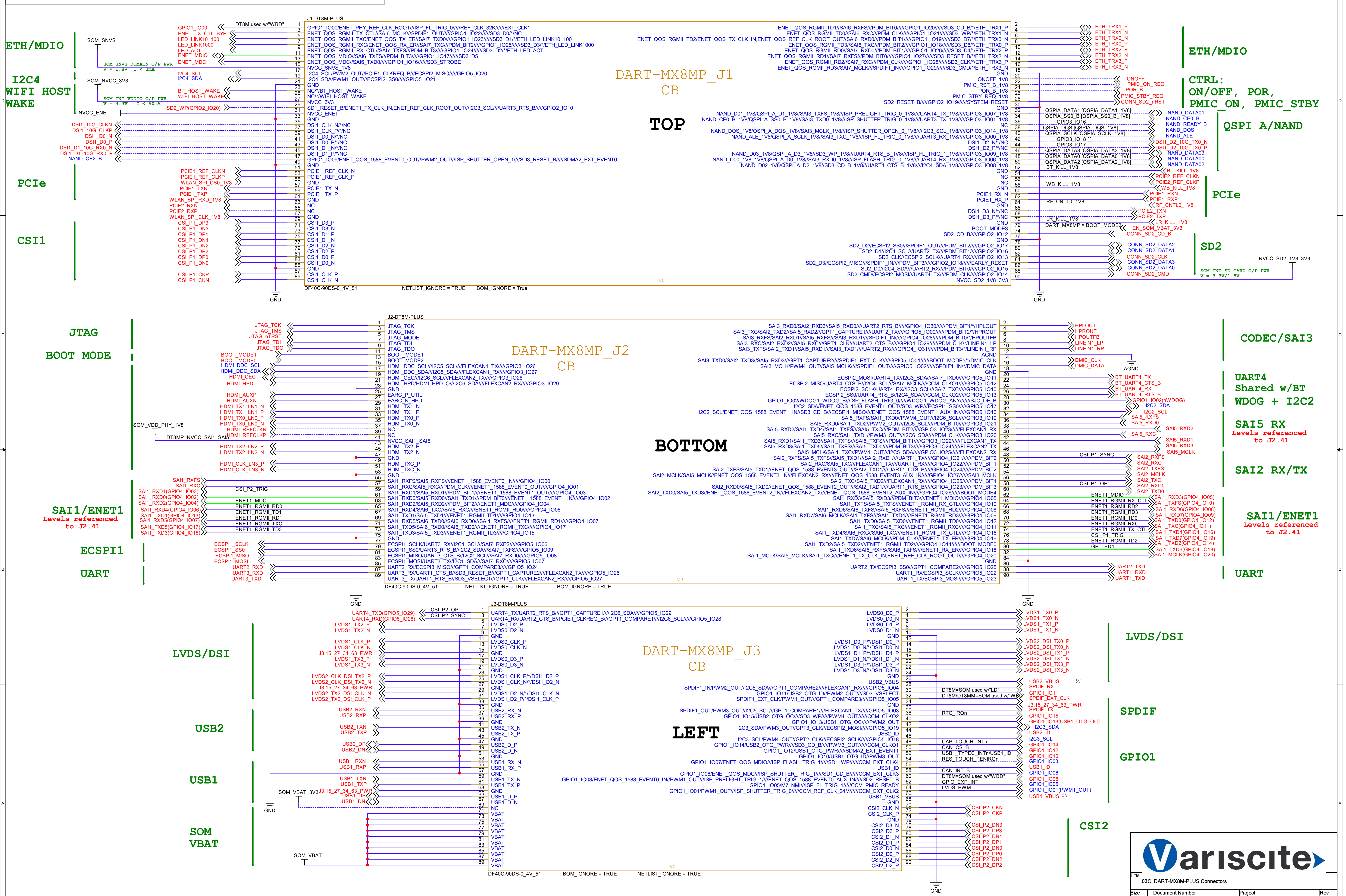
Note: Pinname with /*/ prefix denotes a HW assy option.

Variscite

Title: 03B. DART-MX8M Connectors			
Size: A2	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 9 of 23	

03C - DART-MX8M-PLUS Connectors

*** Dotted nets - Functionality differ from DART-MX8M. ***



Note: Pinname with /*/ prefix denotes a HW assy option.

Variscite

Title: 03C. DART-MX8M-PLUS Connectors			
Size: A2	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 10 of 23	

03D - DART-MX95 Connectors

J1-DT95

ETH/MDIO	GPIO1_IO00	1	PF09_INT_B_PF53_SOC_PG_PF53_ARM_PG	2	ETH_TRX1_P
	ENET_TX_CTL_BYP	3	NETC_ETH0_RGMII_TX_CTL/UART3_DTR_B//NETC_ETH0_RMII_TX_EN////FLEXIO2_FLEXIO6////GPIO4_IO6/*/NC	4	ETH_TRX1_N
	LED_LINK10_100	5	NETC_ETH0_RGMII_TX_CLK/CCMSRCGPCMIX_ENET_REF_CLK_ROOT////FLEXIO2_FLEXIO7/////GPIO4_IO7/*/LED_LINK10_100	6	ETH_TRX0_N
	LED_LINK1000	7	NETC_ETH0_RGMII_RX_CLK/NETC_ETH0_RMII_RX_ER////FLEXIO2_FLEXIO9/////GPIO4_IO9/*/LED_LINK1000	8	ETH_TRX0_P
I2C4	SOM_SNVS LED_ACT	9	NETC_ETH0_RGMII_RX_CTL/UART3_DSR_B//NETC_ETH0_RMII_CRS_DV///USB2_OTG_PWR////FLEXIO2_FLEXIO8/////GPIO4_IO8/*/LED_ACT	10	ETH_TRX2_P
	ENET_MDIO	11	NETC_MDIO/UART3_RIN_B//I3C2_SDA///USB1_OTG_PWR////FLEXIO2_FLEXIO1/////GPIO4_IO1	12	ETH_TRX2_N
	ENET_MDC	13	NETC_MDC/UART3_DCD_B//I3C2_SCL////FLEXIO2_FLEXIO0/////GPIO4_IO0	14	ETH_TRX3_P
		15	VDD_BBSM_1V8	16	ETH_TRX3_N
	GPIO_IO11(I2C8_SCL) RGB_B03	17	GPIO2_IO11/SPI3_SCK////TPM5_EXTCLK/////UART7_RTS_B//////I2C8_SCL/////FLEXIO1_FLEXIO11	18	
I2C4_SCL	GPIO_IO10(I2C8_SDA) RGB_D02	19	GPIO2_IO10/SPI3_SOUT////TPM4_EXTCLK/////UART7_CTS_B//////I2C8_SDA/////FLEXIO1_FLEXIO10	20	
I2C4_SDA		21	GND	22	ONOFF
WIFI HOST WAKE	BT_HOST_WAKE	23	NC/*/BT_HOST_WAKE_1V8	24	PMIC_ON_REQ
	WIFI_HOST_WAKE	25	NC/*/WIFI_HOST_WAKE_1V8	26	POR_B
		27	VDD_3V3	28	PMIC_STBY_REQ
	SD2_WP(GPIO2_IO20)	29	NC/*/ADC_IN0	30	CONN_SD2_nRST
NVCC_ENET		31	ETH_3V3	32	XSPI_DATA1
		33	GND	34	XSPI_SS0_B
	DSI1_10G_CLKN	35	ETH_CLKIN_N	36	BT_PCM_IN_1V8
	DSI1_10G_CLKP	37	ETH_CLKIN_P	38	XSPI_DQS
DSI	DSI1_D0_N	39	NC/*/RF_CNTL1_1V8	40	XSPI_CLK
	DSI1_D0_P	41	NC/*/SPI_TXD_1V8	42	ETH_TX0_N
	DSI1_D1_10G_RX0_N	43	ETH_RX0_N	44	ETH_TX0_P
	DSI1_D1_10G_RX0_P	45	ETH_RX0_P	46	XSPI_DATA3
	NAND_CE2_B	47	FLEXSPI_A_SS1_B/SAI5_RX_BCLK//SAI5_TX_DATA3///SAI2_RX_DATA7/////GPIO5_IO11	48	XSPI_DATA0
		49	GND	50	XSPI_DATA2
	PCIE1_REF_CLKN	51	PCIE1_CLKIN_N	52	
	PCIE1_REF_CLKP	53	PCIE1_CLKIN_P	54	GND/*/BT_KILL_1V8
	WLAN_SPI_CS0_1V8	55	GND/*/SPI_CS0_1V8	56	PCIE2_CLKIN_N/*/BT_PCM_CLK_1V8
PCIe	PCIE1_TXN	57	PCIE1_TX0_N	58	PCIE2_CLKIN_P/*/BT_PCM_OUT_1V8
	PCIE1_TXP	59	PCIE1_TX0_P	60	GND/*/WB_KILL_1V8
	WLAN_SPI_RXD_1V8	61	GND/*/SPI_RXD_1V8	62	PCIE1_RX0_N
	PCIE2_RXN	63	PCIE2_RX0_N/*/SPI_TXD_1V8	64	PCIE1_RX0_P
	PCIE2_RXP	65	PCIE2_RX0_P/*/BT_PCM_SYNC_1V8	66	GND/*/RF_CNTL0_1V8
	WLAN_SPI_CLK_1V8	67	GND/*/SPI_CLK_1V8	68	PCIE2_TX0_N/*/RF_CNTL3_1V8
	CSI_P1_DP3	69	MIPI_CSI_D3_P	70	PCIE2_TX0_P/*/RF_CNTL4_1V8
	CSI_P1_DN3	71	MIPI_CSI_D3_N	72	GND/*/LR_KILL_1V8
	CSI_P1_DP1	73	MIPI_CSI_D1_P	74	SAI1_TXD_BT_MODE2
	CSI_P1_DN1	75	MIPI_CSI_D1_N	76	SD2_CD_B
CSI1	CSI_P1_DN2	77	MIPI_CSI_D2_N	78	SD2_DATA2
	CSI_P1_DP2	79	MIPI_CSI_D2_P	80	SD2_DATA1
	CSI_P1_DP0	81	MIPI_CSI_D0_P	82	SD2_CLK
	CSI_P1_DN0	83	MIPI_CSI_D0_N	84	SD2_DATA3
		85	GND	86	SD2_DATA0
	CSI_P1_CKP	87	MIPI_CSI_CLK_P	88	SD2_CMD
	CSI_P1_CKN	89	MIPI_CSI_CLK_N	90	VDD_SDIO2

DART-MX95_J1

TOP

DF40C-90DS-0_4V_51

GND

GND

ETH/MDIO

CTRL: ON/OFF, POR, PMIC_ON, PMIC_STBY

QSPI A DSI

PCIe

BOOT MODE3

SD2

NVCC_SD2_1V8_3V3

SOM INT SD CARD O/P PWR V = 3.3V/1.8V

J2-DT95

	SOC	EXT			
JTAG	PD	10K PD	1	DAP_TCLK_SWCLK//CAN4_RX////FLEXIO1_FLEXIO30/////GPIO3_IO30/////UART5_CTS_B	2
	PU		3	DAP_TMS_SWDIO//CAN4_TX////FLEXIO2_FLEXIO31/////GPIO3_IO29/////UART5_RTS_B	4
			5	NC/*/ADC_IN7	6
	PU		7	DAP_TDI/MQS2_LEFT//NETC_TMR_1588_ALARM1////CAN2_TX////FLEXIO2_FLEXIO30/////GPIO3_IO28/////UART5_RX	8
			9	DAP_TDO_TRACESWO/MQS2_RIGHT//NETC_TMR_1588_ALARM2////CAN2_RX////FLEXIO1_FLEXIO31/////GPIO3_IO31/////UART5_TX	10
JTAG	UART2_TXD(GPIO1_IO07) BT_MODE1		11	UART2_TX/UART1_RTS_B//SPI2_SCK///TPM1_CH3////GPIO1_IO7/CCMSRCGPCMIX_BOOT_MODE1	12
BOOT MODE	SAI1_TXFS_BT_MODE2		13	SAI1_TX_SYNC/SAI1_TX_DATA1//SPI1_PCS0//UART2_DTR_B///MQS1_LEFT/////GPIO1_IO11/CCMSRCGPCMIX_BOOT_MODE2_P13	14
			15	NC/*/ADC_IN1	16
			17	NC/*/ADC_IN2	18
			19	NC	20
			21	NC	22
			23	GND	24
			25	AUD_P_UTIL	26
			27	AUD_N_HPD	28
	EARC_UTIL_P		29	NC/*/USDHC3_DATA3/FLEXSPI_A_DATA3//SAI5_RX_DATA3///SAI5_TX_BCLK////FLEXIO1_FLEXIO25/////GPIO3_IO25//////XSPI_SLV_DATA3	30
	EARC_HPD_N		31	NC/*/USDHC3_DATA2/FLEXSPI_A_DATA2//SAI5_RX_DATA2///SAI5_TX_SYNC////FLEXIO1_FLEXIO24/////GPIO3_IO24//////XSPI_SLV_DATA2	32
HDMI	CONN_SD3_DATA3		33	NC/*/USDHC3_DATA1/FLEXSPI_A_DATA1//SAI5_RX_DATA1///SAI5_TX_DATA0////FLEXIO1_FLEXIO23/////GPIO3_IO23//////XSPI_SLV_DATA1	34
	CONN_SD3_DATA2		35	NC/*/USDHC3_DATA0/FLEXSPI_A_DATA0//SAI5_TX_DATA3///SAI5_RX_BCLK////FLEXIO1_FLEXIO22/////GPIO3_IO22//////XSPI_SLV_DATA0	36
	CONN_SD3_DATA1		37	NC/*/COEX_SIN_1V8	38
	CONN_SD3_DATA0		39	NC/*/COEX_SOUT_1V8	40
			41	VDD_1V8	42
	CONN_SD3_CMD		43	NC/*/USDHC3_CMD/FLEXSPI_A_SS0_B//SAI5_TX_DATA2///SAI5_RX_SYNC////FLEXIO1_FLEXIO21/////GPIO3_IO21//////XSPI_SLV_CS	44
	CONN_SD3_CLK		45	NC/*/USDHC3_CLK/FLEXSPI_A_SCLK//SAI5_TX_DATA1///SAI5_RX_DATA0////FLEXIO1_FLEXIO20/////GPIO3_IO20//////XSPI_SLV_CLK	46
			47	GND	48
			49	TAMPER0	50
			51	TAMPER1	52
			53	GND	54
	XSPI_DATA4		55	FLEXSPI_A_DATA4/SAI5_TX_DATA0//SAI5_RX_DATA1////XSPI_SLV_DATA4/////GPIO5_IO4	56
	XSPI_DATA5		57	FLEXSPI_A_DATA5/SAI5_TX_SYNC//SAI5_RX_DATA2////SAI2_RX_DATA6////XSPI_SLV_DATA5/////GPIO5_IO5	58
SAI1	XSPI_DATA6 CSI_P2_TRIG		59	FLEXSPI_A_DATA6/SAI5_TX_BCLK//SAI5_RX_DATA3///SAI2_RX_DATA7/////XSPI_SLV_DATA6/////GPIO5_IO6	60
	XSPI_DATA7		61	FLEXSPI_A_DATA7/SAI5_RX_DATA0//SAI5_TX_DATA1////XSPI_SLV_DATA7/////GPIO5_IO7	62
	ENET2_MDC		63	NETC_MDC/UART4_DCD_B/SAI2_RX_SYNC////FLEXIO2_FLEXIO14/////GPIO4_IO14	64
	ENET2_RD0		65	NETC_ETH1_RGMII_RXD0/UART4_RX//SAI2_TX_DATA2///SAI4_RX_BCLK////FLEXIO2_FLEXIO24/////GPIO4_IO24//////NETC_ETH1_RMII_RXD0	66
	ENET2_TD1		67	NETC_ETH1_RGMII_TXD1/UART4_TX//SAI2_RX_DATA2///SAI4_TX_BCLK////FLEXIO2_FLEXIO18/////GPIO4_IO18//////NETC_ETH1_RMII_TXD1	68
	ENET2_RD1		69	NETC_ETH1_RGMII_RXD1/SPDIF1_IN//SAI2_TX_DATA3///SAI4_RX_DATA0////FLEXIO2_FLEXIO25/////GPIO4_IO25//////NETC_ETH1_RMII_RXD1	70
	ENET2_TXC		71	NETC_ETH1_RGMII_TX_CLK/CCMSRCGPCMIX_ENET_REF_CLK_ROOT//SAI2_TX_BCLK////FLEXIO2_FLEXIO21/////GPIO4_IO21	72
	ENET2_TD3		73	NETC_ETH1_RGMII_TXD3//SAI2_RX_DATA0////FLEXIO2_FLEXIO16/////GPIO4_IO16	74
			75	GND	76
	GPIO_IO07(SPI7_SCK)		77	GPIO2_IO7/SPI3_PCS1////SPI7_SCK/////UART6_RTS_B//////I2C7_SCL/////FLEXIO1_FLEXIO7	78
ECSPI1	GPIO_IO04(SPI7_PCS0)		79	GPIO2_IO4/TPM3_CH0//PDM_CLK////CAN4_TX////SPI7_PCS0/////UART6_TX//////I2C6_SDA/////FLEXIO1_FLEXIO4	80
	GPIO_IO05(SPI7_SIN)		81	GPIO2_IO5/TPM4_CH0//PDM_BIT_STREAM0////CAN4_RX////SPI7_SIN/////UART6_RX//////I2C6_SCL/////FLEXIO1_FLEXIO5	82
	GPIO_IO06(SPI7_SOUT)		83	GPIO2_IO6/TPM5_CH0//PDM_BIT_STREAM1////SPI7_SOUT/////UART6_CTS_B//////I2C7_SDA/////FLEXIO1_FLEXIO6	84
	GPIO_IO13(UART8_RX)		85	GPIO2_IO13/TPM4_CH2//PDM_BIT_STREAM3////SPI8_SIN/////UART8_RX//////I2C8_SCL/////FLEXIO1_FLEXIO13	86
UART	GPIO_IO15(UART3_RX)		87	GPIO2_IO15/UART3_RX////SPI8_SCK/////UART8_RTS_B//////UART4_RX/////FLEXIO1_FLEXIO15	88
	GPIO_IO14(UART3_TX)		89	GPIO2_IO14/UART3_TX////SPI8_SOUT/////UART8_CTS_B//////UART4_TX/////FLEXIO1_FLEXIO14	90

DART-MX95_J2

BOTTOM

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GND

GND

CODEC/SAI3

UART4 Shared w/BT WDOG + I2C2

SAI5

SAI2

SAI1 BOOT CFG

UART

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	GPIO_IO08(UART7_TX)	CSI_P2_SYNC	1	GPIO2_IO8/SPI3_PCS0////TPM6_CH0/////UART7_TX//////I2C7_SDA/////FLEXIO1_FLEXIO8	2
	GPIO_IO09(UART7_RX)	CSI_P2_OPT	3	GPIO2_IO9/SPI3_SIN////TPM3_EXTCLK/////UART7_RX//////I2C7_SCL/////FLEXIO1_FLEXIO9	4
LVDS/DSI			5	LVDS0_D2_P	6
			7	LVDS0_D2_N	8
			9	GND	10
			11	LVDS0_CLK_P	12
			13	LVDS0_CLK_N	14
			15	VBAT/*/NC	16
			17	LVDS0_D3_P	18
			19	LVDS0_D3_N	20
			21	GND	22
			23	LVDS1_CLK_P/*/DSICSI_D2_P	24
			25	LVDS1_CLK_N/*/DSICSI_D2_N	26
			27	VBAT/*/NC	28
			29	LVDS1_D2_N/*/DSICSI_CLK_N	30
			31	LVDS1_D2_P/*/DSICSI_CLK_P	32
			33	GND	34
			35	USB1_RX1_N	36
			37	USB1_RX1_P	38
			39	GND	40
			41	USB1_TX1_N	42
			43	USB1_TX1_P	44
			45	GND	46
			47	USB2_DP	48
			49	USB2_DN	50
			51	GND	52
			53	USB1_RX0_N	54
			55	USB1_RX0_P	56
			57	GND	58
			59	USB1_TX0_N	60
			61	USB1_TX0_P	62
			63	VBAT/*/NC	64
			65	USB1_DP	66
			67	USB1_DN	68
			69	NC	70
			71	VBAT	72
			73	VBAT	74
			75	VBAT	76
			77	VBAT	78
			79	VBAT	80
			81	VBAT	82
			83	VBAT	84
			85	VBAT	86
			87	VBAT	88
			89	VBAT	90

DART-MX95_J3

LEFT

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GND

GND

LVDS/DSI

SPDIF

GPIO1

CSI2

USB2

USB1

VBAT LICELL

SOM_VBAT

Will use GPIO instead of USB_ID native

BT_KILL_1V8 0R R43 GND
WB_KILL_1V8 0R R50
RF_CNTL0_1V8 0R R42
LR_KILL_1V8 0R R51

NC R46 GND
WLAN_SPI_RXD_1V8 0R NC R45
WLAN_SPI_CLK_1V8 0R R44

Note: Pinname with /*/ prefix denotes a HW assy option.

Variscite

Title	03D. DART-MX95 Connectors		
Size A2	Document Number Sonata Board	Project Sonata Board	Rev 1.1
Designer:	Shay V.	Approved By:	
Date:	Wednesday, April 02, 2025	Sheet 11 of 23	

03E - DART-MX93 Connectors

ETH/MDIO

I2C4

WIFI HOST WAKE

DSI

PCIe

CSI1

JTAG

BOOT MODE

HDMI

SAI1

ECSPI1

UART

USB2

USB1

SOM VBAT

LVDS/DSI

CODEC/SAI3

UART4 Shared w/BT WDOG + I2C2

SAI5 RX

Levels referenced to J2.41

SAI2 RX/TX

SAI1/ENET1

Levels referenced to J2.41

SPDIF

GPIO1

CSI2

QSPI A DSI

BOOT MODE3

SD2

SOM INT SD CARD O/P PWR
V = 3.3V/1.8V

CTRL: ON/OFF, POR, PMIC_ON, PMIC_STBY

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1	PMIC_NINT	ENET_QOS.RGMII_TD1/UART3.RTS_B/I3C2.PUR/USB1.OTG_OC/FLEXIO2.FLEXIO[4]/GPIO4.IO[4]/I3C2.PUR_B/*/ETH0_MDI_B_P	2
3	ENET_QOS.RGMII_TX_CTL/UART3.DTR_B///FLEXIO2.FLEXIO[6]/GPIO4.IO[6]/*/NC	ENET_QOS.RGMII_TD/UART3.TX///FLEXIO2.FLEXIO[5]/GPIO4.IO[5]/*/ETH0_MDI_B_M	4
5	ENET_QOS.RGMII_TXC/ENET_QOS.TX_ER///FLEXIO2.FLEXIO[7]/GPIO4.IO[7]/*/LED_LINK10_100	ENET_QOS.RGMII_TD2/ENET_QOS.TX_CLK/CAN2.RX/USB2.OTG_OC/FLEXIO2.FLEXIO[3]/GPIO4.IO[3]/*/ETH0_MDI_A_M	6
7	ENET_QOS.RGMII_RXC/ENET_QOS.RX_ER///FLEXIO2.FLEXIO[9]/GPIO4.IO[9]/*/ETH0_LED_LINK	ENET_QOS.RGMII_TD3//CAN2.TX/USB2.OTG_ID/FLEXIO2.FLEXIO[2]/GPIO4.IO[2]/*/ETH0_MDI_A_P	8
9	ENET_QOS.RGMII_RX_CTL/UART3.DSR_B//USB2.OTG_PWR/FLEXIO2.FLEXIO[8]/GPIO4.IO[8]/*/ETH0_LED_ACT	ENET_QOS.RGMII_RD/UART3.RX///FLEXIO2.FLEXIO[1]/GPIO4.IO[1]/*/ETH0_MDI_C_P	10
11	ENET_QOS.MDIO[4]/UART3.RIN_B/I3C2.SDA/USB1.OTG_PWR/FLEXIO2.FLEXIO[1]/GPIO4.IO[1]	ENET_QOS.RGMII_RD1/UART3.CTS_B/LPTMR2.ALT/FLEXIO2.FLEXIO[11]/GPIO4.IO[11]/*/ETH0_MDI_C_M	12
13	ENET_QOS.MDC[4]/UART3.DCD_B/I3C2.SCL/USB1.OTG_ID/FLEXIO2.FLEXIO[0]/GPIO4.IO[0]	ENET_QOS.RGMII_RD2///LPTMR2.ALT1/FLEXIO2.FLEXIO[12]/GPIO4.IO[12]/*/ETH0_MDI_D_P	14
15	NVCC_BBSM	ENET_QOS.RGMII_RD3///LPTMR2.ALT2/FLEXIO2.FLEXIO[13]/GPIO4.IO[13]/*/ETH0_MDI_D_M	16
17	GPIO2.IO[7]/SPI3.PCS1/ISI.D[1]/LCDIF.D[3]/SPI7.SCK/UART6.RTS_B/I2C7.SCL/FLEXIO1.FLEXIO[7]	GND	18
19	GPIO2.IO[6]/TPM5.CH/PDM.BIT_STREAM[1]/LCDIF.D[2]/SPI7.SOUT/UART6.CTS_B/I2C7.SDA/FLEXIO1.FLEXIO[6]	ONOFF	20
21	GND	PMIC_RST_B	22
23	NC/*/BT_HOST_WAKE	POR_B	24
25	NC/*/WIFI_HOST_WAKE	PMIC_STBY_REQ	26
27	VDD_3V3	CCMSRCGPCMIX.CLKO3////FLEXIO2.FLEXIO[28]/GPIO4.IO[28]	28
29	NC1	GND	30
31	NC2	NC/*/BT_DEV_WAKE	32
33	GND	NC3	34
35	NC4	NC/*/BT_PCM_IN	36
37	NC5	NC6	38
39	NC/*/RF_CNTL1	NC7	40
41	NC8	NC9	42
43	NC10	NC11	44
45	NC12	NC13	46
47	NC14	NC15	48
49	GND	NC16	50
51	NC17	GND/*/BT_KILL	52
53	NC18	NC/*/BT_PCM_CLK	54
55	GND/*/WLAN_SPI_CS0	NC/*/BT_PCM_OUT	56
57	NC19	GND/*/WB_KILL	58
59	NC20	NC21	60
61	GND/*/WLAN_SPI_RXD	NC22	62
63	NC/*/WLAN_SPI_TXD	GND/*/RF_CNTL0	64
65	NC/*/BT_PCM_SYNC	NC/*/RF_CNTL3	66
67	GND/*/WLAN_SPI_CLK	NC/*/RF_CNTL4	68
69	NC23	GND/*/LR_KILL	70
71	NC24	NC25	72
73	MIPI_CSI1_D1_P	USDHC2.CD_B/ENET_QOS.1588_EVENT_IN/I3C2.SCL//FLEXIO1.FLEXIO[0]/GPIO3.IO[0]	74
75	MIPI_CSI1_D1_N	GND	76
77	NC26	USDHC2.DATA2/ENET2.1588_EVENT1_OUT/MQS2.RIGHT//FLEXIO1.FLEXIO[5]/GPIO3.IO[5]	78
79	NC27	USDHC2.DATA1/ENET2.1588_EVENT1_IN/CAN2.RX//FLEXIO1.FLEXIO[4]/GPIO3.IO[4]	80
81	MIPI_CSI1_D0_P	USDHC2.CLK/ENET_QOS.1588_EVENT_OUT/I3C2.SDA//FLEXIO1.FLEXIO[1]/GPIO3.IO[1]	82
83	MIPI_CSI1_D0_N	USDHC2.DATA3/LPTMR2.ALT/MQS2.LEFT//FLEXIO1.FLEXIO[6]/GPIO3.IO[6]	84
85	GND	USDHC2.DATA/ENET2.1588_EVENT_OUT/CAN2.TX//FLEXIO1.FLEXIO[3]/GPIO3.IO[3]	86
87	MIPI_CSI1_CLK_P	USDHC2.CMD/ENET2.1588_EVENT_IN/I3C2.PUR/I3C2.PUR_B/FLEXIO1.FLEXIO[2]/GPIO3.IO[2]	88
89	MIPI_CSI1_CLK_N	NVCC_SD	90

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1	NC1	SAI1.RX_DATA[0]/SAI1.MCLK/SPI1.SOUT/UART2.DSR_B/MQS1.RIGHT/GPIO1.IO[14]/*/HPLOUT	2
3	NC2	SAI1.TX_BCLK/UART2.CTS_B/SPI1.SIN/UART1.DSR_B/CAN1.RX/GPIO1.IO[12]/*/HPROUT	4
5	NC3	I2C2.SCL/I3C1.PUR/UART2.DCD_B/TPM2.CH2/SAI1.RX_SYNC/GPIO1.IO[2]/I3C1.PUR_B/*/HPOUTFB	6
7	NC4	I2C2.SDA//UART2.RIN_B/TPM2.CH3/SAI1.RX_BCLK/GPIO1.IO[3]/*/LINEIN1_LP	8
9	NC5	SAI1.TX_SYNC[3]/SAI1.TX_DATA[1] [3]/SPI1.PCS/UART2.DTR_B/MQS1.LEFT/GPIO1.IO[11]/*/LINEIN1_RP	10
11	NC6	AGND	12
13	NC7	SAI1.TX_DATA[0]/UART2.RTS_B/SPI1.SCK/UART1.DTR_B/CAN1.TX/GPIO1.IO[13]/*/DMIC_CLK	14
15	NC8	UART2.RXD/UART1.CTS_B/SPI2.SOUT/TPM1.CH2/SAI1.MCLK/GPIO1.IO[6]/*/DMIC_DATA	16
17	NC9	GND	18
19	NC10	DAP.TDO_TRACESWO/MQS2.RIGHT//CAN2.RX/FLEXIO1.FLEXIO[31]/GPIO3.IO[31]/UART5.TX[1]	20
21	NC11	DAP.TMS_SWDIO////FLEXIO2.FLEXIO[31]/GPIO3.IO[29]/UART5.RTS_B[1]	22
23	GND	DAP.TDI/MQS2.LEFT//CAN2.TX/FLEXIO2.FLEXIO[3]/GPIO3.IO[28]/UART5.RX[1]	24
25	USDHC2.RESET_B/LPTMR2.ALT1///FLEXIO1.FLEXIO[7]/GPIO3.IO[7]/*/NC	DAP.TCLK_SWCLK////FLEXIO1.FLEXIO[3]/GPIO3.IO[3]/UART5.CTS_B[1]	26
27	ENET2.MDIO/UART4.RIN_B/SAI2.RX_BCLK//FLEXIO2.FLEXIO[15]/GPIO4.IO[15]/*/NC	WDOG1.WDOG_ANY//////GPIO1.IO[15]	28
29	USDHC3.DATA3/FLEXSPI.A_DATA[3]///FLEXIO1.FLEXIO[25]/GPIO3.IO[25]	I2C1.SDA/I3C1.SDA/UART1.RIN_B/TPM2.CH1//GPIO1.IO[1]	30
31	USDHC3.DATA2/FLEXSPI.A_DATA[2]///FLEXIO1.FLEXIO[24]/GPIO3.IO[24]	I2C1.SCL/I3C1.SCL/UART1.DCD_B/TPM2.CH//GPIO1.IO[0]	32
33	USDHC3.DATA1/FLEXSPI.A_DATA[1]///FLEXIO1.FLEXIO[23]/GPIO3.IO[23]	GPIO2.IO[19]/SAI3.RX_SYNC/PDM.BIT_STREAM[3]/LCDIF.D[15]/SPI5.SIN/SPI4.SIN/TPM6.CH2/SAI3.TX_DATA[0]	34
35	USDHC3.DATA/FLEXSPI.A_DATA[0]///FLEXIO1.FLEXIO[22]/GPIO3.IO[22]	GPIO2.IO[2]/SAI3.RX_DATA[0]/PDM.BIT_STREAM[0]/LCDIF.D[16]/SPI5.SOUT/SPI4.SOUT/TPM3.CH1/FLEXIO1.FLEXIO[2]	36
37	NC/*/COEX_SIN	GPIO2.IO[16]/SAI3.TX_BCLK/PDM.BIT_STREAM[2]/LCDIF.D[12]/UART3.CTS_B/SPI4.PCS2/UART4.CTS_B/FLEXIO1.FLEXIO[16]	38
39	NC/*/COEX_SOUT	GPIO2.IO[18]/SAI3.RX_BCLK/ISI.D[9]/LCDIF.D[14]/SPI5.PCS/SPI4.PCS/TPM5.CH2/FLEXIO1.FLEXIO[18]	40
41	VDD_1V8	GPIO2.IO[26]/USDHC3.DATA2/[2]/PDM.BIT_STREAM[1]/LCDIF.D[22]/TPM5.CH3/DAP.TDI/SPI8.PCS1/SAI3.TX_SYNC	42
43	USDHC3.CMD/FLEXSPI.A_SS_B///FLEXIO1.FLEXIO[21]/GPIO3.IO[21]/*/NC	GPIO2.IO[21]/SAI3.TX_DATA[0]/PDM.CLK/LCDIF.D[17]/SPI5.SCK/SPI4.SCK/TPM4.CH1/SAI3.RX_BCLK	44
45	USDHC3.CLK/FLEXSPI.A_SCLK///FLEXIO1.FLEXIO[2]/GPIO3.IO[2]/*/NC	GPIO2.IO[17]/SAI3.MCLK/ISI.D[8]/LCDIF.D[13]/UART3.RTS_B/SPI4.PCS1/UART4.RTS_B/FLEXIO1.FLEXIO[17]	46
47	GND	GPIO2.IO[1]/SPI3.SOUT/ISI.D[4]/LCDIF.D[6]/TPM4.EXTCLK/UART7.CTS_B/I2C8.SDA/FLEXIO1.FLEXIO[1]	48
49	NC12	PDM.CLK/MQS1.LEFT///LPTMR1.ALT/GPIO1.IO[8]/CAN1.TX	50
51	NC13	NC14	52
53	GND	GPIO2.IO[27]/USDHC3.DATA3[2]/CAN2.RX/LCDIF.D[23]/TPM6.CH3/DAP.TMS_SWDIO/SPI5.PCS1/FLEXIO1.FLEXIO[27]	54
55	NC15	PDM.BIT_STREAM[0]/MQS1.RIGHT/SPI1.PCS1/TPM1.EXTCLK/LPTMR1.ALT1/GPIO1.IO[9]/CAN1.RX	56
57	NC16	NC17	58
59	NC18	GPIO2.IO[25]/USDHC3.DATA1[2]/CAN2.TX/LCDIF.D[21]/TPM4.CH3/DAP.TCLK_SWCLK/SPI7.PCS1/FLEXIO1.FLEXIO[25]	60
61	NC19	NC20	62
63	NC21	ENET2.RGMII_RX_CTL/UART4.DSR_B/SAI2.TX_DATA[0]//FLEXIO2.FLEXIO[22]/GPIO4.IO[22]	64
65	ENET2.RGMII_RD/UART4.RX/SAI2.TX_DATA[2]//FLEXIO2.FLEXIO[24]/GPIO4.IO[24]	ENET2.RGMII_RD2/UART4.CTS_B/SAI2.MCLK/MQS2.RIGHT/FLEXIO2.FLEXIO[26]/GPIO4.IO[26]	66
67	ENET2.RGMII_TD1/UART4.RTS_B/SAI2.RX_DATA[2]//FLEXIO2.FLEXIO[18]/GPIO4.IO[18]	ENET2.RGMII_RD3/SPDIF1.OUT/SPDIF1.IN/MQS2.LEFT/FLEXIO2.FLEXIO[27]/GPIO4.IO[27]	68
69	ENET2.RGMII_RD1/SPDIF1.IN/SAI2.TX_DATA[3]//FLEXIO2.FLEXIO[25]/GPIO4.IO[25]	ENET2.RGMII_TD/UART4.TX/SAI2.RX_DATA[3]//FLEXIO2.FLEXIO[19]/GPIO4.IO[19]	70
71	ENET2.RGMII_TXC/ENET2.TX_ER/SAI2.TX_BCLK//FLEXIO2.FLEXIO[21]/GPIO4.IO[21]	ENET2.RGMII_RXC/ENET2.RX_ER/SAI2.TX_DATA[1]//FLEXIO2.FLEXIO[23]/GPIO4.IO[23]	72
73	ENET2.RGMII_TD3//SAI2.RX_DATA[0]//FLEXIO2.FLEXIO[16]/GPIO4.IO[16]	ENET2.RGMII_TX_CTL/UART3.DTR_B/SAI2.TX_SYNC//FLEXIO2.FLEXIO[2]/GPIO4.IO[2]	74
75	GND	CCMSRCGPCMIX.CLKO1////FLEXIO1.FLEXIO[26]/GPIO3.IO[26]	76
77	GPIO2.IO[15]/UART3.RX/ISI.D[7]/LCDIF.D[11]/SPI8.SCK/UART8.RTS_B/UART4.RX/FLEXIO1.FLEXIO[15]	ENET2.RGMII_TD2/ENET2.TX_CLK/SAI2.RX_DATA[1]//FLEXIO2.FLEXIO[17]/GPIO4.IO[17]	78
79	GPIO2.IO[12]/TPM3.CH2/PDM.BIT_STREAM[2]/LCDIF.D[8]/SPI8.PCS/UART8.TX/I2C8.SDA/SAI3.RX_SYNC	GPIO2.IO[11]/SPI3.SCK/ISI.D[5]/LCDIF.D[7]/TPM5.EXTCLK/UART7.RTS_B/I2C8.SCL/FLEXIO1.FLEXIO[11]	80
81	GPIO2.IO[13]/TPM4.CH2/PDM.BIT_STREAM[3]/LCDIF.D[9]/SPI8.SIN/UART8.RX/I2C8.SCL/FLEXIO1.FLEXIO[13]	NC/*/ETH_INT	82
83	GPIO2.IO[14]/UART3.TX/ISI.D[6]/LCDIF.D[10]/SPI8.SOUT/UART8.CTS_B/UART4.TX/FLEXIO1.FLEXIO[14]	GND	84
85	GPIO2.IO[5]/TPM4.CH/PDM.BIT_STREAM[0]/LCDIF.D[1]/SPI7.SIN/UART6.RX/I2C6.SCL/FLEXIO1.FLEXIO[5]	GPIO2.IO[4]/TPM3.CH/PDM.CLK/LCDIF.D[0]/SPI7.PCS/UART6.TX/I2C6.SDA/FLEXIO1.FLEXIO[4]	86
87	GPIO2.IO[9]/SPI3.SIN/ISI.D[3]/LCDIF.D[5]/TPM3.EXTCLK/UART7.RX/I2C7.SCL/FLEXIO1.FLEXIO[9]	UART1.RX/SECO.RX/SPI2.SIN/TPM1.CH//GPIO1.IO[4]	88
89	GPIO2.IO[8]/SPI3.PCS/ISI.D[2]/LCDIF.D[4]/TPM6.CH/UART7.TX/I2C7.SDA/FLEXIO1.FLEXIO[8]	UART1.TX/SECO.TX/SPI2.PCS/TPM1.CH1//GPIO1.IO[5]	90

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1	NC1	LVDS_D0_P	2
3	NC2	LVDS_D0_N	4
5	LVDS_D2_P	LVDS_D1_P	6
7	LVDS_D2_N	LVDS_D1_N	8
9	GND	GND	10
11	LVDS_CLK_P	MIPI_DSI1_D0_P	12
13	LVDS_CLK_N	MIPI_DSI1_D0_N	14
15	GND	MIPI_DSI1_D1_P	16
17	LVDS_D3_P	MIPI_DSI1_D1_N	18
19	LVDS_D3_N	MIPI_DSI1_D3_P	20
21	GND	MIPI_DSI1_D3_N	22
23	MIPI_DSI1_D2_P	GND	24
25	MIPI_DSI1_D2_N	5V	26
27	GND	USB2_VBUS	28
29	MIPI_DSI1_CLK_N	NC3	30
31	MIPI_DSI1_CLK_P	GPIO2.IO[0]//ISI.PCLK/LCDIF.PCLK/SPI6.PCS/UART5.TX[1]/I2C5.SDA/FLEXIO1.FLEXIO[0]	32
33	GND	NC/*/WLAN_SPI_IRQ	34
35	NC4	GND	36
37	NC6	NC5	38
39	GND	GPIO2.IO[2]/I2C4.SDA/ISI.FRAME_VALID/LCDIF.VSYNC/SPI6.SOUT/UART5.CTS_B[1]/I2C6.SDA/FLEXIO1.FLEXIO[2]	40
41	NC8	NC7	42
43	NC9	GPIO2.IO[22]/USDHC3.CLK[2]/SPDIF1.IN/LCDIF.D[18]/TPM5.CH1/TPM6.EXTCLK/I2C5.SDA/FLEXIO1.FLEXIO[22]	44
45	GND	USB2_ID	46
47	USB2_D_P	GPIO2.IO[23]/USDHC3.CMD[2]/SPDIF1.OUT/LCDIF.D[19]/TPM6.CH1//I2C5.SCL/FLEXIO1.FLEXIO[23]	48
49	USB2_D_N	CCMSRCGPCMIX.CLKO2////FLEXIO1.FLEXIO[27]/GPIO3.IO[27]	50
51	GND	GPIO2.IO[1]//ISI.D[0]/LCDIF.DE/SPI6.SIN/UART5.RX[1]/I2C5.SCL/FLEXIO1.FLEXIO[1]	52
53	NC10	CCMSRCGPCMIX.CLKO4////FLEXIO2.FLEXIO[29]/GPIO4.IO[29]	54
55	NC12	NC11	56
57	GND	USB1_ID	58
59	NC13	GPIO2.IO[3]/I2C4.SCL/ISI.LINE_VALID/LCDIF.HSYNC/SPI6.SCK/UART5.RTS_B[1]/I2C6.SCL/FLEXIO1.FLEXIO[3]	60
61	NC15	NC14	62
63	GND	PDM.BIT_STREAM[1]/M33.NMI/SPI2.PCS1/TPM2.EXTCLK/LPTMR1.ALT2/GPIO1.IO[1]	64
65	USB1_D_P	GPIO2.IO[24]/USDHC3.DATA[2]//LCDIF.D[2]/TPM3.CH3/DAP.TDO_TRACESWO/SPI6.PCS1/FLEXIO1.FLEXIO[24]	66
67	USB1_D_N	USB1_VBUS	68
69	NC16	GND	70
71	VBAT	TAMPER0	72
73	VBAT	TAMPER1	74
75	VBAT	GND	76
77	VBAT	ADC_IN0	78
79	VBAT	ADC_IN1	80
81	VBAT	ADC_IN2	82
83	VBAT	ADC_IN3	84
85	VBAT	CLKIN1	86
87	VBAT	CLKIN2	88
89	VBAT	PMIC_ON_REQ	90

DF40C-90DS-0_4V_51_v1

Note: Pinname with /*/ prefix denotes a HW assy option.

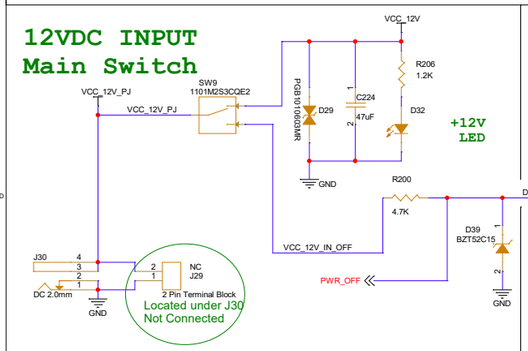
Title	03E. DART-MX93 Connectors
Size	A2
Document Number	Sonata Board
Project	Sonata Board
Rev	1.1
Designer	Shay V.
Approved By	
Date	Wednesday, April 02, 2025
Sheet	12 of 23

03F - DART-MX91 Connectors

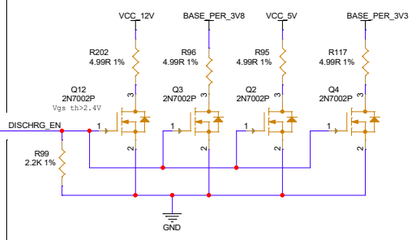
Title	03F. DART-MX91 Connectors
Size	A2
Document Number	Sonata Board
Project	Sonata Board
Rev	1.1
Designer	Shay V.
Approved By	
Date	Wednesday, April 02, 2025
Sheet	13 of 23

04. Power, RTC,Board ID

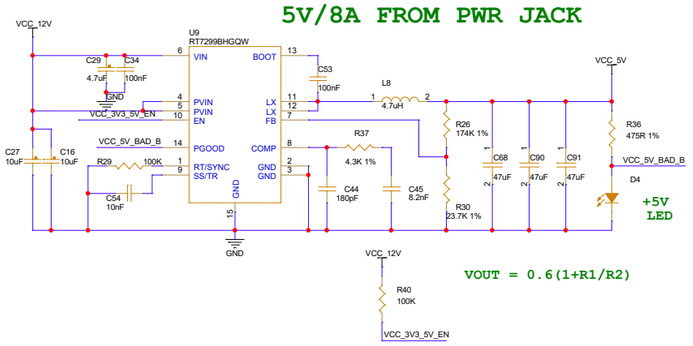
12VDC INPUT Main Switch



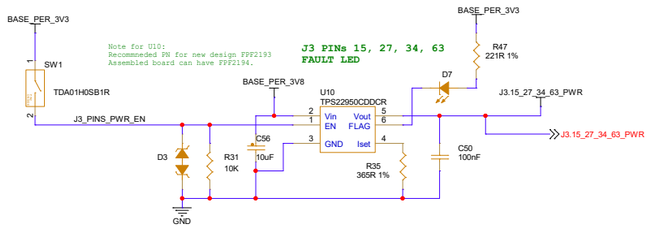
POWER DISCHARGE



5V/8A FROM PWR JACK

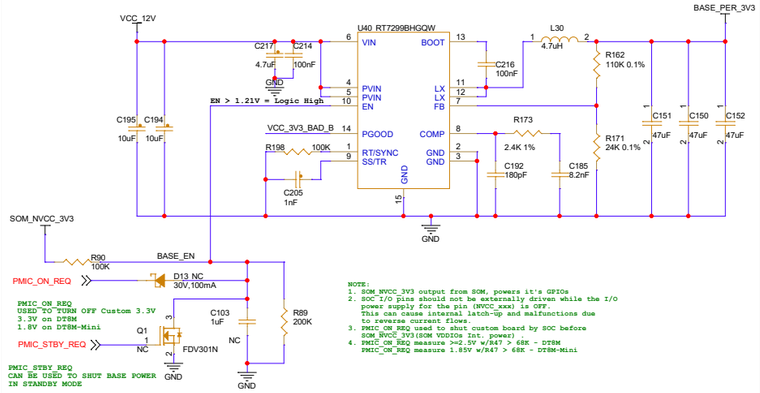


J3 PINS 15 27 34 63 POWER

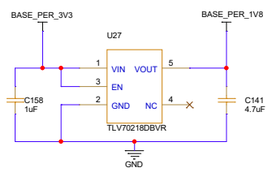


Switch deafults to OFF,
Must be set to ON when connecting
DT95 SOM

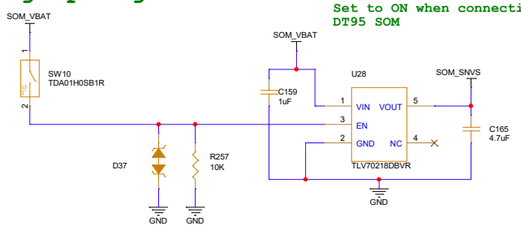
3.35V/8A FROM PWR JACK



1.8V/0.3A BASE

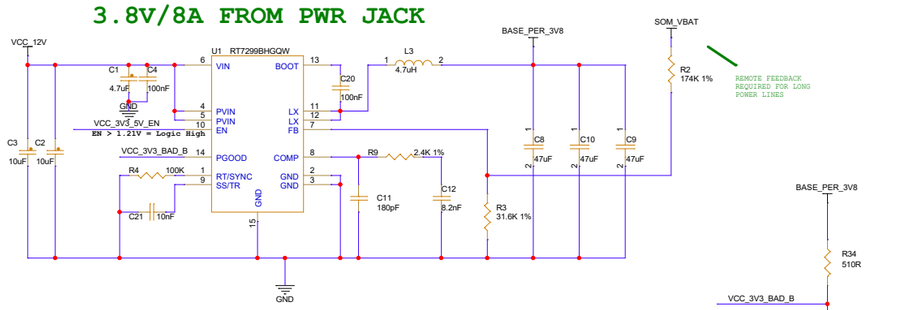


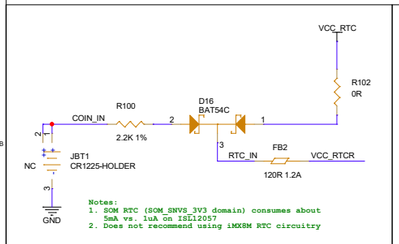
Workaround for NXP DART-MX95 bring up bug



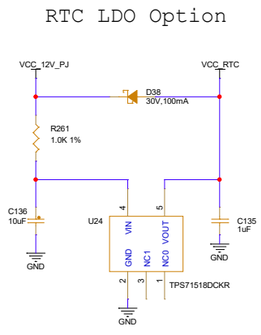
Switch deafults to OFF,
Set to ON when connecting
DT95 SOM

3.8V/8A FROM PWR JACK

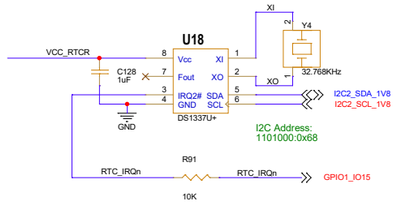




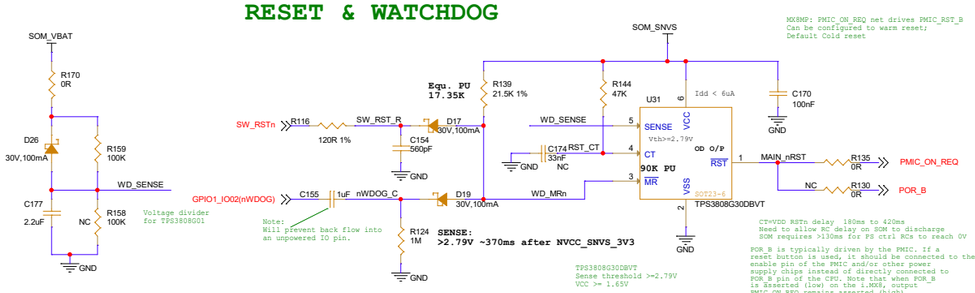
RTC LDO Option



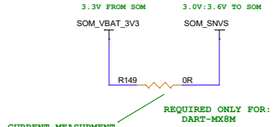
RTC BATTERY



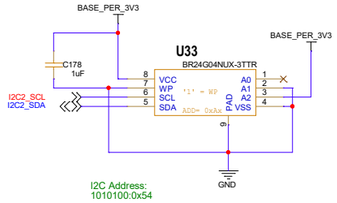
RESET & WATCHDOG



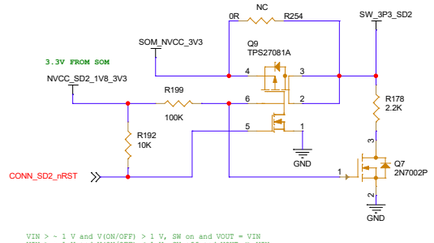
SOM SNVS



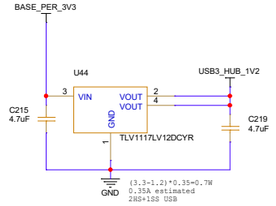
BOARD ID



SD POWER

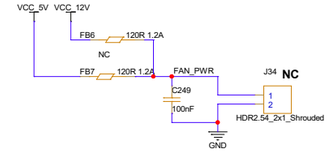


USB3 HUB POWER

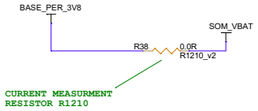


Note: Need to ensure 1.2V rise before OR with 3.3V

FAN : 5V/0.2A



SOM PWR



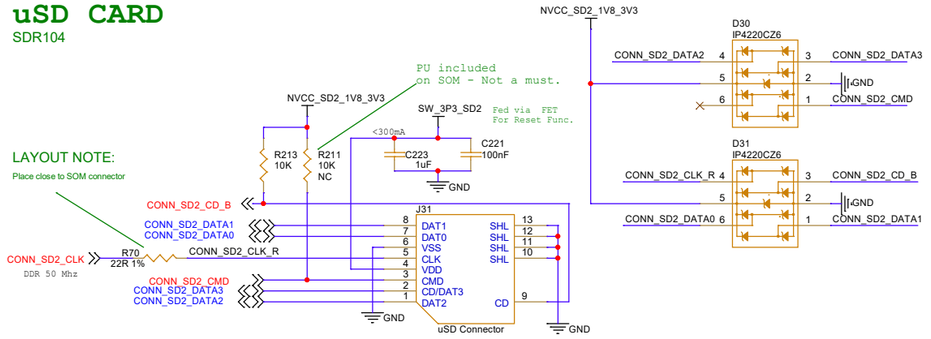
Variscite

Title	04. Power, RTC,Board ID		
Size: Custom	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Tuesday, April 22, 2025		Sheet 14 of 23	

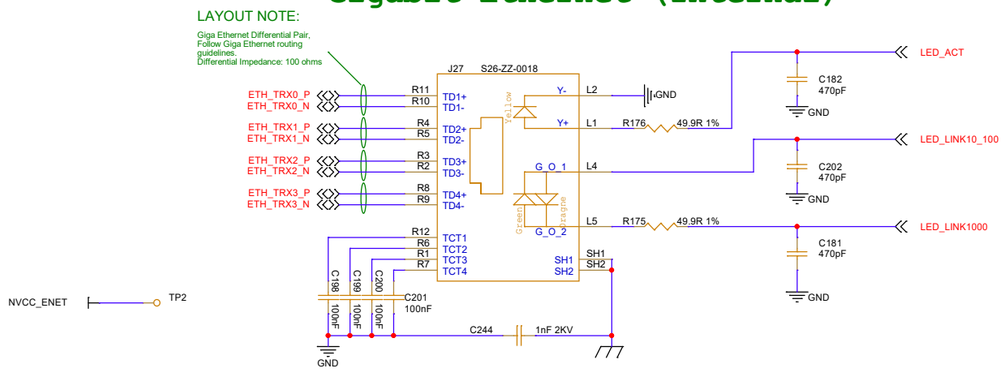
05. ETH, uSD, AUDIO, MIPI-CSI

uSD CARD

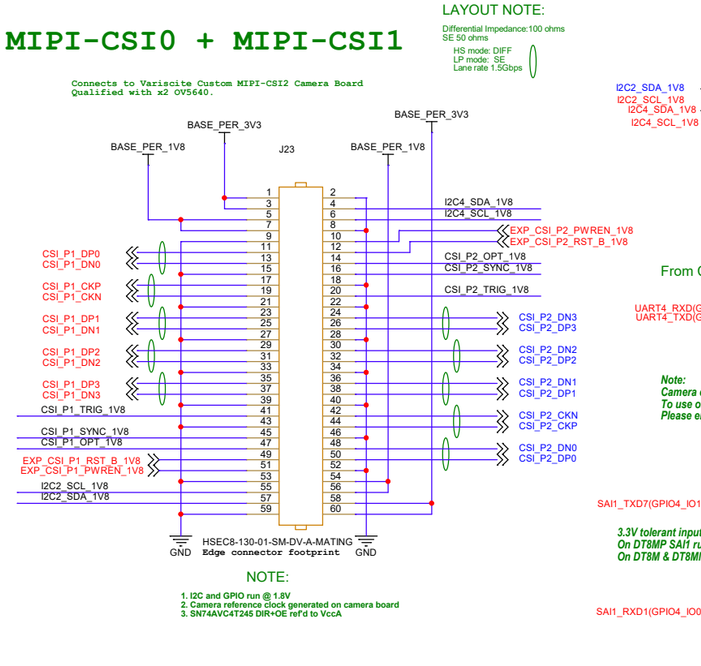
SDR104

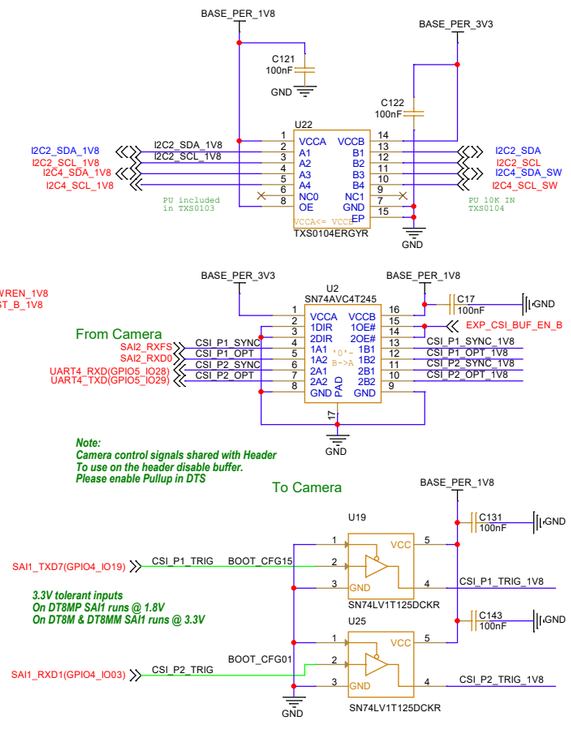


Gigabit Ethernet (Internal)



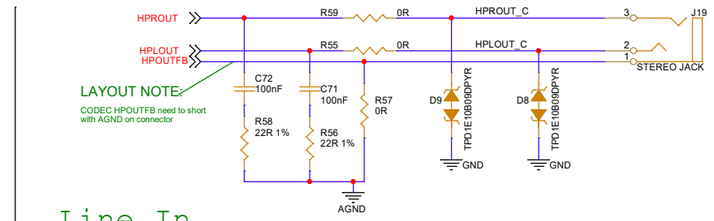
MIPI-CSI0 + MIPI-CSI1



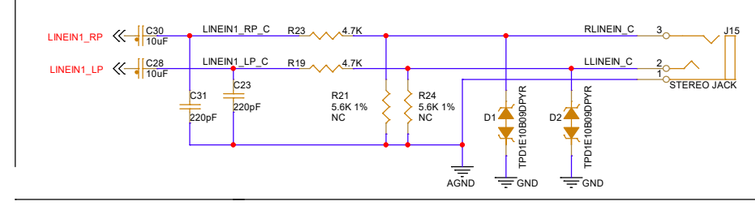


AUDIO

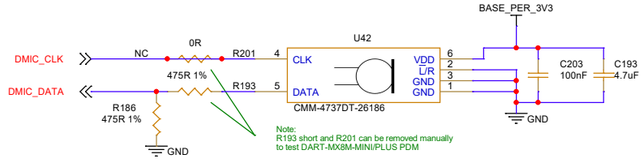
Headphones



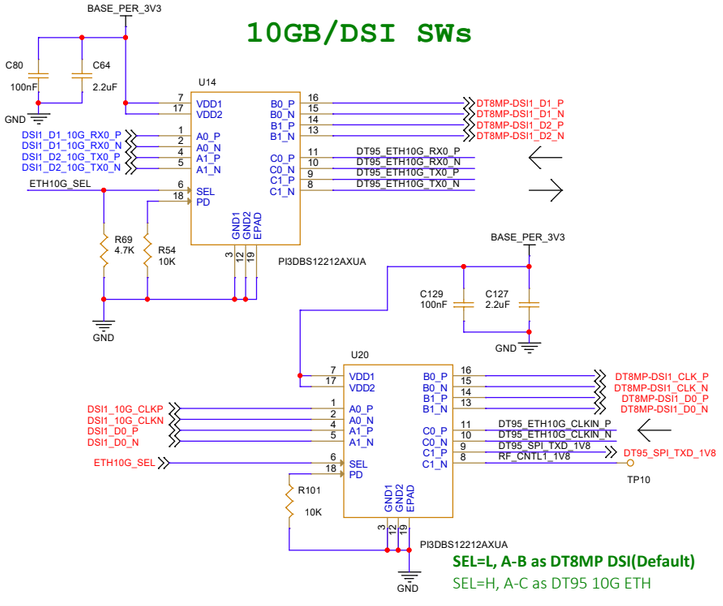
Line In



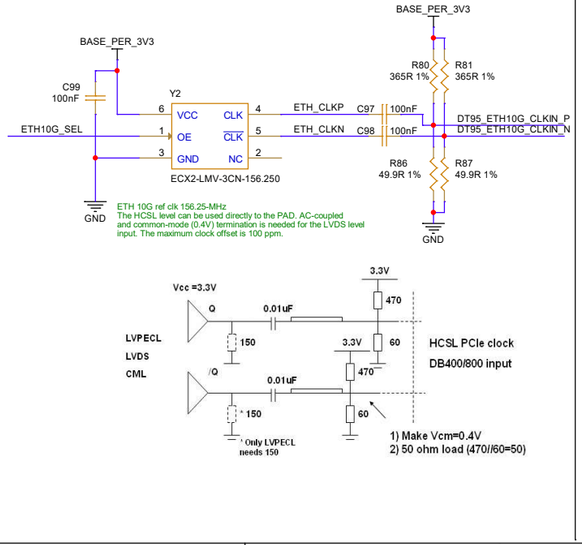
DIGITAL MIC



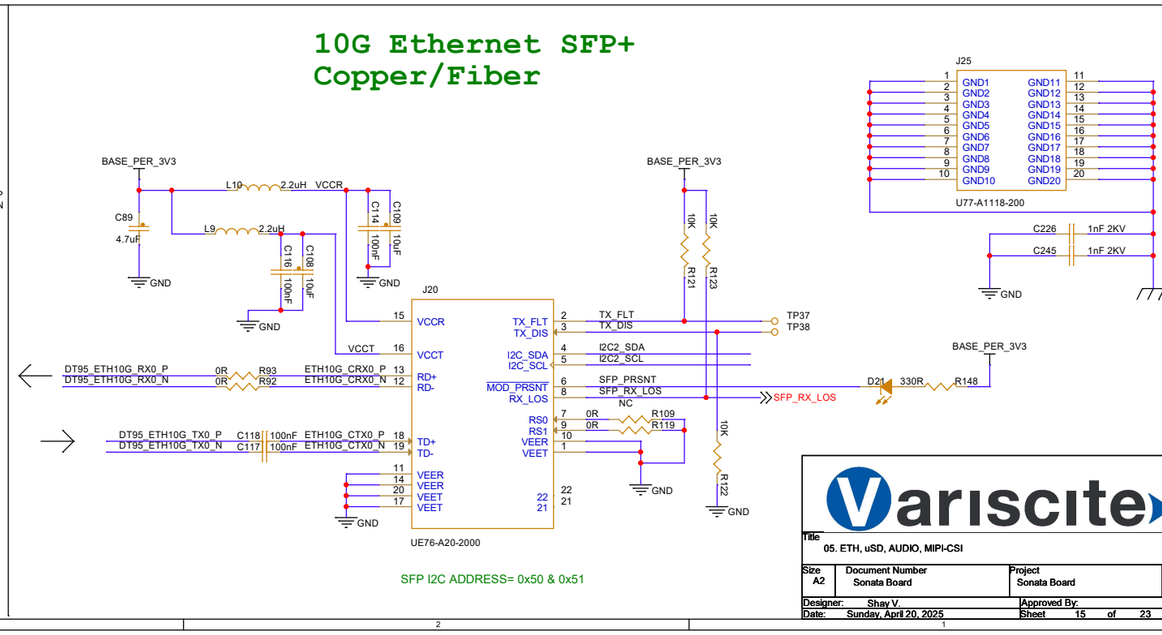
10GB/DSI SWs



ETH 10G ref clk 156.25MHz LVDS



10G Ethernet SFP+ Copper/Fiber



Variscite

Title: 05. ETH, uSD, AUDIO, MIPI-CSI			
Size: A2	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V		Approved By:	
Date: Sunday, April 20, 2025		Sheet 15 of 23	

06. HDMI

HDMI PATH

LAYOUT NOTE: Differential Impedance: 100 ohms

HDMI_TX2_LN2_P
HDMI_TX2_LN2_N
HDMI_TX1_LN1_P
HDMI_TX1_LN1_N
HDMI_TX0_LN0_P
HDMI_TX0_LN0_N
HDMI_CLK_LN3_P
HDMI_CLK_LN3_N

L27 DLM0QSN500HY2: HDMI_CN_D2_P / HDMI_CN_D2_N
L28 DLM0QSN500HY2: HDMI_CN_D1_P / HDMI_CN_D1_N
L29 DLM0QSN500HY2: HDMI_CN_D0_P / HDMI_CN_D0_N
L31 DLM0QSN500HY2: HDMI_CN_CLK_P / HDMI_CN_CLK_N

HDMI_CN_D2_P / HDMI_CN_D2_N
HDMI_CN_D1_P / HDMI_CN_D1_N
HDMI_CN_D0_P / HDMI_CN_D0_N
HDMI_CN_CLK_P / HDMI_CN_CLK_N

HDMI_CEC — 0R R53 — HDMI_CN_CEC — 3.3V Level

HDMI_AUXP — C113 1uF
HDMI_AUXN — C96 1uF
HDMI_CN_Utility/HEAC+ / HDMI_CN_HPD/HEAC- → HDMI_R_Utility/HEAC+
HDMI_CN_SCL / HDMI_CN_SDA

TXS0102 Include 10K PU on A & B ports

HDMI_DDC_SCL — 0R R66
HDMI_DDC_SDA — 0R R60
HDMI_CN_SCL / HDMI_CN_SDA

HDMI_HPD — 0R R77 — HDMI_HPD_CN_3V3

R53 R66 R60 R77
REMOVE TO ACCESS
ALT FUNC. OF MX8MP ON:
HDMI_CEC
HDMI_HPD
HDMI_DDC_SCL
HDMI_DDC_SDA

HDMI EDGE CONNECTOR

VCC_5V
BASE_PER_3V3
J16
HDMI_CN_SCL
HDMI_CN_SDA
HDMI_CN_Utility/HEAC+_R — 0R R82 — HDMI_R_Utility/HEAC+
HDMI_CN_HPD/HEAC-
HDMI_CN_CEC
KEY
HDMI_CN_D0_P / HDMI_CN_D0_N
HDMI_CN_D1_P / HDMI_CN_D1_N
HDMI_CN_CLK_P / HDMI_CN_CLK_N
HDMI_CN_D2_P / HDMI_CN_D2_N
GND
HSEC8-113-01-L-RA-MATING
GND

HDMI REFCLK

Note for OSC2
Assembled for using DART-MX8M HDMI and eDP
- DC coupling and no termination tested with limited monitors to function properly upto 4K resolution.
- Customers designing for DART-MX8M required to modify to AC acoupling and 604 Ohm termination.

BASE_PER_3V3
R129 100K
C161 100nF
GND
OSC1
1 OE — 6 VCC
2 NC — Q
3 GND — Q
HCSL
DSC1104CE2-027.0000T
GND

LAYOUT NOTE: Place close to SOM connector

AC coupled differential low swing clock (HCSL levels)

5HDMI_REFCLKN_R — 0R R125 — HDMI_REFCLKN
4HDMI_REFCLKP_R — 0R R126 — HDMI_REFCLKP

NC R105 49.9R 1%
NC R104 49.9R 1%
GND GND

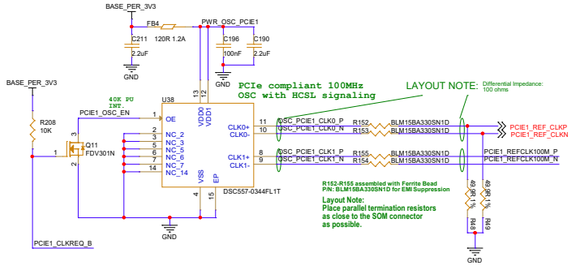
Compatible PN:
DIODES: NX5427001Z
MICROCHIP: DSC1104/24

Variscite

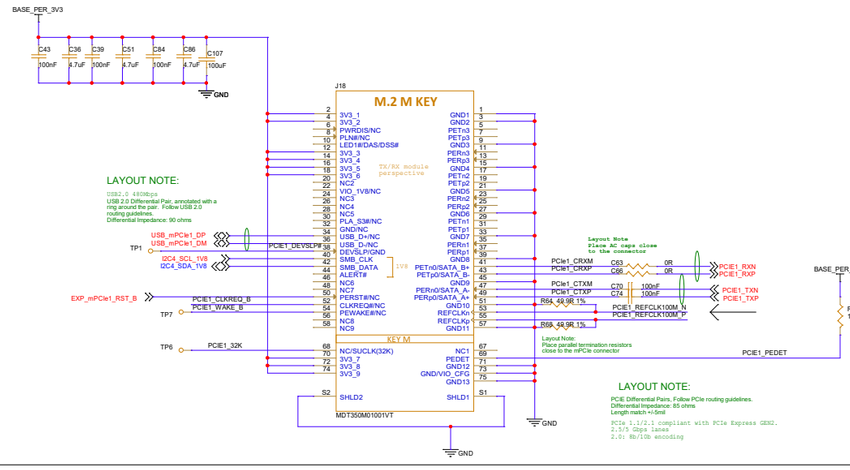
Title: 06. HDMI			
Size: A2	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By: <Approved By>	
Date: Wednesday, April 02, 2025		Sheet 16 of 23	

07. PCIe, QSPI, MIPI-DSI, USB DEBUG

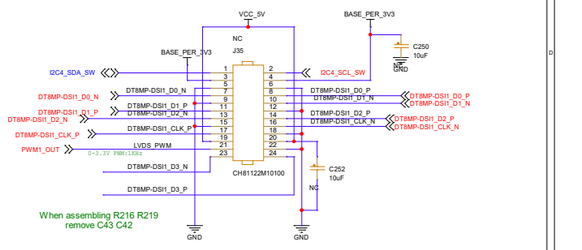
PCIe1 CLK DIST.



PCIe1 M.2 M Key Vertical Connector



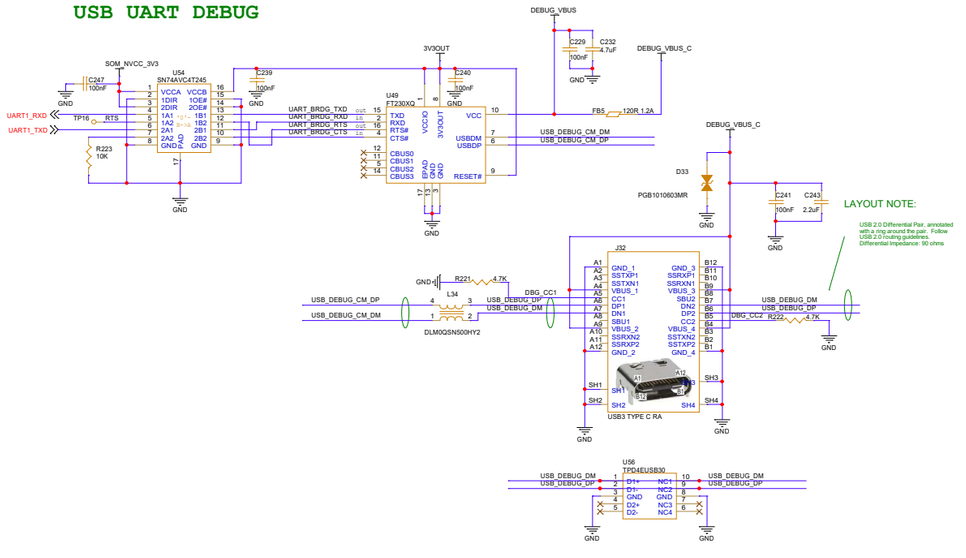
DART-MX8MP MIPI-DSI ON PS Compatible to Symphony J7+J8



PCIe2 CLK DIST.

PCIe2 M.2 M Key Vertical Connector

USB UART DEBUG



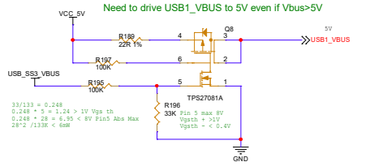
PCIE SWs

Variscite

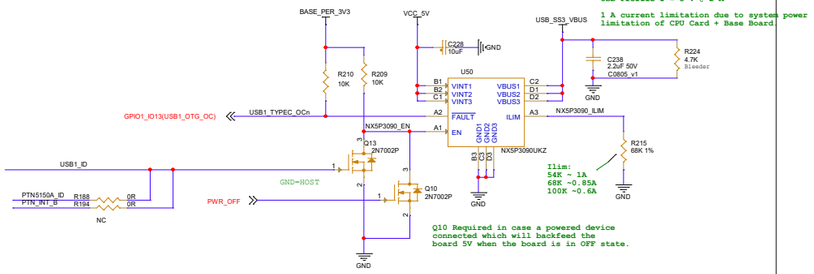
Title: 07. PCIe, QSPI, MIPI-DSI, USB DEBUG			
Size: A1	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	<Approved By>
Date: Wednesday, April 02, 2025		Sheet 17 of 23	

08. USB TYPE C, USB 3 HUB

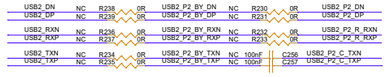
USB#1 - DRP
USB TYPE C



5V Source Load Switch



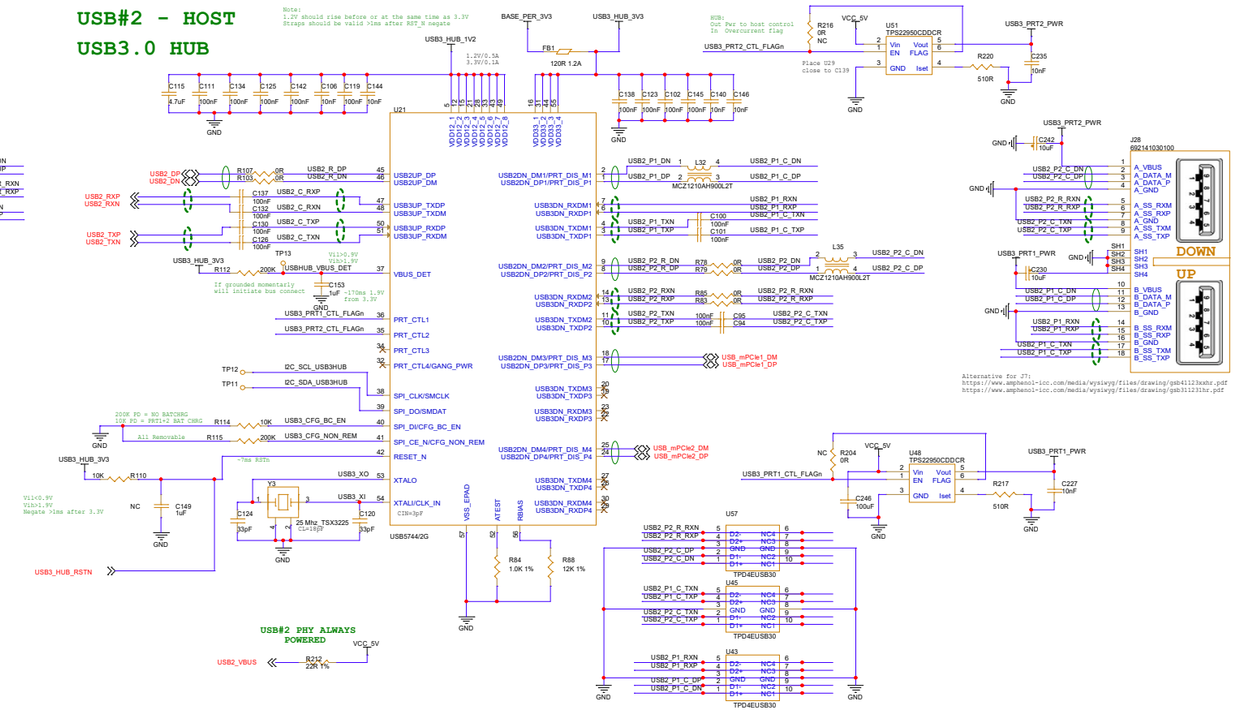
USB HUB Bypass to Port A Connector



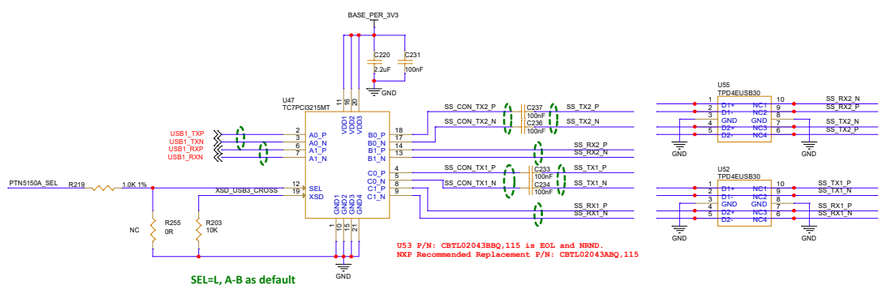
Put @ PS
R239 under R107
R238 under R103
R237 under C137
R236 under C132
R235 under C130
R234 under C126

Put @ PS
R230 under R78
R231 under R79
R232 under R85
R233 under R83
R256 under C95
R257 under C94

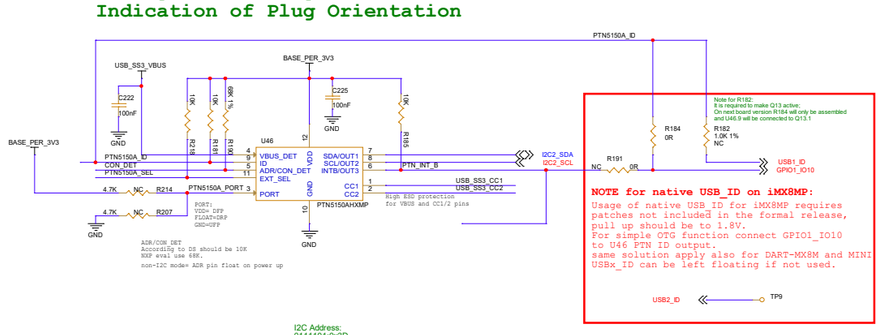
USB#2 - HOST
USB3.0 HUB



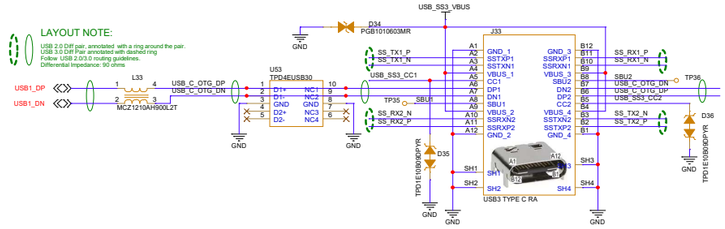
USB3.0 Type-C crossbar switch



Config Channel Logic Detection & Indication of Plug Orientation



I2C Address:
0111101:0x3D

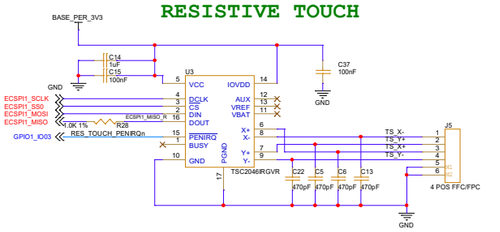


Note:
VBUS active discharge replaced with bleeder

Title: 08. USB TYPE C, USB3 HUB			
Size: A1	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 18 of 23	

09. LVDS, TOUCH, JTAG, I2C EXP

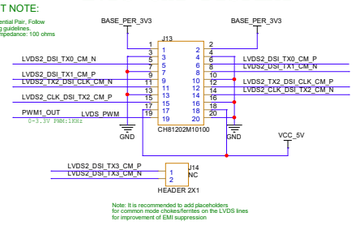
RESISTIVE TOUCH



LVDS CH1 DISPLAY

LAYOUT NOTE:

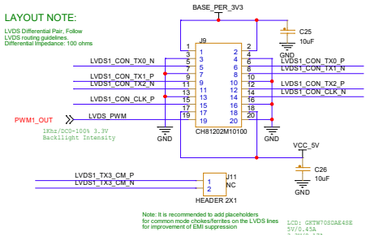
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms



LVDS DISPLAY CH0

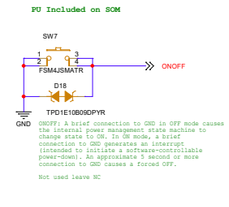
LAYOUT NOTE:

LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

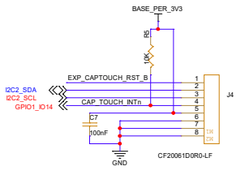


ON/OFF

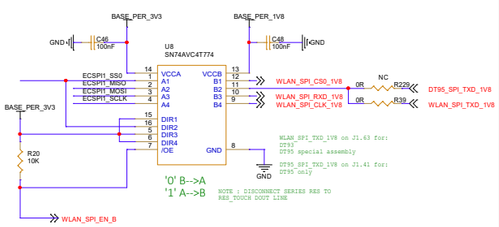
PU Included on SOM



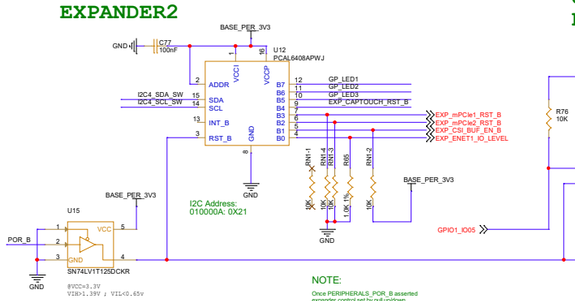
CAPACITIVE TOUCH



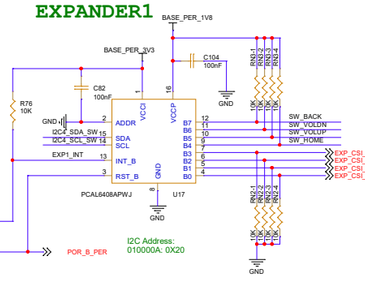
SPI BUFFER for WBE



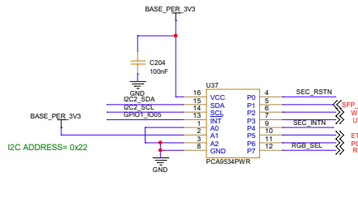
GPIO EXPANDER2



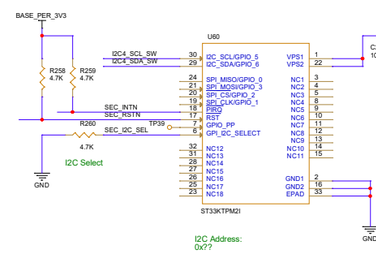
GPIO EXPANDER1



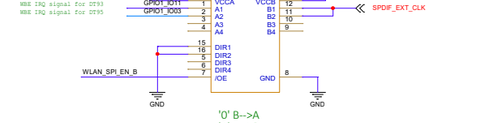
GPIO EXPANDER3



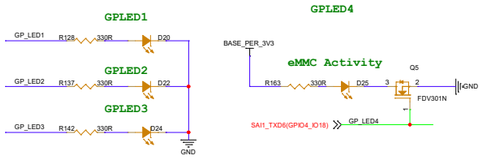
Trusted Platform Module (TPM)



SPI BUFFER for WBE

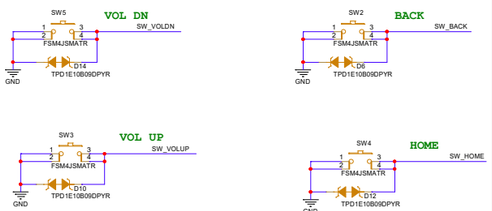


GP LEDS

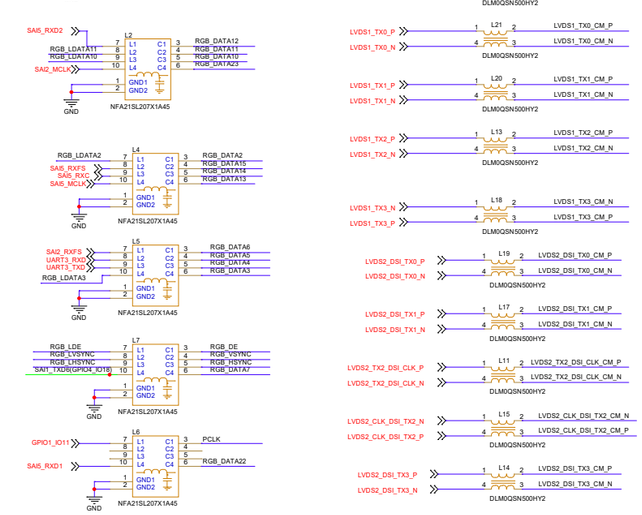


RST

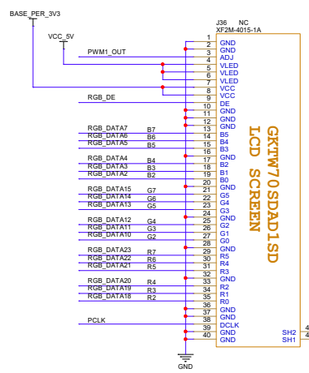
GP BUTTONS



EMI Filters

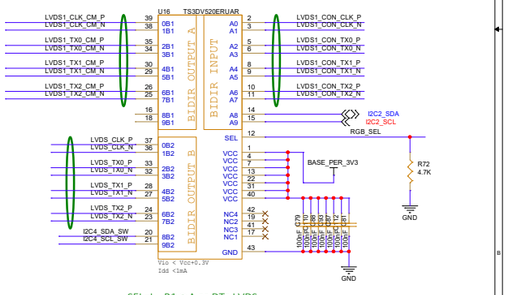


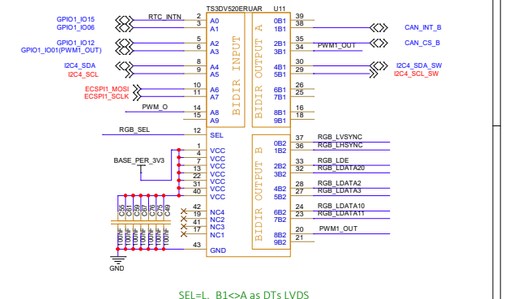
RGB 666 LCD



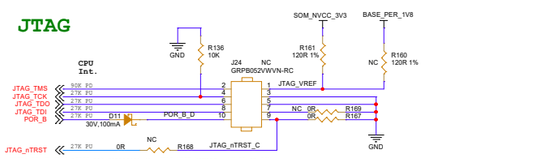
Parallel RGB 666 to LVDS Bridge DT91 24-Bit Color Host to 18-Bit Color LCD

LVDS SWs





JTAG



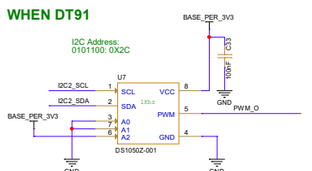
The new 10 pin smaller connector is now becoming an industry standard.

The ARM DStream comes with a 10-pin connector. If you need a ribbon, they can be purchased at Digikey:
Samtec Inc MPN: FTSD-05-D-04.00-01-N

If you need to expand to a 20-pin connector for a different JTAG device, the expander board can also be purchased at Digikey:
Olimex LTD MPN: ARM-JTAG-20-10

https://www.digikey.com/products/en/development-boards-kits-programmers/accessories/783?k=JTAG%20adapter

PWM WHEN DT91



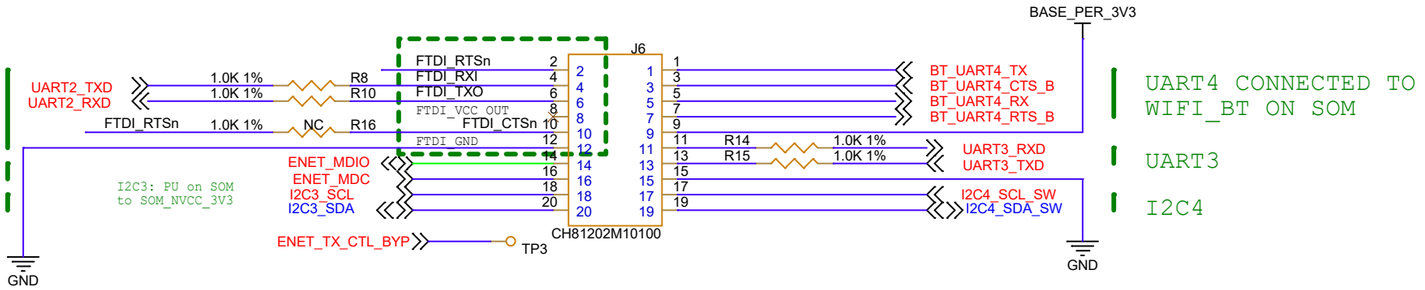
Variscite

Title	09. LCD, TOUCH, JTAG, I2C EXP, SEC		
Size A1	Document Number Sonata Board	Project Sonata Board	Rev 1.1
Designer: Shay V.		Approved By:	
Date: Tuesday, May 13, 2025		Sheet 19 of 23	

10. HEADERS, Mechanics, Pull Ups

UART2 FTDI PINOUT

ENET0 I2C3

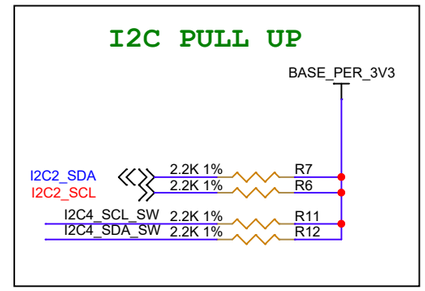


UART4 CONNECTED TO WIFI_BT ON SOM

UART3

I2C4

I2C PULL UP

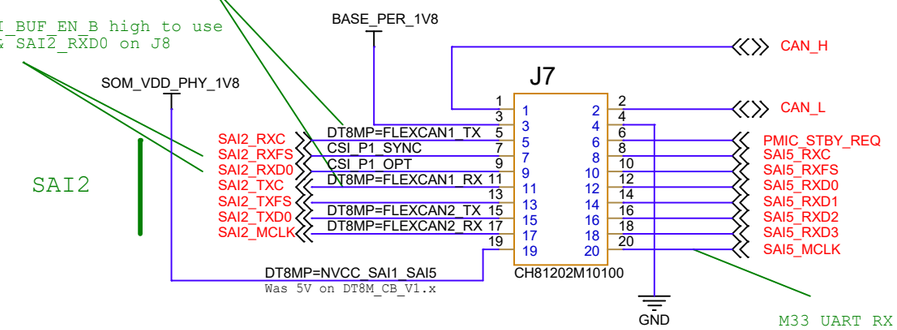


FTDI Adpater can be purchased @ DigiKey :
https://www.digikey.com/product-detail/en/ftdi-future-technology-devices-international-ltd/TTL-232R-3V3/768-1015-ND/1836393
See pinout: http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_TTL-232R_CABLES.pdf

HW NOTE:
Remove R111 & R113 (see CAN-FD page) to use different ALT Func. on J7

SW NOTE:
Set EXP_CSI_BUF_EN_B high to use SAI2_RXFS & SAI2_RXD0 on J8

SAI2



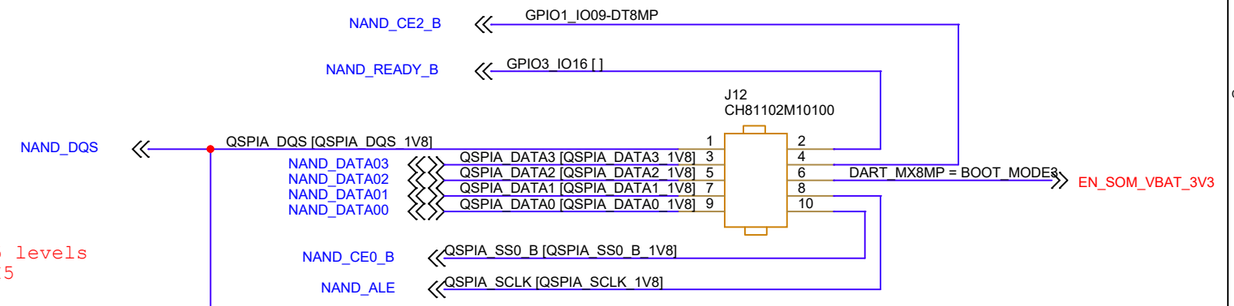
CAN FD

SAI5 RX

DART-MX8MP SAI1 SAI5 levels follow NVCC_SAI1_SAI5

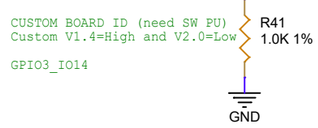
M33 UART RX

QSPI HEADER

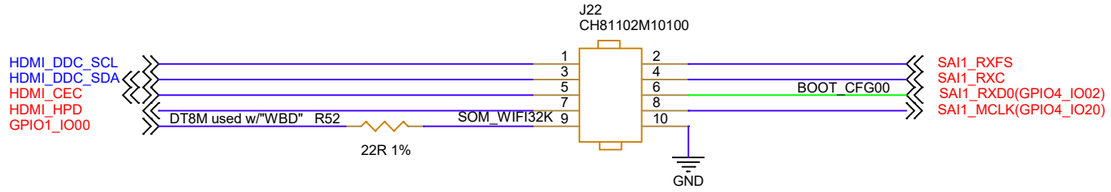


CUSTOM BOARD ID (need SW PU)
Custom V1.4=High and V2.0=Low

GPIO3_IO14



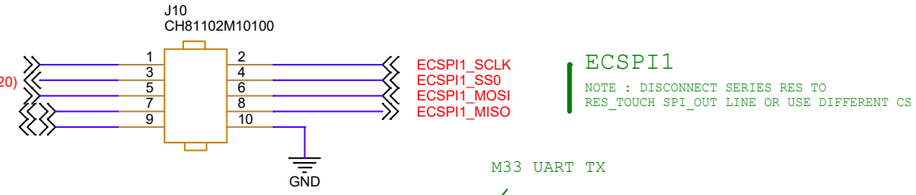
HDMI DDC
HPD CEC



SAI1 RX

SW NOTE:
Requires GPIO on J1.29 configured as interrupt input

BT/WIFI
HOST WAKE
DT8MP CAN



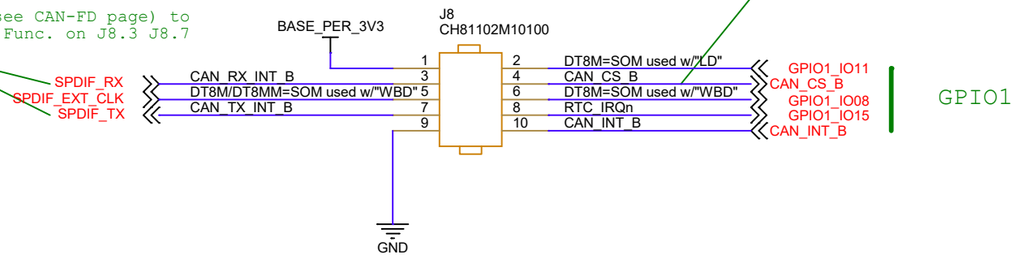
ECSPI1

NOTE : DISCONNECT SERIES RES TO RES_TOUCH SPI_OUT LINE OR USE DIFFERENT CS

M33 UART TX

HW NOTE:
Remove R13 R17 (see CAN-FD page) to use different ALT Func. on J8.3 J8.7

SPDIF

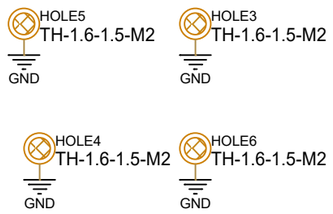


GPIO1

MECHANICS

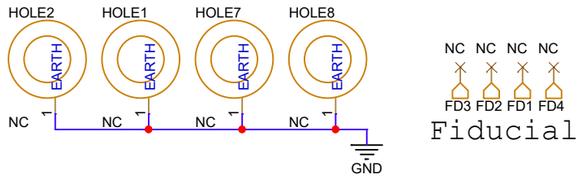
SOM MOUNTING STANDOFF

Place on TOP



VSS0041 NUT M2
VSS0042 X SCREW CONIC HEAD M2

CHASSIS HOLES



Variscite

Title: 10. HEADERS, Mechanics, Pull Ups			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Tuesday, May 13, 2025		Sheet 20 of 23	

11. BOOT CONFIG & MODE

		INT. BOOT	EXT. BOOT	
SAI1_RXD0(GPIO4_IO02)		BOOT_CFG00	0	0 Need to Enable PU in DTS; See pp. 5
SAI1_RXD1(GPIO4_IO03)	CSI_P2_TRIG	BOOT_CFG01	0	0
SAI1_RXD2(GPIO4_IO04)	ENET1_MDC	BOOT_CFG02	0	0
SAI1_RXD3(GPIO4_IO05)	ENET1_MDIO	BOOT_CFG03	0	0
SAI1_RXD4(GPIO4_IO06)	ENET1_RGMII_RD0	BOOT_CFG04	0	0
SAI1_RXD5(GPIO4_IO07)	ENET1_RGMII_RD1	BOOT_CFG05	0	0
SAI1_RXD6(GPIO4_IO08)	ENET1_RGMII_RD2	BOOT_CFG06	0	0
SAI1_RXD7(GPIO4_IO09)	ENET1_RGMII_RD3	BOOT_CFG07	0	0
SAI1_TXD0(GPIO4_IO12)	ENET1_RGMII_TD0	BOOT_CFG08	0	0
SAI1_TXD1(GPIO4_IO13)	ENET1_RGMII_TD1	BOOT_CFG09	0	0
SAI1_TXD2(GPIO4_IO14)	ENET1_RGMII_TD2	BOOT_CFG10	0	1
SAI1_TXD3(GPIO4_IO15)	ENET1_RGMII_TD3	BOOT_CFG11	0	0
SAI1_TXD4(GPIO4_IO16)	ENET1_RGMII_TX_CTL	BOOT_CFG12	0	1
SAI1_TXD5(GPIO4_IO17)	ENET1_RGMII_TXC	BOOT_CFG13	1	0
SAI1_TXD6(GPIO4_IO18)	GP_LED4	BOOT_CFG14	0	0
SAI1_TXD7(GPIO4_IO19)	CSI_P1_TRIG	BOOT_CFG15	0	0

10K R241 NC BOOT_CFG00 — SAI1_RXD0(GPIO4_IO02)
10K R245 NC BOOT_CFG01 CSI_P2_TRIG — SAI1_RXD1(GPIO4_IO03)
10K R240 NC BOOT_CFG02 ENET1_MDC — SAI1_RXD2(GPIO4_IO04)
10K R248 NC BOOT_CFG03 ENET1_MDIO — SAI1_RXD3(GPIO4_IO05)
10K R242 NC BOOT_CFG04 ENET1_RGMII_RD0 — SAI1_RXD4(GPIO4_IO06)
10K R246 NC BOOT_CFG05 ENET1_RGMII_RD1 — SAI1_RXD5(GPIO4_IO07)
10K R244 NC BOOT_CFG06 ENET1_RGMII_RD2 — SAI1_RXD6(GPIO4_IO08)
10K R253 NC BOOT_CFG07 ENET1_RGMII_RD3 — SAI1_RXD7(GPIO4_IO09)
GND

POR_B_PER
R165 10K
C179 4.7uF
GND
POR_B_PER_DELAY

SOM_NVCC_3V3
C186 100nF
GND

Vih >1.39V
Vil <0.65V

U35 SN74LV1T125DCKR
BOOT_CFG
1 2 3 GND 4 VCC 5

10K R252 NC BOOT_CFG08 ENET1_RGMII_TD0 — SAI1_TXD0(GPIO4_IO12)
10K R243 NC BOOT_CFG09 ENET1_RGMII_TD1 — SAI1_TXD1(GPIO4_IO13)
GND

10K R145 BOOT_CFG10 SAI1_TXD2(GPIO4_IO14) — SAI1_TXD2(GPIO4_IO14)

10K R251 NC BOOT_CFG11 ENET1_RGMII_TD3 — SAI1_TXD3(GPIO4_IO15)
GND

U36 SN74LV1T125DCKR
1 2 3 GND 4 VCC 5

10K R140 BOOT_CFG12 SAI1_TXD4(GPIO4_IO16) — SAI1_TXD4(GPIO4_IO16)

U30 SN74AUP1G240DCK
1 2 3 GND 4 VCC 5

C169 100nF GND

10K R138 BOOT_CFG13 SAI1_TXD5(GPIO4_IO17) — SAI1_TXD5(GPIO4_IO17)
10K R174 NC BOOT_CFG14 GP_LED4 — SAI1_TXD6(GPIO4_IO18)
10K R247 NC BOOT_CFG15 CSI_P1_TRIG — SAI1_TXD7(GPIO4_IO19)
GND

U35 U36 U30 Note:
* Tristate buffers required not to pull ENET1 to 3.3V while running @ lower voltage.
* Buffers required for DART-MX8M & DART-MX8M-MINI
* For DART-MX8M-PLUS only U35 required

Notes:
a. Sampled on rising edge of POR_B
b. SOC PD during POR_B and after on BOOT CFG[15:0] and BOOTMODE[1:0]
c. BOOT_MODE[1:0] ="10" is Internal Boot - Always used.
d. Active boot cfg for one dip sw sel EXTERNAL/INTERNAL

DART-MX8M-MINI Notes:
b. Boot config lines do not follow the Mini datasheet in full DART-MX8M-MINI have added logic to be compatible to DART-MX8M

DART-MX8M-PLUS Notes:
a. Boot configuration set only by SAI1_TXD2 connected on DART via buffer to BOOT_MODE0

i.MX8M Plus Boot Mode

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit) Default
0	0	1	1	USDHC2 (SD boot only, SD2)

CustomBoard Net: BOOT_MODE0 SAI1_TXD2 EN_SOM_VBAT_3V3 BOOT_MODE1

DART-MX8MP BOOT MODE

SOM_NVCC_3V3
R151 10K
BOOT_CFG
SW8 TDA01H0SB1R
D23
GND

BOOT CFG PRIORITY:
H Ext. SD Card
L Int. eMMC

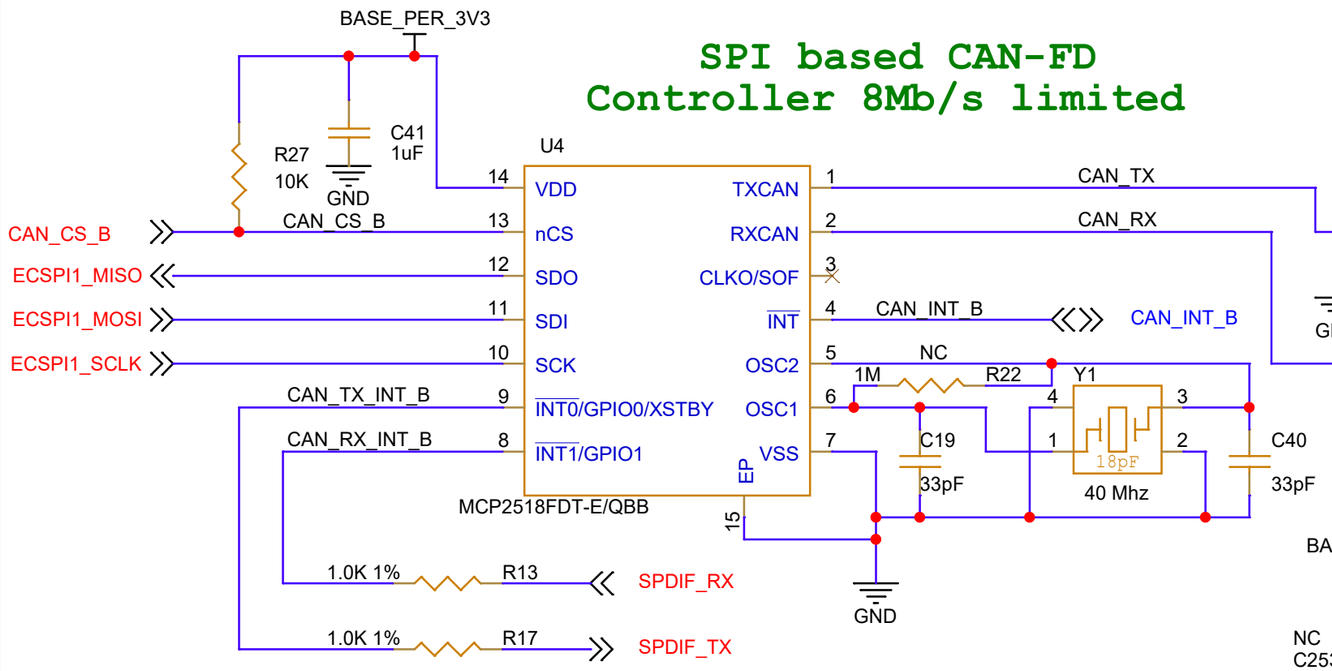
SOM_NVCC_3V3
R146 4.7K
R147 4.7K NC
BOOT_MODE0
BOOT_MODE1
R156 10K NC
R157 4.7K
GND

Variscite

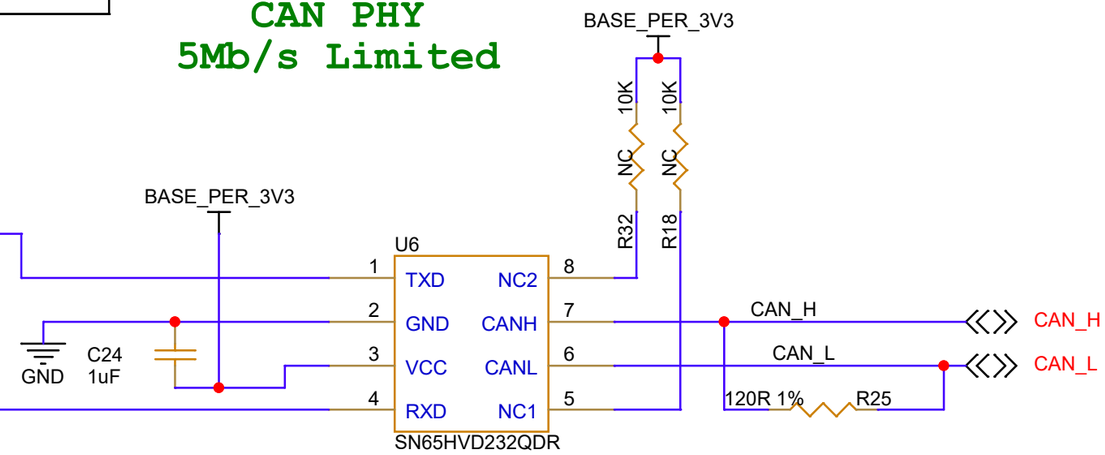
Title: 11. BOOT CONFIG & MODE			
Size: B	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 21 of 23	

12. CAN FD Interface

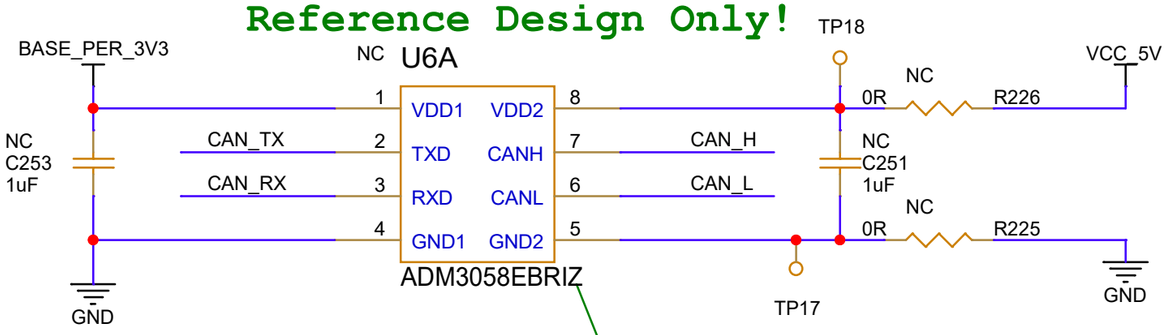
SPI based CAN-FD Controller 8Mb/s limited



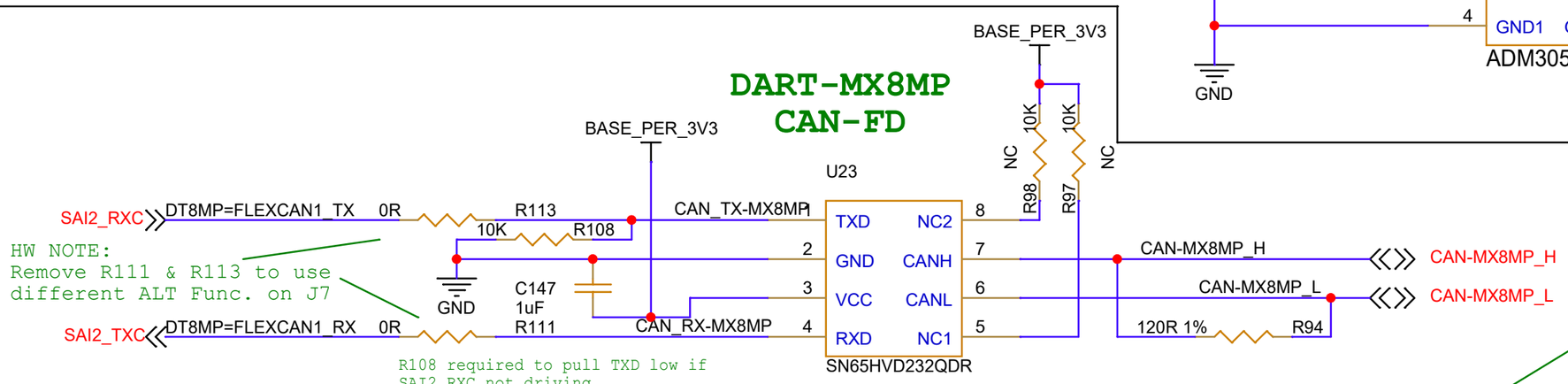
CAN PHY 5Mb/s Limited



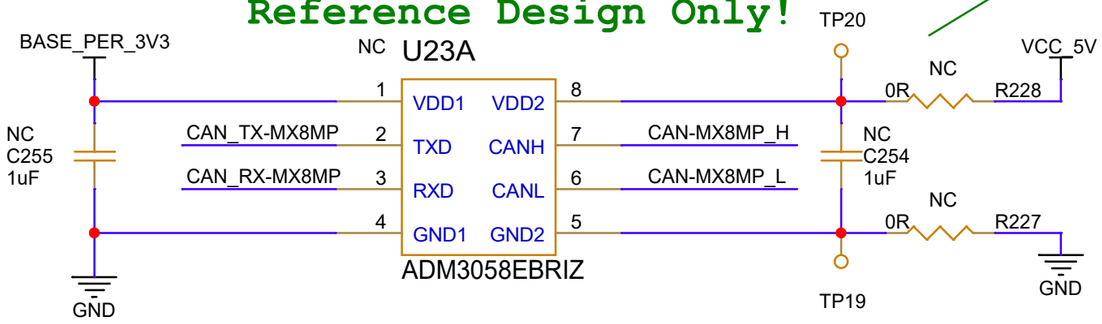
CAN PHY 12Mb/s Reference Design Only!



DART-MX8MP CAN-FD



CAN PHY 12Mb/s Reference Design Only!



NOTE FOR U6A U23A

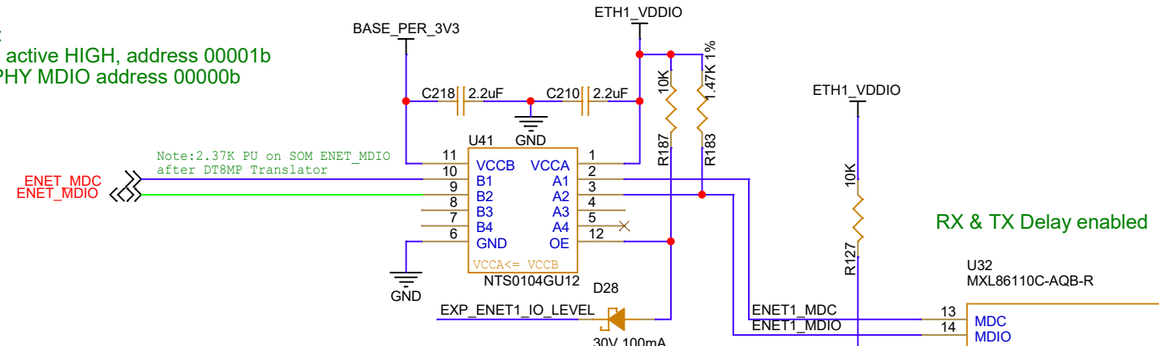
- Located on bottom side
- When assembling the ADM3058E IC removal of TCAN332 is a must!

Variscite

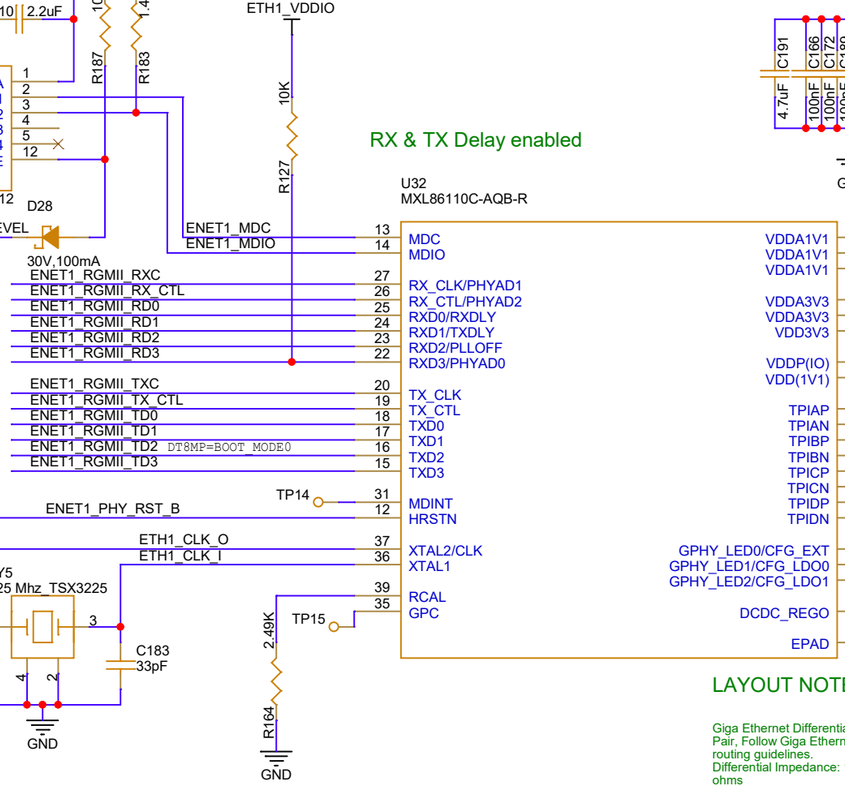
Title: 12. CAN FD Interface			
Size: A4	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, April 02, 2025		Sheet 22 of 23	

13. ENET1 Gigabit Ethernet

Straps:
LEDs - active HIGH, address 00001b
SOM PHY MDIO address 00000b

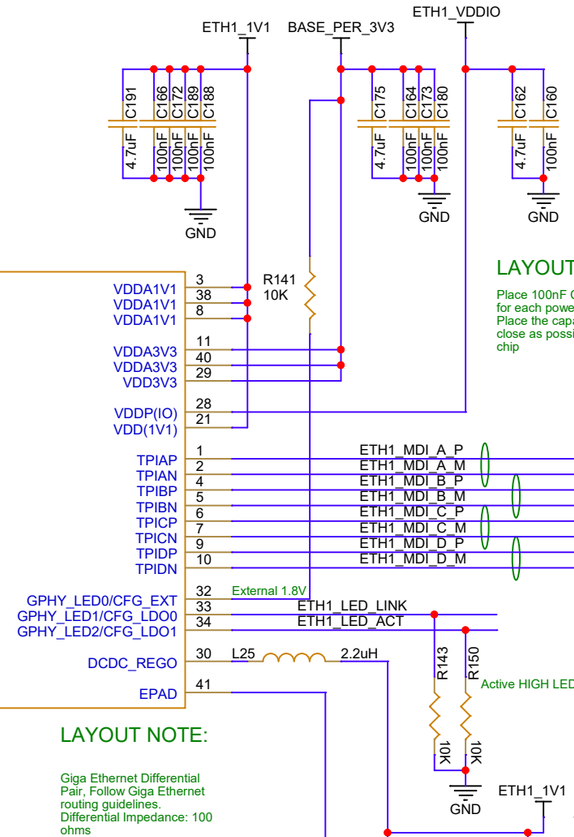


RX & TX Delay enabled



NOTE for EXP_ENET1_IO_LEVEL:
L: 3.3V (PHY in RESET - IOs tristated and 3.3V tolerant)
H: 1.8V (PHY active)

For a simplified design connected directly to a free GPIO;

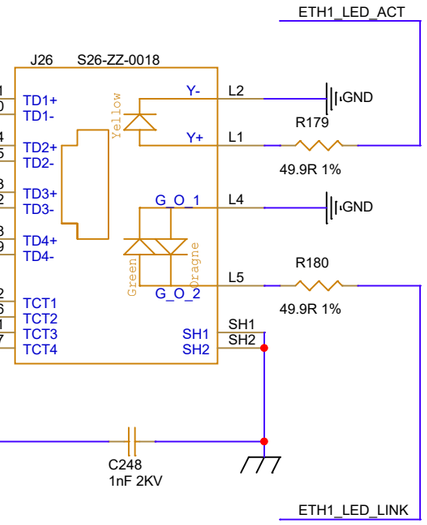


LAYOUT NOTE:

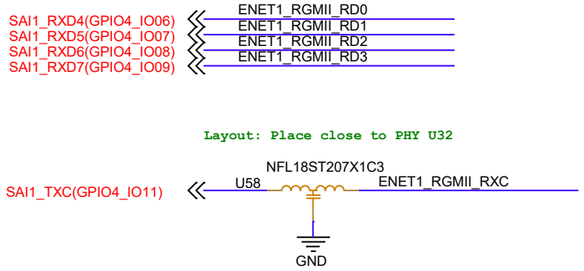
Giga Ethernet Differential Pair, Follow Giga Ethernet routing guidelines.
Differential Impedance: 100 ohms

LAYOUT NOTE:

Place 100nF Capacitors for each power pin
Place the capacitors as close as possible to the chip

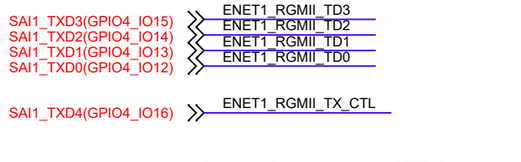


RGMII RX

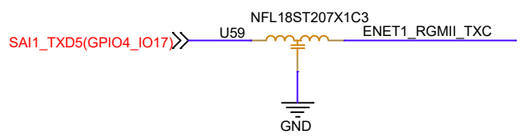


Layout: Place close to PHY U32

RGMII TX



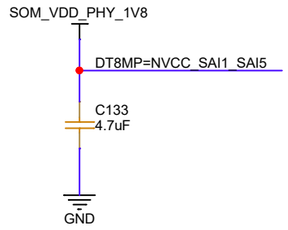
Layout: Place close to DART J2



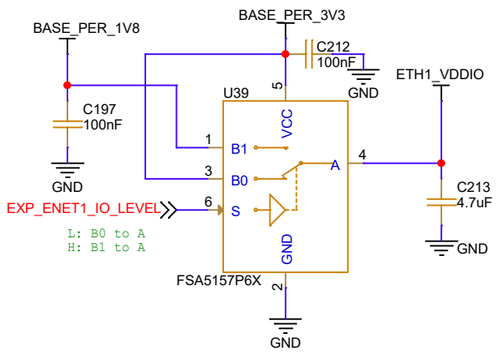
NOTE:
For DT8MP net SOM_VDD_PHY_1V8 connected to NVCC_SAI1_SAI5 which is an output from the DT8MPprogrammable PMIC LDO.

This output voltage will set SAI1 and SAI5 pads voltage level;
With DT8MCustomBoard-V1.x and earlier it is set to 3.3V. On DT8MCustomBoard-V2.x it is set to 1.8V for RGMII.

Bypass with 4.7uF min. 6.3V capacitor.

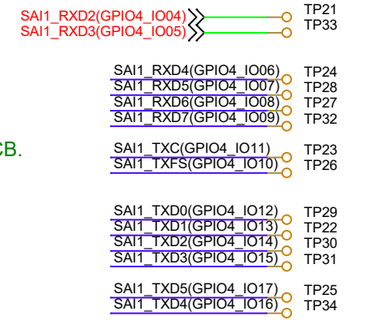


NOTE for U63:
Required for compatibility to DT8M & DT8MM where SAI1 levels are fixed to 3.3V;



NOTE:
Test points used to access DT8M & DT8MM SAI1 signals;

Levels are fixed to 3.3V by modules;
These test points located on the Print Side of the PCB.



Variscite

Title: 13. Ethernet2			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Tuesday, April 22, 2025		Sheet 23 of 23	